Combined In-Pixel Linear and Single-Photon Avalanche Diode Operation With Integrated Biasing for Wide-Dynamic-Range Optical Sensing

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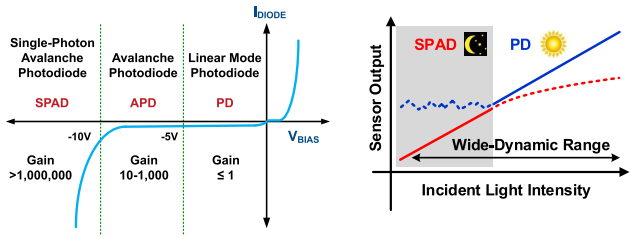
***Abstract*— This article presents a fully integrated, wide linear dynamic range (DR) optical sensor array combining linear and single-photon avalanche diode (SPAD) operation within each pixel. A pulse-counting readout scheme provides in-pixel digitization in an area-efficient manner for both the operation modes, enabling fully parallel measurement across the array. The proposed dual-mode optical sensor array alternately requires high-voltage (10–20 V) and low-voltage supply (2–5 V) for reverse bias of the photodiodes, which is provided by a reconfigurable, closed-loop high-voltage charge pump in the same substrate. An 8 × 8 array architecture along with the dual-mode bias generator is fabricated in a general purpose 180-nm CMOS process and demonstrates 129-dB DR while maintaining linear photoresponse operating with a dual-mode frame rate of 20 Hz. We present a pixel design methodology for implementing a dual-mode optical sensor scalable to an array format, as well as high-voltage dc–dc conversion in a low-voltage CMOS process.**

***Index Terms*— Complementary metal–oxide–semiconductor (CMOS), high-voltage charge pump, image sensors, optical sensors, photodiode, single-photon avalanche diode (SPAD), wide dynamic range (DR).**

I. Introduction

OPTICAL detectors and imaging arrays leveraging complementary metal–oxide–semiconductor (CMOS) process technologies serve a wide range of applications, including consumer and scientific imaging, 2-D/3-D range finding, ambient light detection, and optical communication links. In many such applications, the ability to operate over a wide range of incident optical power is a critical performance metric, described by the optical dynamic range (DR). For example, wide DR enables imaging of highlights and shadows in conventional CMOS image sensors (CISs) [1]. Wide DR is also important in chemical and biological sensing applications, where the expected signal can range from 10^5 photons/cm^2·s for bioluminescence-based detection [2], [3] to 10^{10}–10^{11} photons/cm^2·s for fluorescence-based detection [4]–[6] and upward of 10^{20} photons/cm^2·s for optical transmission or absorption measurements.



(a) (b)

Fig. 1. (a) Photodiode current response with respect to bias voltage; reverse-bias regions are annotated. (b) Linear (PD) and single-photon (SPAD) operations are combined to extend optical DR.

CMOS optical detectors use a reverse-biased photodiode for signal transduction; the regions of operation for such detectors are illustrated in Fig. 1(a). Many of these systems operate in the linear regime (PD-mode) at low reverse bias, where high quantum efficiency and low deep-sub-electron read noise (DSERN) are needed for wide DR as well as low-light performance [7]. As the CMOS technology scales to smaller technology nodes, decreasing diode capacitance increases charge-to-voltage conversion gain, along with adverse effects, including limited quantum efficiency, increased leakage current, limited full-well capacity (FWC), and reduced signal swing. Enhanced conversion gain or two-stage charge conversion with lateral overflow gates has achieved low-noise and wide DR, yet these approaches are limited to low FWC and are not well suited to standard CMOS processes [8]–[11]. Noise reduction techniques, such as correlated multiple sampling, have been used to demonstrate ultra-low read noise without significant signal gain [12], which leads to longer integration time. A quanta image sensor (QIS) with jot devices has also demonstrated DSERN pixel performance [7], but a fine CIS-specific CMOS process is necessary to reduce floating

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diffusion capacitance. The jot device has limited FWC, where even multi-bit jot has a few hundreds of electrons of FWC; this requires many multiple jots to implement wide DR.

Companding or multi-mode (linear-logarithmic) wide DR CISs can increase DR utilizing linear photoresponse at low illumination and logarithmic response at high illumination [13], [14], but these suffer from increased fixed-pattern noise, reduced sensitivity, and reduced signal swing. A range of techniques, such as multi-shutter measurements [15], spatio-temporal oversampling, and time-to-saturation [16], have been demonstrated to increase DR at the cost of degraded frame rate [17] or increased complexity.

As an alternative to the PD-mode operation, the single-photon avalanche mode (SPAD-mode) operation can significantly enhance optical sensitivity, where an above-breakdown reverse bias yields an avalanche multiplication gain of 10^5–10^6. This mode also provides a pulse-based digital output and fast impulse response, but DR may be limited by saturation at low illumination levels or limited to binary images. As such, CMOS-integrated SPAD detectors have been used primarily for time-of-flight (TOF) range imaging and fluorescence lifetime imaging (FLIM) using high sensitivity and actively controlled illumination sources [18]. Recent work has significantly increased DR by oversampling binary pixel data [19], [20], an extension of the QIS [21]. Despite this increased DR, high oversampling ratios and increased readout overhead are a challenge in very high-intensity illumination, which may limit achievable bright-light performance for these solely SPAD-based approaches. While photon detection DR of 152 dB has also been demonstrated without oversampling [22]–[24], which is attributed to a short dead time (<10 ns) and low dark count rate (DCR) (<10 cps), it requires a custom HV CMOS process and low operating temperature (−20 °C).

To extend optical DR, linear and single-photon regimes can be combined, as illustrated in Fig. 1(b). This approach has been demonstrated previously using a vertical avalanche photodiode (VAPD)-based CIS structure [25], [26] or using a standard CMOS-integrated *p*-*n* photodiode with separate linear and SPAD readout circuits [27]. While providing enhanced DR and very low DCR, using a VAPD-based CIS approach limits detector output to single-photon binary output in low-illumination rather than quantified intensity, and it employs a relatively complex diode structure. In these approaches, readout has been limited to column-based [25], [26] or single-detector [27] output by the required readout circuit area.

To provide fully parallel operation of arrayed, wide-DR optical detectors at a high sample rate, linear and single-photon operations were combined at the pixel level in [28]. This article expands on [28] with design considerations for combining PD-mode and SPAD-mode operations in a single dual-mode pixel, including a block-level circuit architecture, detailed electrical and optical measurements, and an analysis of dual-mode switching to maximize linearity over a wide DR. In addition, a fully integrated sensor system on chip is demonstrated, including integrated on-chip generation of high-voltage (>10 V) and low-voltage (<5 V) detector biases in a general purpose 0.18-μm CMOS process.

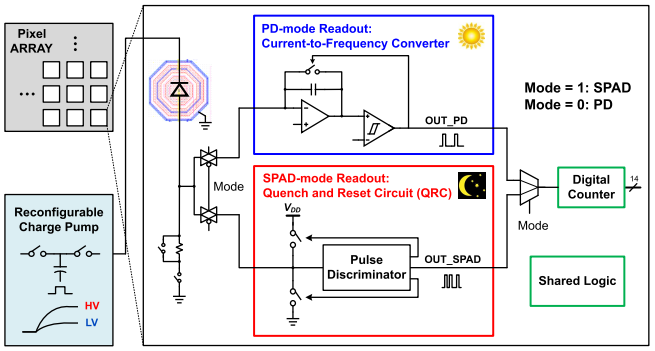


Fig. 2. Pixel consists of a photodiode and readout circuits; a current-to-frequency converter measures photocurrent in PD-mode, and a QRC counts SPAD-mode current pulses. Peripheral digital blocks are shared, including a digital counter for in-pixel accumulation.

Integrating multi-mode photodiode readout at the pixel level necessarily decreases fill factor, and the proposed approach is primarily intended to provide parallel, fast optical detectors for biomedical and biosensing applications, rather than for CIS and high-resolution imagers. For these applications, CMOS optical sensors are pitch-matched with microarrays or microwells containing DNA, cells, or proteins [6], [29]. Sensor pitch is limited by bio-spotting resolution, where individual wells or spots must be spatially separated to avoid physical, chemical, and optical crosstalk. As such, pixel pitch requirements are significantly relaxed compared with conventional CIS applications and 80–100 μm is typical [6]. In addition, using in-pixel quantization enables fully parallel readout with individual addressing, eliminating the need for time-division multiplexing and increasing detector sample rate.

The remainder of this article is organized as follows. Section II describes dual-mode pixel architecture and its design constraints. Section III describes an array of dual-mode sensor pixels with integrated PD/SPAD bias generator. Section IV presents measured electrical and optical performance from the fabricated sensor IC. Section V provides a summary of conclusions and discussion of future work.

II. Dual-Mode Pixel Architecture

The pixel-level readout architecture is shown in Fig. 2, which supports both linear (PD-mode) and SPAD-mode operations from a shared photodiode. The diode operation can be alternately switched between linear and single-photon modes by applying low-voltage (<10 V) and high-voltage (>10 V) reverse biases at the cathode. Photodiode current is measured by one of two readout circuits, as the anode is routed to each readout circuit through a transmission-gate analog multiplexer controlled by a mode-selection signal. While the photodiode cathode is exposed to above-breakdown voltage bias for the CMOS process, each readout circuit block is implemented using low-voltage devices; the anode is driven by each readout either behaving as a virtual ground (PD-mode) or sensing node (SPAD-mode) actively driven to ground or VDD, allowing low-voltage devices to be used for readout.

To support pixel-level dual-mode operation, each photodiode is co-located (Fig. 2) with a current-to-frequency

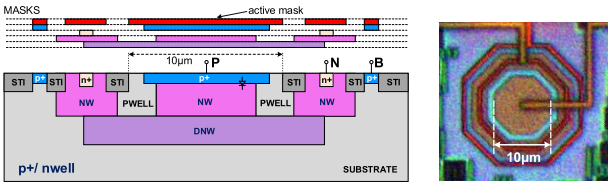


Fig. 3. Illustrated cross-sectional view and top view of die photograph of the p+/n-well junction PD/SPAD device fabricated in a general purpose 0.18-μm CMOS process (figure modified from [30]).

TABLE I
DIODE CHARACTERISTICS

Junction	Active area	Dark current	Median DCR (V_{ex})	PDP (V_{ex}, λ)
p+/n-well	53 μm^2	50 fA	135 kcps (0.8 V)	2.5 % (0.8 V, 565 nm)

converter for measuring continuous photocurrent (top), as well as a quench and reset circuit (QRC) for controlling pulse-based SPAD operation (bottom). Both readout circuits produce a digital pulse stream output, which is integrated using a local digital counter. To minimize the area for readout circuits, a few peripheral digital blocks are shared using multiplexers, including a 14-bit ripple counter and fixed-width, one-shot pulse generators. The photodiode bias required for each mode operation is supplied by a reconfigurable charge pump, which provides adjustable high-voltage (>10 V) and low-voltage (<5 V) reverse biases for fully integrated SPAD/PD operation.

A. Dual-Mode Photodiode

Each pixel contains a photodiode constructed from general purpose CMOS layers that can be operated alternately as a PD-mode detector and SPAD-mode detector, depending on the applied reverse bias. Fig. 3 shows a cross section of the photodiode structure used for this article, where the primary p-n junction is formed between the p+ and n-well (NW) layers. An additional n-well/deep-n-well (DNW) guard ring is added, forming an isolated p-well to mitigate premature edge breakdown [30]. The photodiode has an octagonal active area with a diameter of 10 μm, and the reverse-bias breakdown voltage of p+/n-well junction is measured at 11.2 V. For linear-mode operation, the photodiode is reverse-biased at approximately 2 V, well below the junction breakdown voltage; for single-photon avalanche operation, the photodiode is reverse-biased at 12 V, beyond the junction breakdown voltage, providing an over-voltage of approximately 800 mV. The diode characteristics including dark current in PD-mode and DCR and photon detection probability (PDP) in SPAD-mode are summarized in Table I.

B. PD-Mode Readout: Current-to-Frequency Converter

Several optical sensor array designs employing per-pixel analog-to-digital converter (ADC) for CISs and biochips have been demonstrated [2], [4], [6], [31], [32], where a slope-based ADC or a delta–sigma ADC is incorporated into each pixel. Alternately, current-to-frequency converter architectures

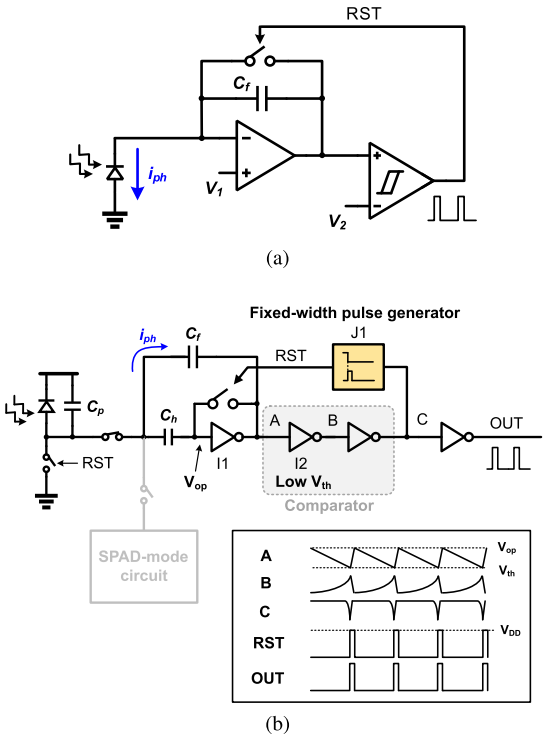


Fig. 4. (a) General current-to-frequency converter architecture. (b) Proposed inverter-based architecture with illustrated transient operation.

for optical sensor arrays have been reported in [28], [33], and [34]. This approach has also been used to provide wide DR for other current-mode sensors using a transimpedance amplifier (TIA) followed by a comparator [35], similar to the circuit illustrated in Fig. 4(a).

The current-to-frequency converter, which serves as a pulse frequency modulation (PFM)-based readout circuit, is advantageous in this context over conventional voltage-mode ADCs [36]: its input DR is no longer limited by the power supply rails; second, no additional sampling clock is needed; data transmission bandwidth is much lower than an over-sampling delta–sigma ADC [6]; and pulse accumulation provides inherent first-order, low-pass filtering by counting pulses in a fixed time window.

A current-to-frequency converter is illustrated in Fig. 4(a). In this architecture, photocurrent $i_{\rm ph}$ is converted to a proportional reset pulse rate $f_{\rm out}$; a comparator continuously compares the integration voltage ramp V_1 to a voltage reference, V_2, and a self-resetting digital pulse is generated. The resulting current-to-frequency conversion can be described for the ideal (zero switch time) case as

$$\frac{N}{t_w} = \frac{i_{\rm ph}}{C_f(V_1 - V_2)} = f_{\rm out} \tag{1}$$

where N output pulses occur in a set integration time window, t_w, and C_f is the feedback capacitance of the front-end amplifier. As this capacitive TIA allows photocurrent to be integrated independent of the photodiode well capacity, unlike an active pixel sensor (APS) structure that uses intrinsic diode capacitance for integration, this approach is well suited for wide-DR current sensing.

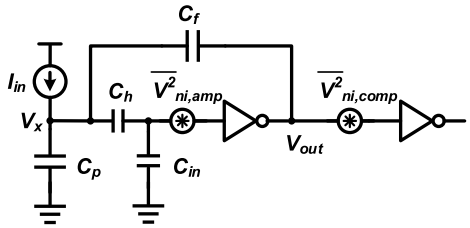


Fig. 5. Capacitive TIA followed by an inverter-based comparator, including relevant capacitors affecting transimpedance gain and noise sources.

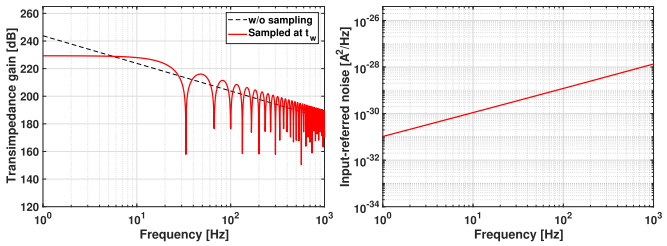


Fig. 6. (a) Simulated transimpedance gain of the CTIA. (b) Simulated noise spectral density for different output pulse rates.

Considering that for this dual-mode architecture (Fig. 2), low-light detection is performed using SPAD-mode operation, the PD-mode readout design constraints can be significantly relaxed for small i_{ph}. For this article, we employ an inverter-based architecture as shown in Fig. 4(b) to minimize circuit area for in-pixel integration. This architecture is similar to Fig. 4(a), where the front-end amplifier and comparator have been replaced with inverter-based amplifiers. The operation of the architecture is as follows.

The front-end inverter (I1) serves as a self-biased, single-ended amplifier where the operating point (V_{op}) is approximately half of supply voltage, determined by reset (RST) once per integration period. A feedback capacitor C_f and a hold capacitor C_h are precharged during reset, and the photodiode anode is shorted to ground by a switch. Due to the C_h, the anode voltage is held at ground, which minimizes leakage current through the reset switch and SPAD-mode circuit. RST is triggered once to begin integration and then forms the self-triggered reset signal during the specified integration window.

During integration, the anode voltage is held at ground by the capacitive negative feedback, which maintains a fixed reverse bias voltage across the photodiode regardless of variation in front-end inverter operating point, V_{op}, within each pixel. As photocurrent, i_{ph}, is integrated on C_f, the voltage at node A falls, as illustrated in the timing diagram of Fig. 4(b). When the voltage at A crosses the switching threshold of the second inverter, a fixed-width reset pulse is generated by a monostable delay block, J1, which is detailed in Section II-C.

This process repeats, forming a pulse-based output, where RST is self-triggered asynchronously. With larger i_{ph}, node A reaches the threshold more quickly, producing more reset pulses in a fixed time window and a corresponding increase in f_{out}. A skewed inverter, which uses a larger aspect ratio for NMOS than for PMOS, with decreased threshold voltage, V_{th}, is used for I2, followed by balanced inverters to drive the output node. This approach eliminates the need for a conventional continuous-time comparator, which would require a current bias circuit and a higher transistor count.

Relaxation of several key design requirements for the current-to-frequency converter is validated by the following analysis, which refers to the circuit model including noise sources illustrated in Fig. 5:

1) Signal Analysis for I-to-F Converter: Input current, I_{in}, is converted to a voltage, V_{out}, where the transimpedance gain $T_1(s)$ can be derived as

$$|T_1(s)| = \frac{1}{\omega[((C_p + C_f)(1 + C_{\text{in}}/C_h) + C_{\text{in}})/|A(s)| + C_f]} \approx \frac{1}{\omega C_f} \tag{2}$$

for large inverter gain, $|A(s)|$ with $C_f = 100$ fF, $C_h = 150$ fF, $C_{\text{in}} = 92$ fF, and $C_p = 100$ fF; trimmable C_f and fixed C_h are implemented as MIM capacitors. This can be further generalized for a sampled system considering asynchronous reset and integration for the entire time window, t_w, as

$$|T_w(s)| = \frac{1}{\omega C_f} \cdot |1 - e^{-t_{\text{int}} \cdot s}| \cdot \left| \frac{1 - e^{-t_w \cdot s}}{1 - e^{-t_{\text{int}} \cdot s}} \right| = \frac{1}{\omega C_f} \cdot |1 - e^{-t_w \cdot s}| \tag{3}$$

where t_{int} represents the duration between output pulses.

Fig. 6(a) plots this frequency response, where the low-frequency transimpedance gain is determined by t_w or f_{out}, and minimum resolvable photocurrent i_{min} is derived as

$$i_{\text{min}} \approx \frac{C_f \Delta V}{t_w}. \tag{4}$$

For this article, i_{min} is set as approximately 1.3 pA, where $\Delta V = V_{\text{op}} - V_{\text{th}}$ is 390 mV and integration time window t_w is 30 ms, which is considered to be sufficient to measure light intensity, where the SPAD-mode output starts to become nonlinear. A systematic gain error due to the finite dc gain of the amplifier, 43 dB, is 2.8%, which can be easily calibrated while not degrading linearity. In addition, signal bandwidth is determined by the integration time window, which is the sampling rate of the readout; for this article, it is 15 Hz.

2) Noise Analysis for I-to-F Converter: Output voltage noise of the current-to-frequency converter circuit is determined by input-referred noise of the front-end integrator, $\overline{V^2_{\text{ni,amp}}}$, and comparator noise, $\overline{V^2_{\text{ni,comp}}}$, as shown in Fig. 5. The noise spectral density of the amplifier output, $\overline{V^2_{\text{no}}}$, and input-referred noise current, $\overline{I^2_{\text{ni}}}$, during integration time t_w is calculated as

$$\overline{V^2_{\text{no}}} = \left(\overline{V^2_{\text{ni,amp}}} \cdot |A(s)|^2 + \overline{V^2_{\text{ni,comp}}}\right) \cdot |1 - e^{-t_w \cdot s}|^2 \tag{5}$$

$$\overline{I^2_{\text{ni}}} = \overline{V^2_{no}} \cdot \frac{1}{|T(s)|^2} = \left(\overline{V^2_{\text{ni,amp}}} \cdot |A(s)|^2 + \overline{V^2_{\text{ni,comp}}}\right) \cdot (\omega C_f)^2. \tag{6}$$

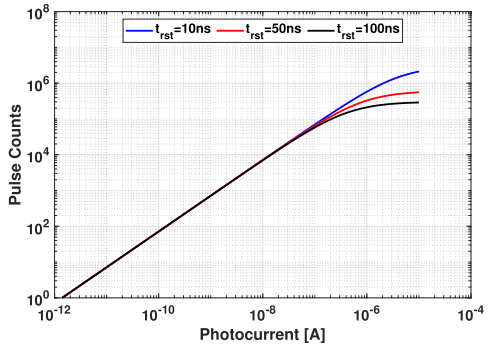


Fig. 7. Simulated pulse counts at different t_{rst} values with respect to input photocurrent.

From (5) and (6), simulated total input-referred noise spectral density is plotted in Fig. 6(b). For these simulations, input-referred voltage noise of the amplifier and comparator is provided by transistor-level noise simulation results. The resulting rms noise current over bandwidth is 3.4 fA_{rms}, which is smaller than minimum resolvable current i_{min}. Note that device noise is negligible compared with relaxed minimum required signal level, where the SPAD-mode operation is used for low-light detection.

3) Nonlinearity Due to Non-Zero Reset Pulse: A reset pulse is generated by the fixed-width pulse generator (J1) when the inverter output voltage C falls low, as shown in Fig. 4(b). This maintains reset for a fixed time, avoiding errors due to false comparisons, especially if voltage at node A fluctuates near the threshold voltage of the inverter (I2). Typically, a comparator with hysteresis is used for the reason, as illustrated in Fig. 4(a). Pulse generator J1 is a monostable delay block shared with SPAD-mode readout circuits (Section II-C); no additional circuits are needed for reset pulse generation.

Due to the finite reset pulsewidth accumulated over every pulse event, the resulting pulse count, $N = i_{in}/i_{min}$, can be determined by

$$i_{in} \cdot (t_w - N \cdot t_{rst}) = N \cdot C_f \cdot \Delta V$$
$$N = \frac{i_{in} t_w}{i_{in} t_{rst} + C_f \Delta V} \tag{7}$$

where the non-zero t_{rst} causes nonlinearity as plotted in Fig. 7, with input photocurrent ranging from 1 pA to 10 μA (t_w = 30 ms). For this article, maximum estimated pulse count N with t_{rst} of 50 ns is 553 510. Although smaller t_{rst} degrades linearity less, it requires the front-end amplifier to have larger bandwidth for faster reset.

The first inverter (I1) is sized to complete reset within the fixed width of the pulse, with a gain bandwidth of 110 MHz achieved at a dc bias current of 18 μA; diode-connected PMOS and NMOS between the rails determines the bias current when input and output are shorted. Moreover, switches are sized such that ON-resistance ($\approx$500 Ω) provides nearly ten times larger bandwidth (>1 GHz) than the amplifier bandwidth.

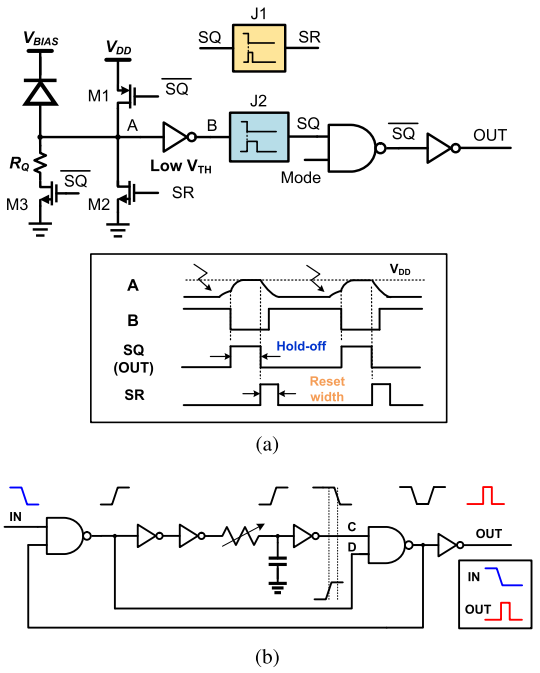


Fig. 8. (a) Mixed QRC with transient operation. (b) Monostable delay circuit for fixed-width pulse generators J1 and J2.

C. Quench and Reset Circuit for SPAD-Mode Readout

For the SPAD-mode operation of the photodiode (Fig. 2), a QRC is required to halt the current avalanche and reset the SPAD after each current pulse. For this article, as shown in Fig. 8(a), a mixed quench and active reset scheme was utilized, because it combines the advantages of purely passive and purely active quenching circuits, offering faster reset and well-defined dead time [37]. In addition, this implementation limits the total avalanche charge to at most equal to a fully passive approach [38].

The operation of the QRC is illustrated in Fig. 8(a): at idle, voltage at node A is low, inverter output B is high, quench and reset switches M1 and M2 are OFF, and M3 is ON to maintain the anode voltage at ground. After photon absorption, the diode avalanche current flows through a sense resistor, R_Q, and anode voltage increases until it reaches the threshold of the first skewed inverter, which uses a larger aspect ratio for NMOS than for PMOS; B is flipped, and active quenching begins. When $\overline{SQ}$ is low and SR is low, the anode is pulled to V_{DD} by M1, and M2 and M3 are turned OFF. Note that the active logic allows the node A voltage to be maintained below the threshold of the first inverter, which prevents any device breakdown in low-voltage CMOS readout circuits, including transmission gates routed to the anode. A monostable delay block (J2) generates a quench-on pulse at the falling edge of B, which is adjustable to control hold-off time. After quenching, a reset pulse, SR, is generated by a second monostable delay block (J1), allowing the photodiode to be recharged for the next avalanche current event.

The operation of the monostable delay blocks (J1 and J2) is illustrated in Fig. 8(b). An internal variable resistor and a capacitor cause a delayed transition, thereby allowing both A

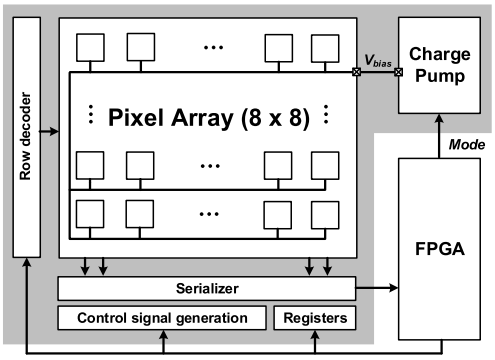


Fig. 9. Dual-mode pixel array architecture with fully parallel digital readout.

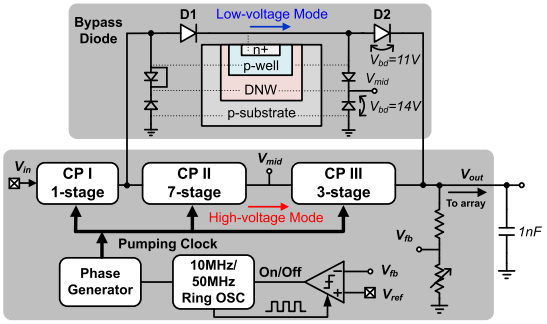
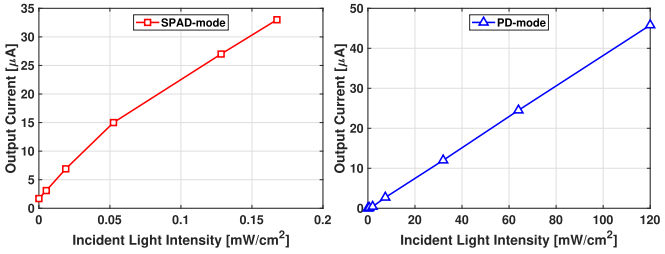


Fig. 10. On-chip high-voltage/low-voltage generation architecture.



(a) (b)

Fig. 11. (a) Measured charge-pump output current during SPAD-mode operation. (b) Measured charge-pump output current during PD-mode operation.

and B to remain high for the overlap duration, generating a one-shot pulse corresponding to the falling edge of the input.

For this article, the hold-off time and reset width are 50 and 50 ns, respectively. A single square output pulse is generated during a quench and reset cycle, corresponding to a single avalanche event. The finite dead time t_{dead} (=hold-off time + reset width) causes nonlinearity as the signal increases, similar to the PD-mode readout nonlinearity due to non-zero reset pulse in (7). The effect of signal-dependent gain error can be described by the temporal aperture ratio (TAR), written as

$$\text{TAR} = \frac{T_{\text{total}} - T_{\text{dead}}}{T_{\text{total}}} \tag{8}$$

$$T_{\text{dead}} = N \cdot t_{\text{dead}} \tag{9}$$

where N represents the total number of pulses for total measurement time T_{total} [39]. Estimated maximum N is 25 000 for $t_{\text{dead}} = 100$ ns, which is 10 Mcps. Of note, the dead time in this avalanche pulse detection circuit need not be as short as in other SPAD-based wide-DR imagers, as the higher illumination range (high photon count rate) is measured using PD-mode operation (i.e., hold-off time of 20 ns for maximum counting rate of 50 Mcps [40]).

III. Wide Dynamic Range Optical Sensor Array

A. High-Level Array Architecture

A dual-mode optical sensor array offering fully parallel readout was designed to demonstrate in-pixel measurements of both linear and single-photon avalanche diode (SPAD) operational modes (Fig. 9). This design validates scalability and modularity of the proposed pixel design, where only digital data flow circuits are required for extension to an array. Each pixel output comprises a 14-bit digital word containing PD-mode or SPAD-mode data, according to the operation mode. Data are generated simultaneously at all pixels and serialized by row for output. Serialized data for the entire array, as well as a frame sync signal, are routed to an external FPGA, which also provides row selection inputs using a data-ready signal. A shift register is used to set variable parameters, including integration time window, pulsewidths, and feedback capacitance.

Maximum output data rate is only required to be 360 kbps in total for 64 channels at a maximum frame rate of 400 Hz in SPAD-mode, which is transmitted as serialized data; this approach does not require high-order off-chip decimation filtering [6]. Diode bias voltage is supplied by a reconfigurable charge pump where mode is selected by the FPGA. By integrating the diode bias generator in the same IC, we can easily change the operational modes of the diode array and respective readout control quickly and simultaneously.

B. Dual-Mode HV–LV Diode Bias Generator

In order to generate both high-voltage (SPAD-mode) and low-voltage (PD-mode) diode biases required for wide-DR optical sensor biasing, a 1-or-N reconfigurable closed-loop charge pump was integrated in the same IC substrate. This dc–dc converter is suitable for efficient low-voltage (<5 V) and high-voltage (>10 V) step-up voltage conversion in a low-voltage CMOS process using a customized stage-bypass diode structure [41].

The architecture diagram of the dual-mode diode bias generator is shown in Fig. 10, which includes a reconfigurable charge pump and a closed-loop load regulation scheme. When biasing an optical sensor array in SPAD-mode, CP I–III are all clocked at 50 MHz, leading to reverse-biased diodes D1 and D2 with negligible reverse leakage current. The total number of stages (11) is optimized for fast recovery at the target output voltage (>10 V). When biasing an optical sensor array in PD-mode, only CP I is clocked at 10 MHz, which is accomplished by gating the clock for CP II and III. In this mode, D1 and D2 are forward biased to feed the output of CP I to the load. Each sub-charge-pump uses a four-phase, cross-coupled topology. The converter input voltage V_{IN} is fixed at 3.3V, and all transistors in sub-charge-pumps are 3.3-V thick-oxide

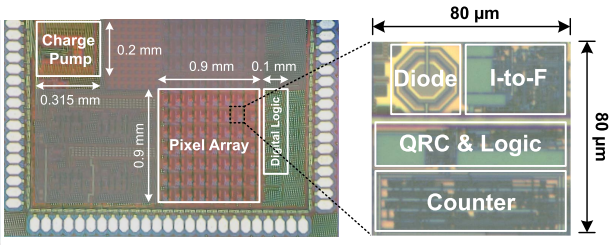


Fig. 12. Die photograph of optical sensor array with zoomed-in view of dual-mode pixel.

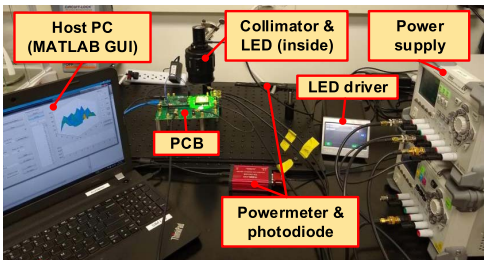


Fig. 13. Experimental measurement setup for optical characterization.

devices including deep-n-well NMOS in CP III whose bulk is connected to V_{MID} for supporting high voltage [42]. The output of charge pump is controlled by an ON/OFF closed-loop regulation scheme using a resistive divider and a comparator with a reference voltage V_{ref} to provide accurate diode bias voltage. The feedback control circuits are all implemented using a 1.8-V voltage supply. The charge pump can support 200 and 50 μA load current with maximum 34% and 56% efficiency at SPAD-mode and PD-mode, respectively [41]. The charge-pump output current for each operational mode with respect to incident light intensity is shown in Fig. 11; all load currents are within the regulated charge-pump output driving range without measurable voltage droop.

C. IC Fabrication

The 8 × 8 dual-mode optical sensor array was fabricated in a general purpose 0.18-μm CMOS process; a die photograph is shown in Fig. 12. Analog circuits, digital circuits, and I/O pads are supplied at 1.8 V. The complete array occupies 900 × 1000 μm^2, with a pixel array area of 900 × 900 μm^2 and digital logic area of 600 × 100 μm^2. Each pixel, including photodiode and readout circuits, is 80 × 80 μm^2, where a ratio of active area (53 μm^2) to total pixel area provides a fill-factor of approximately 0.8%. Lower fill factor is a tradeoff for in-pixel digitization to support increased frame rate, modularity, and a scalable, fully parallel architecture; for future applications, the large-area and fully parallel pixel is well pitch-matched to biosensor and biochip applications with arrayed independent optical detectors, and the signal-to-noise ratio (SNR) will be further improved with increasing fill factor. The reconfigurable HV–LV charge pump occupies a total area of 200 × 315 μm^2 and supplies bias voltages for both PD-mode and SPAD-mode operations.

IV. Verification and Measurement Results

A. Experimental Measurement Setup

The experimental measurement setup is shown in Fig. 13. Each singulated IC was wire-bonded to an 84-pin ceramic carrier. Control and digital interfacing is provided using a custom printed circuit board (PCB) with an on-board FPGA module (OpalKelly XEM6310) and socketed test IC. In these measurements, the FPGA is used for array data acquisition as well as for control shift register input generation. The FPGA also de-serializes the serial output data and transmits these to a host PC for analysis using a MATLAB interface.

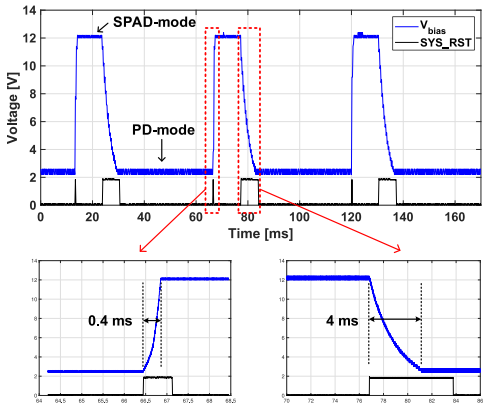


Fig. 14. Measured charge-pump voltage output transients for dual-mode operation switching from low (2.3 V) to high (12 V) voltage and high to low.

To perform optical measurements, a regulated green LED module (Thorlabs, λ = 565 nm) was used as a light source. A collimator provides uniform illumination across the IC surface. Light intensity is controlled by a regulated LED current driver, and an optical power meter (Thorlabs PM100USB) was used to measure illumination power at the IC plane. Measured light intensity ranged from 1.2 nW/cm^2 to 145 mW/cm^2 for these measurements, with the upper bound limited by the LED maximum allowable current. All optical measurements were conducted using a light-tight enclosure (data not shown).

B. Alternate-Frame Operation of the Dual-Mode Array

To enable extended optical DR, the optical sensor array is used alternately in PD-mode and SPAD-mode operations in each frame by switching the diode bias voltages (12 or 2.3 V) supplied by the reconfigurable charge pump, as shown in the measured on-chip bias voltages of Fig. 14 in dark conditions. Readout circuits are held idle by SYS_RST during diode bias transition and are activated after the bias voltage settles. Rising bias transition is pumped actively by the charge pump with a fast settling time (0.4 ms), whereas the falling transition takes longer (4 ms) due to passive discharge operation in conjunction with a large external load capacitor (1 nF).

C. Sensor Array Characterization

1) Measured Sensitivity and Linearity: Output pulse rate is plotted without baseline cancellation for varying illumination intensity in Fig. 15, where the flat region for each mode corresponds to dark signals. Each data point is acquired

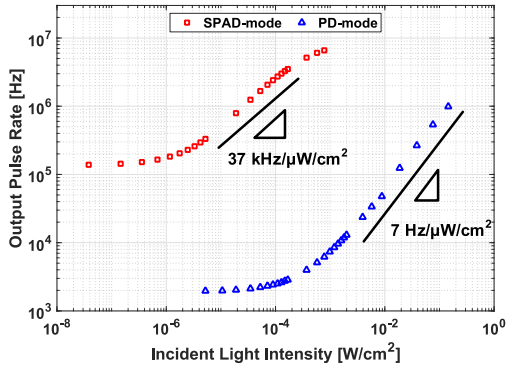


Fig. 15. Measured output pulse rate for varying incident light intensity in SPAD-mode and PD-mode.

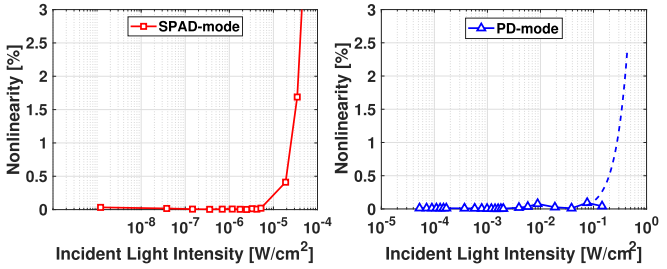
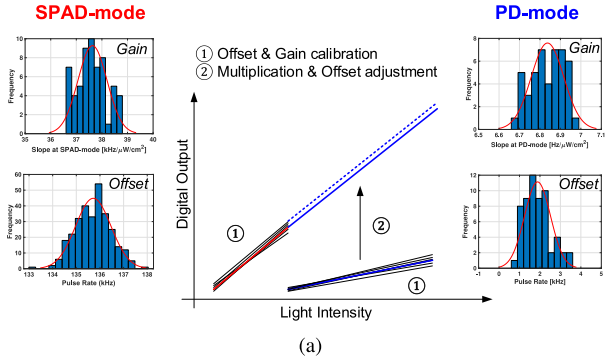


Fig. 16. (a) Measured nonlinearity for SPAD-mode. (b) Measured nonlinearity for PD-mode from stitching point to maximum illumination.



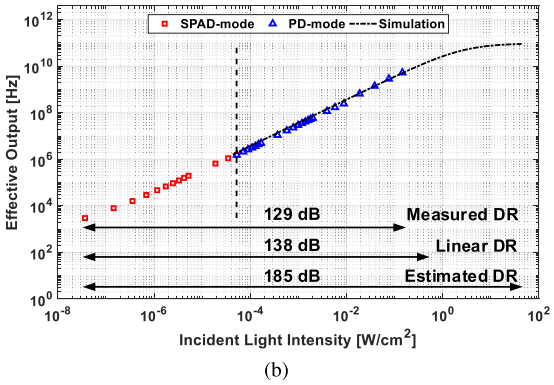


Fig. 17. (a) Illustration of calibration and gain adjustment process for the combined dual-mode data. (b) Optical DR with annotated regions for measured DR, estimated linear DR, and estimated saturated DR under sufficiently high illumination intensity.

with alternate-mode frames, where SPAD-mode measures at 400 Hz, decimated by 4 for an effective frame rate of 100 Hz, and PD-mode measures at a frame rate of 30 Hz; the combined dual-mode frame rate is 20 Hz, including bias change between the modes. Oversampling in SPAD-mode prevents counter-limited readout. The average of approximately 400 frames across the entire 8×8 array is plotted; three peak values have been excluded from the data set as noisy outlier or "stuck-on" pixels.

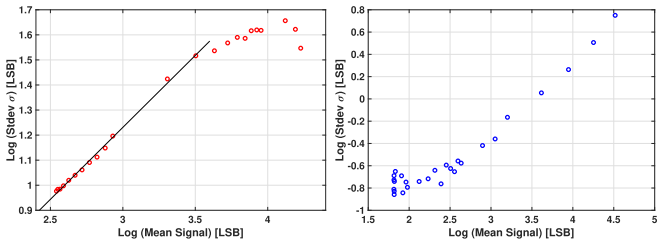
For SPAD-mode, an excess bias of 0.8 V ($V_{\text{bias}} = 12$ V) beyond the breakdown voltage (11.2 V) was applied to the diodes. SPAD hold-off time and reset width were set to 100 ns, which sets dead time. As seen in Fig. 15, the SPAD-mode operation provides increased sensitivity ($\approx$5400$\times$) compared with the PD-mode operation and improved resolution at low illumination, but its response saturates as illumination intensity increases.

For PD-mode, reverse-bias voltage was set at 2.3 V, well below the avalanche breakdown voltage. The PD-mode output is linear across a wide optical range, from 53 μW/cm^2 to the maximum measured light 145 mW/cm^2, where output resolution is set intentionally low in the PD-mode operation compared with the SPAD-mode operation, as low-level illumination is measured in SPAD-mode.

The operational mode switches from SPAD to PD for enhanced DR, and the stitching point is chosen to maintain linearity over the combined operational range. Nonlinearity with respect to illumination intensity is plotted in Fig. 16 as the deviation from measured data from the calculated linear best-fit line, normalized to the full-scale range [43]. For SPAD-mode, nonlinearity increases as the signal saturates with increasing illumination. Allowing for nonlinearity of up to 2 %, the stitching point is set at approximately 53 μW/cm^2. The PD-mode linearity is plotted in Fig. 16(b), beginning at the stitching point, calculated using the maximum saturated output signal from (7).

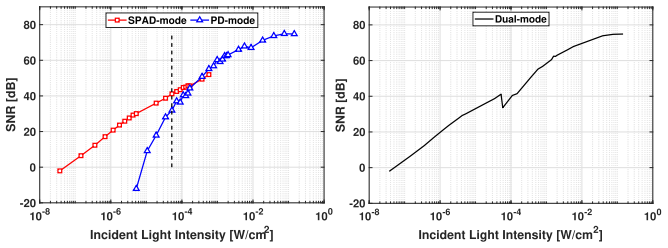
A continuous, wide-DR linear response is provided by a adjusting PD-mode effective pulse rate by the sensitivity ratio ($\approx$5400$\times$) and adjusting the offset, which is done off-chip in post-processing, yielding the dual-mode response shown in Fig. 17(b). To be specific, the per-pixel calibration is done for each mode using the mean offset and gain of the entire array, and then the whole PD-mode data are multiplied with their offset being adjusted to align each slope as illustrated in Fig. 17(a), where measured gain and offset distribution are shown as histogram plots. SPAD-mode is used in the low-illumination range (37 nW/cm^2*to*53 μW/cm^2), and PD-mode is used at higher illumination levels (53 μW/cm^2*to* 145 mW/cm^2).

2) Noise and Dynamic Range: Optical DR is defined as the ratio of maximum illumination that saturates the sensor—or less, depending on linearity requirements—to the optical power equivalent of the noise floor without illumination [21]. As the SPAD-mode operation is used for low-level illuminations, its noise level determines low-light detection limit. For the single-photon operation, the dark noise limit is determined by the DCR. DCR statistical variation in each measurement



(a) (b)

Fig. 18. (a) Measured PTC for SPAD-mode operation. (b) Measured PTC for PD-mode operation.



(a) (b)

Fig. 19. (a) Measured SNR plot in SPAD-mode and PD-mode operations. (b) Combined SNR plot for dual-mode operation validating monotonic increase over entire measurement range, except at the mode-switch point.

window determines the noise floor. A measured photon transfer curve (PTC) for the SPAD-mode operation is plotted in Fig. 18(a), which plots the relationship between standard deviation of noise and mean signal, both on log-scale; the slope of approximately 0.5 indicates that the SPAD-mode operation exhibits shot-noise-limited response until it starts saturating as light increases. This result shows that avalanche breakdown follows a Poisson distribution for both thermal and photon-triggered breakdown [20]; as such, the dark count variation σ is approximately equal to the square root of the dark count [44].

The SNR is plotted in Fig. 19(a) for both photodiode operation modes, where signal represents spatial mean of temporal average for each pixel across the entire array, and noise represents spatial mean of standard deviation of each pixel in time. The slope of PD-mode SNR gradually decreases as light increases and saturates in higher illumination due to readout nonlinearity, as described in (7), as well as shot-noise. The combined dual-mode SNR plot is shown in Fig. 19(b); an SNR dip occurs at the stitching point, which is typical for multi-mode or multi-exposure sensors [14], [45]. A maximum SNR of 75 dB is measured at maximum illumination intensity (145 mW/cm^2).

The minimum detectable optical signal is determined such that the SNR in SPAD-mode is equal to 1, which occurs at a measured illumination of 50 nW/cm^2 (λ = 565 nm). Note that DCR of the SPAD sensors for this article is higher than some reported CMOS-integrated SPADs, which limits the low-illumination measurable range; the proposed approach will yield even higher DR extension when used in conjunction with SPAD devices having low DCR and higher PDP, typically leveraging CIS processes [20], [25], [46].

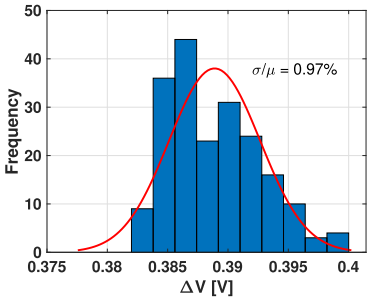


Fig. 20. Threshold ΔV variation from Monte Carlo simulation for PD-mode readout circuit.

The measured optical DR of the proposed dual-mode optical sensor array is 129 dB = ((145 mW/cm^2)/(50 nW/cm^2)), with the maximum tested incident light flux (145 mW/cm^2) limited by the LED source used for these measurements. The SPAD-mode operation covers the lower illumination range of 60 dB, and PD-mode covers 69 dB from the stitching point. Less than 2 % nonlinearity is estimated at an illumination intensity of 400 mW/cm^2 from (7) plotted as a dotted line in Fig. 16(b), for an expected linear DR of 138 dB. The simulated response also indicates sensor saturation at approximately 90 W/cm^2, for a maximum optical DR of 185 dB.

3) Nonuniformity Across the Sensor Array: Pixel nonuniformity is characterized as the dark fixed pattern noise (FPN) and the photo response non-uniformity (PRNU). Dual-mode dark FPN is determined by a ratio of pixel-to-pixel DCR variation in SPAD-mode to maximum signal in PD-mode, as the SPAD-mode operation is used in low-illumination, and maximum high-illumination signal is measured using the PD-mode operation. PRNU represents pixel-to-pixel sensitivity variation to mean value for each mode before gain calibration. Dual-mode dark FPN is negligible due to large maximum signal; the pixel-to-pixel standard deviation of DCR is 3.7 kHz and maximum measured signal is 5.3 GHz (after gain calibration). FPN is 0.06% and 0.005% for SPAD-mode and PD-mode, respectively, where maximum signal calculated is estimated using saturation signal values provided by (7) and (9); the maximum measured signal for PD-mode is not saturated and still in a linear region based on Fig. 17(b). Measured PRNU is 1.7% for SPAD-mode and 1.2% for PD-mode, respectively.

Gain variation for SPAD-mode may primarily result from variable PDP, whereas for PD-mode, it is mostly attributed to the readout circuit. Since the voltage difference ΔV in (4) is determined by the threshold voltage of the first inverter (I1) and the low-V_{th} inverter (I2) used together as a comparator (Fig. 4(b)), mismatch will affect the gain. Fig. 20 shows the Monte Carlo simulation result representing intra-die variation due to mismatch without process variation, where it is shown that the PD-mode PRNU, 1.2%, primarily stems from the ΔV variation.

4) Comparison With SPAD or PD-Mode Wide Dynamic Range Optical Sensors: A summary of measured results is shown alongside prior related work in Table II. In [33], a similar current-to-frequency converter scheme is used for the PD-mode readout, where low-illumination detection is

TABLE II
PERFORMANCE COMPARISON

Reference	[33]	[6]	[20]	[25]	**This Work**
Process	180 nm CMOS	130 nm	40 nm FSI	110 m BSI	**180 nm CMOS**
Array Size	28 x 28	32 x 32	96 x 40	1280 x 720	**8 x 8**
Pixel Size	23 μm	100 μm	8.25 μm^a	3.8 μm	**80 μm**
Fill-factor	25 %	25 %	26 %^{a}	-	**0.8 %**
Diode Operation	PD	PD	SPAD	APD/PD	**SPAD/PD**
Readout Architecture	In-pixel	In-pixel	In-pixel	APS column readout	**In-pixel**
Frame Rate (FPS)	30	1	240^b	30 (APD) 30 (PD)	**100 (SPAD)** **30 (PD)**
Optical Dynamic Range (dB)	110	116	99.6^b @OSR=256	1 photon (APD) 60 (PD)	**129**
Photons Detection Range (photons/cm^2·s)^c	10^{13}-10^{17}	10^{10}-10^{15}	-	10^{8}-10^{13}	$\mathbf{10^{11}}$**-**$\mathbf{10^{18}}$
Dark Signal	-	20 fA	150 cps	0.1 cps	**135 kcps**
Max. SNR (dB)	$<60^d$	$<80^e$	52	-	**75**
Power Consumption per pixel ^{f}	0.25 μW	115 μW	-	-	**36 μW (SPAD)** **40 μW (PD)**
Interface Data Rate per pixel	-	100 kbps	46 kbps	-	**5.6 kbps (SPAD)** **560 bps (PD)**
Integrated HV-LV Bias	-	-	N	N	**Y**

^{a} Readout circuits are separate, and the fill-factor was calculated as the ratio of imaging array area to whole chip area.
^{b} Estimated from summary table for a 1M-pixel HDR QIS reported in the reference.
^{c} Converted from reported lux or intensity (W/cm^2·s) to photon flux, or estimated from values in the reference if optical sensing range is not explicitly provided.
^{d} Estimated from ADC resolution; ^{e} estimated from a measured SNR plot; ^{f} total power including core and I/O power normalized to number of channels.

limited compared with using the SPAD-mode operation for low-light extension. In [6], a small-area oversampling ADC provides in-pixel photodiode readout at the cost of increased per-pixel power consumption and requires off-chip decimation as implemented, sending oversampled data off chip; our proposed current-to-frequency approach includes an in-pixel counter, providing parallel digital output without off-chip post-processing.

Prior demonstrations have used the SPAD-mode [20] and APD-mode [25] operations to increase both low-light sensitivity and DR, where SPAD-only operation increases DR but degrades SNR, due in part to multi-exposure techniques. For these approaches, an increasing oversampling ratio needed to support higher illumination levels may also require exceedingly high data rates. The APD-mode operation was used without QRC in the hybrid APD/PD-mode approach, limiting detection to single-photon binary readout in this mode [25].

The large pixel size and comparatively low fill-factor for the presented approach, as compared with prior wide DR imager and optical sensor approaches, are acceptable for targeted biosenor applications, where 80–100-μm pitch-matching is typically used [6], [29]. Future effort to scale down the pixel size and increase the fill-factor could include additional device sharing between PD-mode and SPAD-mode readout circuits, optimized in-pixel counter layout, and improved guard ring structures to enhance intrinsic photodiode fill-factor.

V. CONCLUSION

In this article, we demonstrate a wide-DR CMOS optical sensor array by combining the single-photon avalanche operation and continuous photocurrent measurement in a single, digital-ouput pixel. The approach demonstrates high linearity and SNR over a broad optical illumination range. An in-pixel pulse-based readout architecture is presented to support the dual-mode operation of a photodiode in area-efficient manner; a current-to-frequency converter measures continuous photocurrent, and a QRC processes SPAD output pulses; in both the modes, pulses are accumulated locally using an in-pixel digital counter.

The proposed in-pixel dual-mode SPAD/PD approach for optical sensor arrays enhances DR, increases the sample rate compared with PD-mode-only optical sensors, and operates from very low light to very bright light illumination conditions. As each pixel provides standalone continuously sampled data, this modular approach can be used to implement 1-D and 2-D optical sensor arrays or used to provide individual wide DR optical sensors to multi-sensor ICs. We also note that the prototype IC for this article was fabricated in an unmodified, general purpose CMOS process. In a modified or CIS-specific process with low-DCR SPADs, noise floor, overall DR, and SNR can be expected to further improve using the proposed approach.

In addition, this article includes the on-chip integration of a reconfigurable, closed-loop charge pump for dual-mode (HV/LV) photodiode biasing, including high-voltage generation in a general purpose, low-voltage CMOS process. In practice, the array can operate using a closed-loop auto-ranging control scheme and the switching operational modes automatically when the PD-mode output is lower than a set threshold or the SPAD-mode output enters a nonlinear or saturated region. Alternatively, a sum of data from the two modes can be used to reconstruct wide DR images (bright and

dark images), as is done for multi-mode and multi-exposure image reconstruction [14], [45].

The proposed pixel design was scaled to an 8×8 dual-mode optical sensor array and integrated alongside. The architecture was fabricated in a general purpose 0.18-μm CMOS process, and measured electrical and optical characterizations demonstrate linear optical DR of 129 dB at a dual-mode operating frame rate of 20 Hz. This approach represents the first reported optical sensor array architecture supporting both the linear and single-photon photodiode operations at the pixel level, which can be applied for a variety of wide-SR optical sensing applications.

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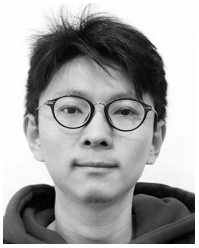

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