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Ultra-wide bandgap AlGaN metal oxide semiconductor heterostructure field effect transistors with high-*k* ALD ZrO_2 dielectric

Shahab Mollah[1], Mikhail Gaevski[1], MVS Chandrashekhar[1], Xuhong Hu[1], Virginia Wheeler[2], Kamal Hussain[1], Abdullah Mamun[1], Richard Floyd[1], Iftikhar Ahmad[1], Grigory Simin[1], Charles Eddy[2] and Asif Khan[1]

[1] Department of Electrical Engineering, University of South Carolina, Columbia, SC 29208, United States of America
[2] Naval Research Laboratory, Washington DC, United States of America

E-mail: mmollah@email.sc.edu

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Abstract

We report on $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ metal oxide semiconductor heterojunction field-effect transistor (MOSHFET) with high-*k* ZrO_2 gate-dielectric deposited using atomic layer deposition process. As extracted from frequency dependent capacitance–voltage (*CV*) characteristics, the oxide gates resulted in an interfacial state trap density of $\sim 2 \times 10^{12}$ cm^{-2}. A comparative study, on the same material, shows the gate-leakage current of the ZrO_2 MOSHFETs to be lower by five orders; their ON/OFF current ratio ($\sim 10^7$) to be higher by about four orders and their threshold voltage to decrease (less negative) by 3.5 V with respect to the Schottky gate devices.

Keywords: AlGaN HFET, AlGaN MOSHFET, high Al composition, insulating gate, atomic layer deposition, threshold voltage, fixed interface charges

(Some figures may appear in colour only in the online journal)

1. Introduction

Due to the higher thermal conductivity and breakdown field, the Baliga figure of merit of ultra-wide bandgap (UWBG) $Al_xGa_{1-x}N$ ($x > 0.5$) channel devices is higher than those with GaN and SiC channels [1–3]. They have been shown to have excellent radiation hardness [4] with the cutoff wavelengths in the solar-blind spectral region. UWBG III-Nitride semiconductors are thus promising materials for compact next-generation power electronics [5–10], solar-blind photodetection [11, 12] and nuclear reactor controls requiring radiation hardness [13].

The research on UWBG transistors is currently focused on several different type of devices, such as high electron mobility transistors (HEMTs), insulating gate HEMTs (also known as MOS-HEMTs or metal oxide semiconductor heterojunction field-effect transistor (MOSHFETs)), vertical MOSHFETs, CAVET devices etc [5]. Among those, HEMTs and MOSHFETs are of particular interest due to simple epilayer structure, excellent defect screening by high-density 2DEG and broad range of potential applications.

We have recently reported on $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ MOSHFETs with SiO_2 gate-oxide that was deposited using a plasma enhanced chemical vapor deposition (PECVD) process [14]. These devices had record high drain currents of 0.6 A mm^{-1}. However, an oxide thickness greater than 100 Å was required for a factor of 10^3 reduction in the gate-current. This in turn increased (more negative) the threshold voltage by about 2 V. Our past work with GaN channel MOSHFETs established that use of high-*k* gate-oxides mitigates this problem giving a very low gate-leakage current without a substantial increase in the threshold voltage [15]. However, high-*k* dielectrics have never been used in UWBG MOSHFETs with high-Al content barrier. The motivation behind the current work is to study the reduction of the gate-leakage current and change in the threshold voltage in UWBG MOSHFET with atomic layer deposition (ALD) high-*k* dielectrics.

2. Experimental

The device epilayer structure shown in figures 1(a), (b) was deposited on a 3 μm thick AlN/sapphire templates using metal-organic-chemical-vapor deposition process. Details of the growth procedure are reported elsewhere [16]. The off axis (102) x-ray peak line width for the AlN buffer layers of our templates was measured to be 330 arcsecs, which based on our past calibrations, translates to an overall defect-density $\sim(1-3)\times10^{8}\,\mathrm{cm}^{-2}$. The channel $Al_{0.40}Ga_{0.60}N$ and the barrier n-$Al_{0.65}Ga_{0.35}N$ layers for our structures were respectively 0.5 μm and 300 Å thick and only the barrier layer was silicon doped. As measured from the $1/C^2$ versus V plot, the barrier layer carrier concentration due to Si-doping was approximately $4\times10^{18}\,\mathrm{cm}^{-3}$. As measured by the Eddy current method, the sheet resistance (R_{sh}) value for our epilayer structure was ~1900 Ω/□.

The device source/drain ohmic contact metal stack Zr/Al/Mo/Au (150/1000/400/300 Å) [14] were evaporated and annealed for 30 s at 950 °C under N_2 using rapid thermal annealing. The devices were mesa-isolated with Cl_2-based inductively coupled plasma reactive ion-etching (ICP-RIE). We achieved linear source–drain ohmic-contacts with a contact resistance as low as 1.64 Ω mm which gives an equivalent ohmic specific contact resistivity of $\sim1.4\times10^{-5}\,\Omega\,\mathrm{cm}^2$. The gate-metal consisted of Ni/Au (1000 Å/2000Å). In addition to devices with gate-length 1.8 μm, gated transmission lined model test structures with gate-lengths ranging from 10 to 100 μm were also fabricated.

For this study, two sets of devices with identical geometry were fabricated on the same wafer. These consisted of devices with Schottky gates and with ZrO_2 oxide under the gate metals. The thickness of the ALD gate-oxide was 10 nm. The ZrO_2 film was deposited using thermal ALD process at 200 °C, with tri-methylaluminum (TMA), tetrakis (dimethylamido) zirconium (IV) (TDMAZ) and deionized water as the precursors. The TDMAZ precursor was also heated to 75 °C in order to achieve a linear growth rate of 0.7 Å/cycle. The deposition was initiated with 15 water pulses prior to the typical AB pulsing sequence to deposit the gate dielectric to ensure saturation of hydroxyl groups at the AlGaN surface required for conformal ALD nucleation [17–19]. The thickness of the ZrO2 films was obtained using witness samples grown on Si substrates in the same run, giving thickness 10 nm, with an index of refraction 2.13 from ellipsometry, very close to the ideal value of 2.15 expected for ZrO_2 [20, 21]. In previous studies by the co-authors' group (e.g. Shahin *et al* [19], the thickness of ZrO_2 on Si witness samples as measured by ellipsometry has identical thickness to the electrical thickness of ZrO_2 deposited on GaN in the same run using identical deposition conditions. The stoichiometry of the films was confirmed by XPS (figures 2(a), (b)). Neither carbon, nor nitrogen were observed, indicating complete ligand exchange during ALD, underscoring the high purity of the films. This is consistent with the close to ideal index of 2.13 measured by ellipsometry. The relative intensities of the Zr3d and O1s core levels (figures 2(a), (b)) are also consistent with

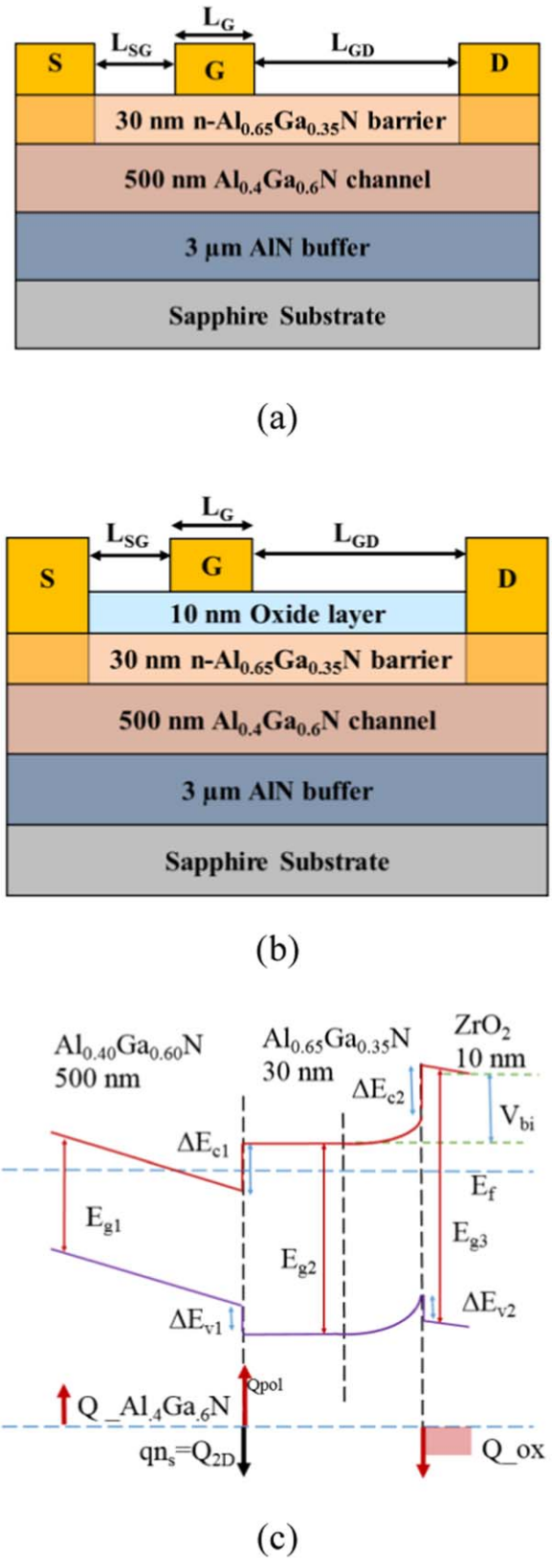

Figure 1. The device structure of the HFET (a) and MOSHFET (b). (c) Band diagram of ZrO_2 MOS-HFET, $E_{g1} = 4.52$ eV, $E_{g2} = 5.22$ eV, $E_{g3} = 6$ eV, $\Delta E_{v1} = 0.21$ eV, $\Delta E_{c1} = 0.49$ eV, $\Delta E_{v2} = 0.234$ eV, $\Delta E_{c2} = 0.546$ eV, $V_{bi} = 2.7$ V and Q_ox $= -3.1\times10^{13}$ q C cm^{-2}.

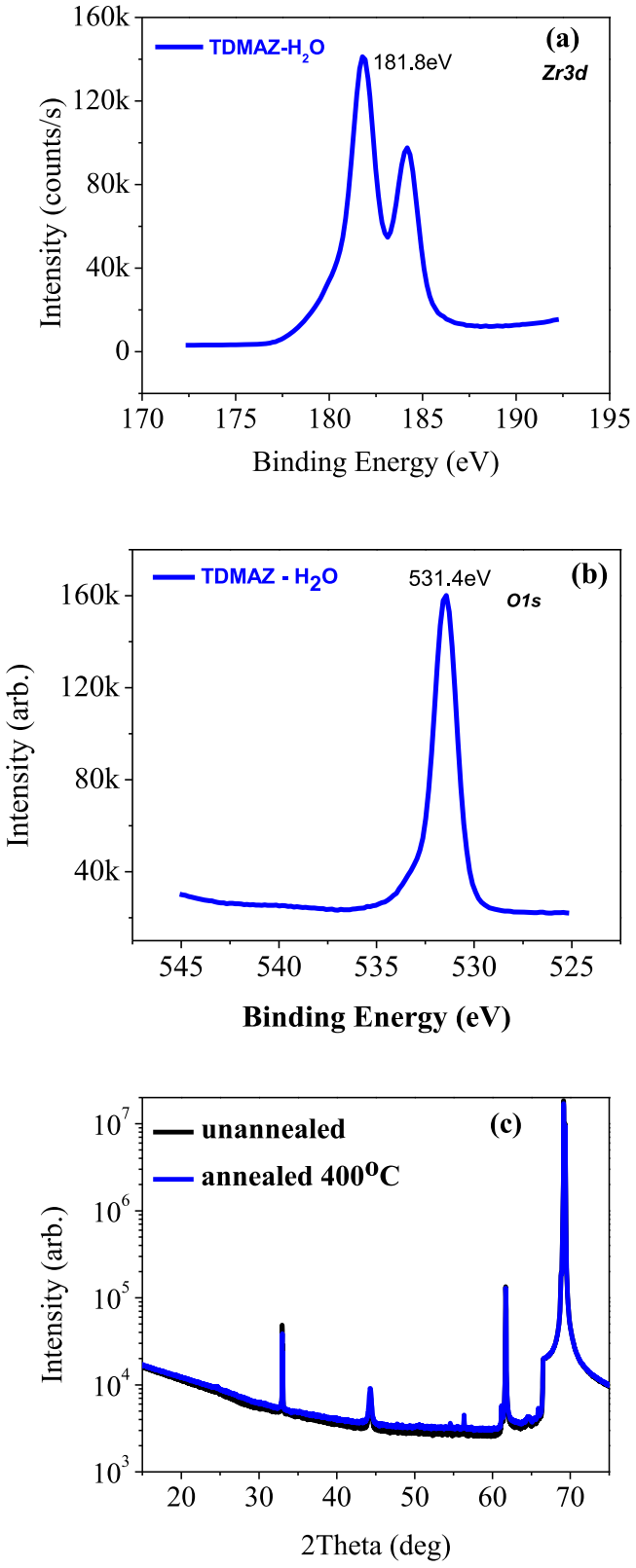

Figure 2. (a) The 3d core level XPS spectra (b) O 1 s photoelectron spectra of ZrO_2 dielectric (c) XRD of ZrO_2 dielectric film.

stoichiometric ZrO_2 [22]. XRD showed no sharp peaks, indicative of highly amorphous films. This amorphous nature persisted until 400 °C, at which point no sharp peaks were seen.

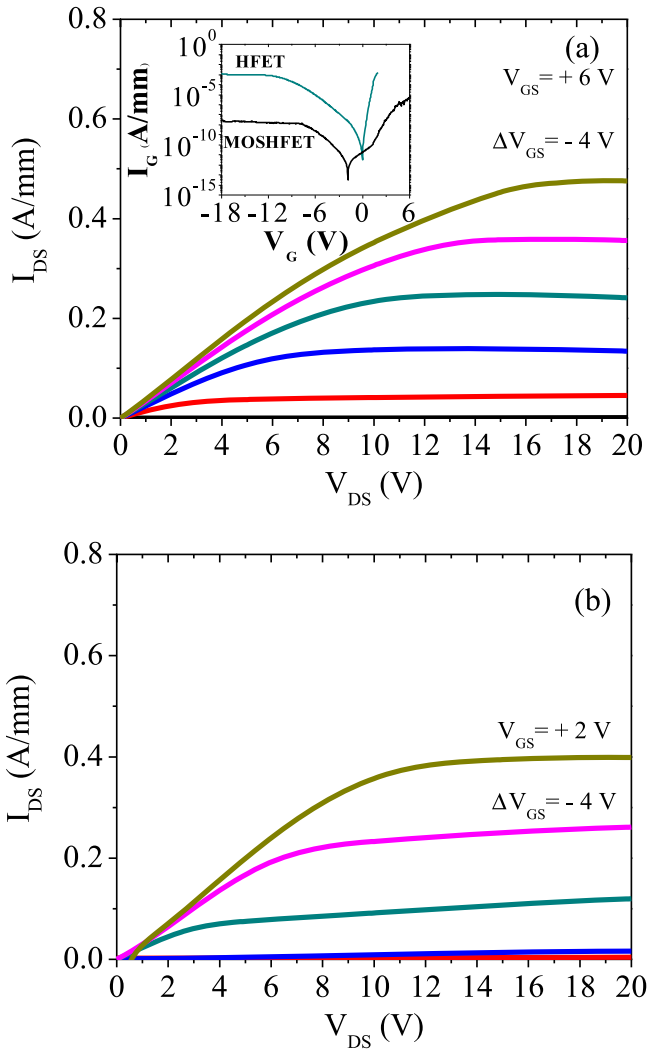

Figure 3. I_{DS} versus V_{DS} for $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ (a) ZrO_2 MOSHFET and (b) HFET, $L_{SD} = 6\ \mu m$, $L_G = 1.8\ \mu m$, $L_{GS} = 1.2\ \mu m$ and $L_{GD} = 3\ \mu m$. (a) Inset shows the gate leakage characteristics of HFET and MOSHFET.

The transfer (I_{DS} versus V_G) and the output I–V characteristics were measured using a parameter analyzer and the capacitance voltage (C–V) measurements were performed using a HP 4284A Precision LCR Meter.

3. Results and discussion

Figure 3(a) shows the output characteristics of the ZrO_2 MOSHFET, with the gate length $L_G = 1.8\ \mu m$, gate–source and gate–drain spacing $L_{SG} = 1.2\ \mu m$ and $L_{GD} = 3\ \mu m$ respectively. Clear saturation is observed, with peak currents $\sim 0.5\ A\ mm^{-1}$ at $V_G = 6\ V$, $V_D = 20\ V$. For the HFET (no oxide under gate i.e. Schottky gate) the saturation current was $\sim 0.4\ A\ mm^{-1}$ ($V_G = 2\ V$) which is shown in figure 3(b), and a channel electron mobility $>400\ cm^2\ V^{-1}\ s^{-1}$ was estimated by accounting for access region and contact resistances. This procedure is outlined in a previous report [14]. The I_G–V_G curves in the inset of figure 2 show that the use of insulating

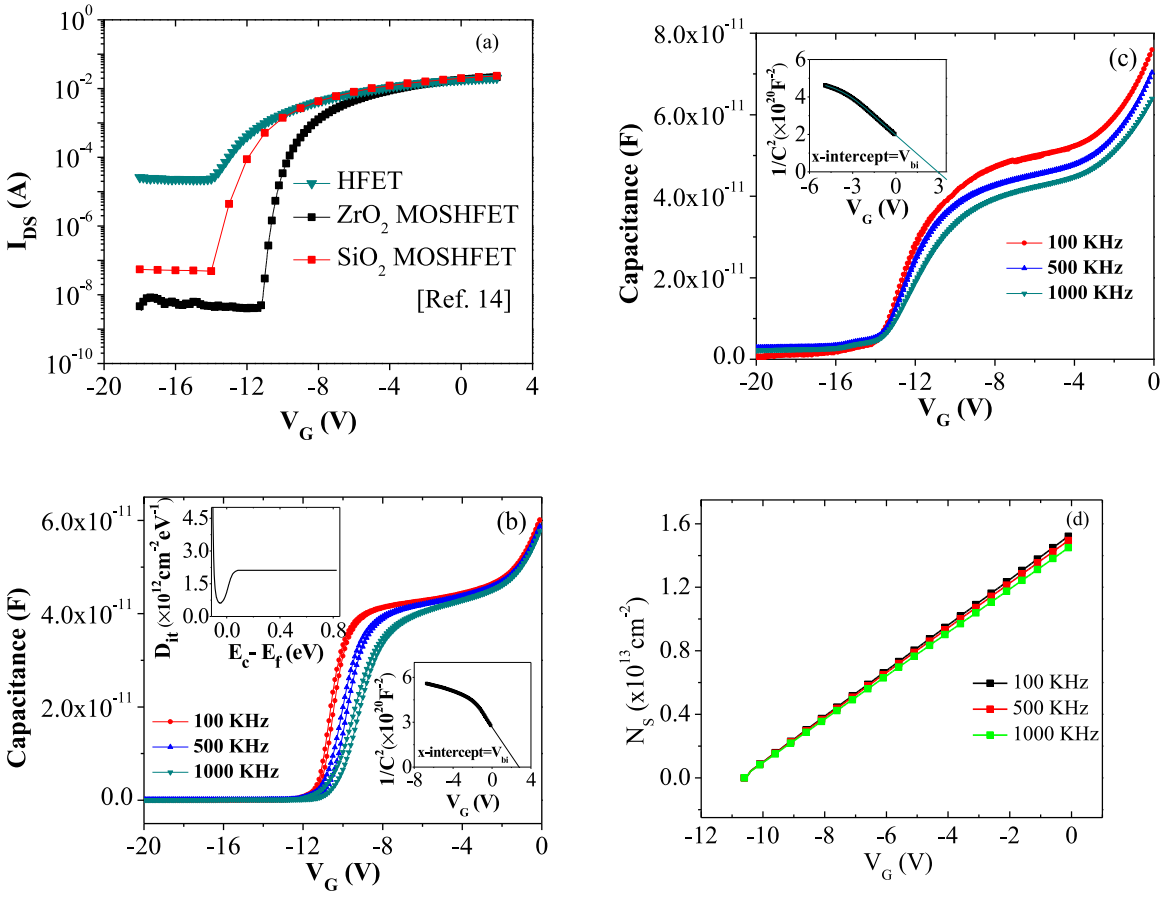

Figure 4. (a): Transfer characteristics HFET and MOSHFET; $L_{SG} = L_{GD} = 10\ \mu$m and $L_G = 10\ \mu$m. (b) MOSHFET *CV* characteristics. Upper inset shows the extracted distribution of traps with $E_c - E_f$ from the *CV* measurements, lower inset shows the $1/C^2$ versus *V* plot. (c) HFET *C–V* characteristics. Inset shows the $1/C^2$ versus *V* plot. (d) 2DEG charge density (N_s (V_G)) of ZrO_2 MOSHFET.

gate with ALD oxide reduces the gate-leakage current by 5 orders of magnitude.

The transfer characteristics of figure 4(a) were measured using 10 μm long gate MOSHFET. This was done to ensure that in the subthreshold regime the gate leakage current is dominated by bulk rather than the surface leakage. The transfer curves show an ON/OFF ratio of $\sim 10^3$ for the HFET which increases to $\sim 6 \times 10^6$ for the MOSHFET, while in our previously reported PECVD SiO_2 MOSHFET [14] it was $\sim 10^6$. This improvement is primarily from the reduction in the gate leakage current by $\sim$5 orders of magnitude compared to HFET, where the gate leakage reduction was $\sim$4 orders of magnitude in SiO_2 MOSHFET. Using data of figure 4(a), the values of threshold voltage V_{th} were obtained as V_G voltages at which the drain current decreases to 30 μA or 0.1 mA mm^{-1}.

The slope in transfer curves shown in figure 4(a) represents the rate of transition from on- into off-state (in a logarithmic scale). The peak drain currents (on-state currents) are similar for HFET and MOSHFET, however, the off-state current in MOSHFET is much lower because in HFET the gate leakage masks the actual subthreshold swing of the device. Besides, MOSHFET with ZrO_2 gate dielectric has more positive threshold voltage compared to HFET. These two factors determine much steeper slope of the MOSHFET transfer curves in figure 4(a).

The transfer characteristics of figure 4(a) show a positive V_{th} shift by $\sim$3.5 V in ZrO_2 MOSHFET as compared to the HFET. This is contrary to what was observed for the PECVD SiO_2 MOSHFETs [14, 23], where a reduction of gate-leakage current is accompanied by a more negative V_{th} [15]. Positive threshold voltage shift is an important effect that may help creating normally-off (enhancement mode) MOSHFETs which are critically important for use in power electronics applications. The V_{th} shift can be caused by a negative charge in the oxide or the oxide/barrier interface or both. Oxide and interfacial charges also play an important role in switching and high-frequency performance of wide bandgap MOSHFETs [24]. To determine these charges in the fabricated ALD ZrO_2 MOSHFETs, a comprehensive study of their frequency-dependent *C–V* measurements was conducted as described below.

For the study, we used devices with gate-length $L_G = 100\ \mu$m, and gate-width $W = 200\ \mu$m to test the *C–V* characteristics. Figure 4(b) shows frequency dependent *C–V* characteristics for the ZrO_2 MOSHFET. The V_{th} value here is consistent with that measured from the transfer characteristics of figure 4(a). At $V_G = 0$, the depletion only extends partially into the barrier layer, and does not reach the 2DEG, simplifying the analysis. Because of the high doping in the barrier

layer, it is possible to clearly distinguish three regimes seen in all devices:

(i) Depletion through barrier layer $-2\ \text{V} < V_G < 0\ \text{V}$ with $1/C^2$ dependence showing constant doping
(ii) 2D electron gas at barrier/channel interface $\approx -8\ \text{V} < V_G < -2\ \text{V}$
(iii) Pinch-off, with depletion extending into channel epitaxial layer $V_G \ll -8\ \text{V}$

The boundary between regime (i) and (ii) represents the voltage at which the 2DEG is being depleted, from which the capacitance of the gate at the 2DEG is measured, C_{2D}, which is true regardless of whether an oxide is present. Given this value of C_{2D}, the V_{th} measured in figure 4(a) can be expressed as:

$$V_{th} = -\frac{Q_{2D}}{C_{2D}} - \frac{qN_d}{2\varepsilon_s}(t_b^2 - x_d^2), \tag{1}$$

where t_b is the barrier layer thickness, x_d is the depletion region width in the $Al_{0.65}Ga_{0.35}N$ barrier layer (figure 1). Q_{2D} is the 2DEG sheet charge density. The first term in the right hand side of equation (1) represents the voltage required to deplete the 2DEG. The sheet charge density Q_{2D} is obtained by integrating the area under the C–V curve in figure 4(b), giving a V_G dependent sheet carrier concentration (N_S) in figure 4(d). Since all voltages are referenced to 0 V, the N_S value at $V_G = 0\ \text{V}$ gives the $Q_{2D} = qN_S$. The capacitance of the 2DEG was measured from C–V at the point where the C–V characteristic begins to flatten out ($\sim$47 pF for an area of $2 \times 10^{-4}\ \text{cm}^2$). Thus, the first term is -8 V. The second part represents the voltage required to deplete the doped barrier. This term is based on standard expression for Schottky junction depletion widths. The calculated value for the second part is -2.5 V based on the 0-bias capacitance value for the MOSHFET, and the measured barrier thickness by C–V (figure 4(c)) from the HFET without the ZrO_2. So the calculated threshold voltage is -10.5 V which is very close to the value -10.7 V determined from the I_d–V_g curve (figure 4(a)). From the linear $1/C^2$ characteristic in regime (i), the donor concentration in the barrier layer, N_d is obtained. The value of N_d for MOSHFET was $\sim 4.2 \times 10^{18}\ \text{cm}^{-3}$, whereas for the HFET, this was significantly higher at $6.8 \times 10^{18}\ \text{cm}^{-3}$. We attribute this change to the *in situ* pre-ALD surface preparation. From the boundary between regimes (i) and (ii) for the HFET, where the 2DEG is located at the barrier/channel interface, the barrier thickness $t_b = \varepsilon_S/C_{2D} = 30$ nm is obtained.

The gate capacitance in ZrO_2 MOSHFET is a series combination of the oxide capacitance and the barrier capacitance at the 2DEG, where the C–V characteristic begins to flatten out:

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_b}$$

C_G is total gate capacitance of MOSHFET 47 pF at 100 KHz from figure 4(b). C_b is barrier capacitance which is obtained from the HFET C–V characteristics without the ZrO_2 (53 pF at 100 KHz figure 4(c)) Thus, the oxide capacitance normalized to the area $2 \times 10^{-4}\ \text{cm}^2$ is obtained. Given the 10 nm thickness, as measured by ellipsometry in the experimental section, the dielectric constant is extracted from $C_{ox} = \varepsilon_r \varepsilon_0 / t_{ox}$ to be $\varepsilon_r = 23$, which is within the experimental range of 18–25 [15, 25, 26]. This relatively high value is consistent with the close to ideal index of 2.13 measured by ellipsometry. This is expected due to the lack of C and N contaminants by XPS, an advantage of the TDMAZ precursor [19].

Figure 4(d) shows the 2DEG charge density as a function of gate voltage. In the on- state the device has a sheet charge density of $\sim 1.53 \times 10^{13}\ \text{cm}^{-2}$.

The built-in voltage V_{bi} (defined in figure 1(c) band diagram), measured from the $1/C^2$ x-intercept in figure 3(a) can be expressed in terms of x_d as follows [27]:

$$V_{bi} = \frac{qN_d x_d^2}{2\epsilon_s} + E_{ox} t_{ox}. \tag{2}$$

The barrier height for MOSHFET and HFET are 2.7 eV and 3 eV respectively (see figures 4(b) and (c) inset). For the HFET, $t_{ox} = 0$, so that from the measured N_d and V_{bi}, x_d is extracted to be 20 nm, in agreement with that extracted from the gate capacitance at $V_G = 0\ \text{V}$ i.e. $C(0)$, which is $x_d = \varepsilon_s/C(0) = 24$ nm, showing that our formalism here is self-consistent. For the MOSHFET, E_{ox} is determined from Gauss's law at the oxide/barrier interface, where Q_{ox} is the fixed sheet charge density at this interface:

$$\epsilon_{ox} E_{ox} - \epsilon_s E_s = Q_{ox} = \epsilon_{ox} E_{ox} - \epsilon_s \left(\frac{qN_d x_d}{\epsilon_s} \right). \tag{3}$$

Solving for E_{ox} in terms of Q_{ox}, we can rewrite V_{bi} as:

$$V_{bi} = \frac{qN_d x_d^2}{2\epsilon_s} + \frac{qN_d x_d}{\epsilon_{ox}} t_{ox} + \frac{Q_{ox}}{\epsilon_{ox}} t_{ox}, \tag{4}$$

where the HFET can be described by setting $t_{ox} = 0$. x_d is deduced from the fact that the oxide capacitance, $C_{ox} = \epsilon_{ox}/t_{ox}$ and the depletion capacitance in the barrier, ϵ_s/x_d are in series. From the measured 0 bias capacitance $C(0)$, $x_d = (C_{ox}\epsilon_s - C(0)\epsilon_s)/C(0)C_{ox}$. Inserting this x_d into the previous equation, we have an equation with a single unknown remaining, namely Q_{ox}, in terms of the measured V_{bi}, N_d, and the known oxide parameters. The extracted value of Q_{ox} is $-3.1 \times 10^{13}\ \text{q C cm}^{-2}$. Negative value of Q_{ox} helps depleting the 2DEG thus making V_{th} more positive. Further optimization of barrier thickness and doping as well as of oxide film may enable realization of enhancement mode UWBG AlGaN devices as was the case for GaN channel HEMTs [28–33].

From the difference in the high (C_{HF}) and the low frequency (C_{LF}) capacitance versus voltage (C–V) characteristics, the density of interface states, D_{it} can be obtained. Since the barrier is doped and relatively thick $\sim$30 nm, the surface oxide charges, Q_{ox} do not significantly impact trapping at the barrier/channel interface. At low frequencies, slow traps have sufficient time to recharge and hence contribute to the measured capacitance, whereas at high frequencies they do not, resulting in lower measured capacitance. Figure 4(b) shows this dispersion for the MOSHFET. From this

difference, at a given, V_G [34]

$$D_{it}(V_G) = \frac{C_{ox}}{q}\left(\frac{C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{HF}}{C_{ox} - C_{HF}}\right). \quad (5)$$

To relate the gate voltage V_G to the Fermi level position with respect to the conduction band in the channel, E_c, we note that the 2D density of states is constant [35], leading to the following expression for a degenerate 2DEG density:

$$n_s = \int_{E_C}^{\infty} \frac{m^*}{\pi\hbar^2} f(E - E_f)d$$
$$= \frac{m^*kT}{\pi\hbar^2} \ln\left[\frac{1}{1 + \exp\left(-\frac{E_C - E_f}{kT}\right)}\right], \quad (6)$$

where we have assumed single sub-band occupation. Rearranging, and with $n_s(V_G)$ measured from integrating the C–V profile in figure 4(b), the distribution of interface traps with energy level below the conduction band E_c is obtained for the channel region in the vicinity of the barrier channel interface [36]

$$E_C - E_f = -kT \ln\left[\exp\left(\frac{n_s\pi\hbar^2}{m^*kT}\right) - 1\right]. \quad (7)$$

The distribution of interfacial traps is plotted in inset of figure 4(b), showing a uniform distribution below the conduction band. This distribution is atypical for III-N devices, which normally show an exponential dependence of D_{it} near the conduction band [36]. The total trap density is $\sim 2 \times 10^{12}$ cm^{-2}.

4. Conclusions

In summary, we have demonstrated V_{th} control in $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ MOS-HFET using ALD deposited high-k ZrO_2 gate dielectric. By using a doped barrier design, high drain-currents of 0.5 A mm^{-1} were achieved, whereas the ZrO_2 gate dielectric reduces the gate leakage currents by a factor of more than 10^4 when compared to Schottky-gate devices. We have found that fixed oxide charges result in a significant, $\sim$3.5 V positive threshold voltage shift compared to Schottky-gate devices. Further improvements in growth process and the device geometry may enable enhancement mode UWBG AlGaN channel devices.

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ORCID iDs

Shahab Mollah https://orcid.org/0000-0002-2848-2959

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