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Ultrawide Bandgap $Al_xGa_{1-x}N$ Channel Heterostructure Field Transistors with drain currents exceeding 1.3 A/mm

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We report an Ultrawide Bandgap $Al_{0.4}Ga_{0.6}N$ channel Metal-Oxide-Semiconductor Heterostructure field effect transistor with drain currents exceeding 1.33 A/mm (pulse) and 1.17A/mm (DC), around a 2-fold increase over past reports. This increase was achieved by incorporating a hybrid barrier layer consisting of an AlN spacer, n-doped $Al_{0.6}Ga_{0.4}N$ barrier and a thin reverse graded $Al_xGa_{1-x}N$ (x from 0.60 to 0.30) cap layer. To enhance current spreading, a "perforated" channel layout comprising of narrow channel sections separated by current blocking islands was used. A composite ALD deposited ZrO_2/Al_2O_3 film was used as gate dielectric. A breakdown field above 2MV/cm was measured.

Index Terms— UWBG AlGaN MOSHFET, Perforated channel, RC-constant, Self-heating, Thermal resistance.

To take advantage of their high breakdown field, several research groups at present are developing ultrawide bandgap (UWBG) $Al_xGa_{1-x}N$ (x>0.4) channel heterostructure field effect transistors (HFETs) for high-temperature, high-voltage, and high-power applications. The higher breakdown field leads to a much higher Baliga Figure of Merit (BFOM).[1,2] Devices with channel alloy compositions of 40% or higher have been reported by several groups including ours.[3,4,5] To date, all these reported AlGaN channel devices have their drain currents well below 1 A/mm which is a typical value for GaN channel HFETs with micron size gate lengths.[6-9] This is also the case even for the insulating gate devices where a positive gate-bias can be used for increasing the drain-currents. The fundamental reason for this is the alloy scattering which leads to the 2-dimensional electron gas (2DEG) mobility in UWBG AlGaN channel layers approximately a factor of 3-5 lower than that of GaN.[10-12] Thus, the sheet resistance values for UWBG AlGaN channel HFETs are typically 2000 Ω/□ as compared to around 300 Ω/□ for GaN channel devices.[13-15] Another current limiting factor is the difficulty in forming formation of low resistivity ohmic contacts to UWBG AlGaN layers. For these layers, the barrier heights are very high, and contacts typically show a Schottky type behavior.[16] For direct contacts to the AlGaN barrier layers, even with high doping and Al-compositions around 0.60, contact resistance is typically over 4 ohm-mm.[17] This again is approximately a factor of 6 higher than that for the GaN channel HFETs.[18]

To decrease the contact resistivity and increase the peak drain currents in UWBG AlGaN channel HFETs and MOSHFETs, several approaches have been explored. Xue et. al. used highly *n*-doped $Al_xGa_{1-x}N$ selectively grown contact layers on top of the UWBG AlGaN barrier layers.[19] However, the lowest achieved contact resistivity was still around 3.9 Ω-mm and, even with 0.16 μm long gates in a 1.2 μm access opening, the peak currents were limited to only 0.42 A/mm (at a gate voltage of +0V). We reported on a new device design for MOSHFETs with *n*-doped barrier layers and achieved a contact resistivity as low as 1.6 Ω-mm and peak drain currents as high as 0.6 A/mm at a gate-voltage of +6V for 2 μm gate-length devices (access region 6 μm).[20] Higher gate-voltages led to excessive leakage currents from the breakdown of the PECVD deposited gate oxide (SiO_2). More recently, we have also reported on a microchannel approach for reducing the effective contact resistance. For a 1:6 (fill factor), a 100 nm long gate in a 1.6 μm long access region, a peak drain-current of 900 mA/mm was measured at a gate voltage of +2V (Schottky gate).[21] The processing sequence for fabricating these micro-channel devices was complicated

with several steps needing precise e-beam lithography. Moreover, high gate leakage in these HFET devices limits usage of positive gate bias and it also reduces the breakdown voltage.

In this paper by incorporating several innovations in the epi-material and device design, we report Al_2O_3/ZrO_2-$Al_{0.6}Ga_{0.3}N$-$Al_{0.4}Ga_{0.6}N$ depletion mode (D-mode) MOSHFETs with peak drain current I_{Dmax} more than 1.3 A/mm, a high transconductance 90 mS/mm and a breakdown field of 2 MV/cm. The devices exhibited very large I_{ON}/I_{OFF} values that were higher than 10^8.

The device schematic cross-section is shown in Fig. 1(a). It consisted of a 3 μm thick, high-quality AlN/sapphire template on which an $Al_{0.4}Ga_{0.6}N$ channel layer was grown using low pressure metalorganic chemical vapor deposition (LP-MOCVD). Hybrid barrier design reported here includes 0.3 nm thick AlN spacer layer followed by a 15 nm thick Si-doped *n*-$Al_{0.6}Ga_{0.4}N$ barrier layer followed by a 20 nm thick reverse composition graded Si-doped $Al_xGa_{1-x}N$ (x from 0.6 to 0.3 layer. This top layer was incorporated to assist ohmic contact formation. The use of reverse-graded layer allows achieving low contact resistance. The high barrier doping compensates the mobile positive charges resulting from the reverse composition grading.[22)]

In addition to the new epilayer design, we also incorporated a perforated channel (PC) layout [Fig. 1 (b)] which was shown to significantly reduce source and drain access resistances[21,23)]. In this design, the device channel consists of relatively narrow 2DEG sections ("straits") separated by current blocking islands. Very high 2DEG concentration enables strong current spreading from the channel straits into the S-G and G-D regions. Current flow profiles are schematically shown by shaded areas in Fig. 1(b). 2D simulations show that 4μm away from the gate edge the current density in between the channel straits is only two times lower than that along the strait center. As a result, the equivalent width of the S-G and G-D access regions, including the contact regions is larger than that of the gate strait hence leading to substantially lower access resistances. Importantly, the HFET capacitance coming mainly from the strait regions does not increase in PC design (see more on this below). For the current study, both the continuous channel (CC) and PC geometry devices were fabricated on the same wafer to allow for a direct comparison of their electrical and thermal performance. For the fabricated devices, the gate-length, gate-source and gate-drain spacing were $L_G \approx 2.0$ μm, $L_{SG} \approx 2$ μm and $L_{GD} \approx 2$-8 μm. For the PC layout, the width of channel sections were $W_S \approx 3.75$ μm, with blocking gaps between them $W_B \approx 8.25$ μm. This geometry corresponds to gap/strait ratio of 2-2.5 which is close to an optimal value as shown in

ref. [23]. The device processing started with mesa-isolation using chlorine-based inductively coupled plasma reactive ion etching. (ICPRIE) The device source/drain electrodes of 15 nm Zr/100 nm Al/40 nm Mo/30 nm Au were deposited using electron-beam evaporation, followed by rapid thermal annealing (RTA) at 950 °C for 30 s in N_2 environment. After the ohmic fabrication, the conducting channels and the blocking islands were formed using standard photolithography and ICPRIE processes. The etch depth to form the current blocking islands was 200 nm to ensure complete isolation of the 2DEG channel straits. Hot tetramethylammonium hydroxide treatment was used to remove post plasma etch residue [24]. Atomic Layer Deposition (ALD) was then used to deposit Al_2O_3/ZrO_2 bilayer for the gate insulator followed by e-beam gate metallization consisting of 100 nm Ni/200 nm Au. Details of ALD process are described in [26]. Identical geometry HFET and MOSHFET devices both with the (CC) and the (PC) layout were fabricated on the same epi-wafer for a comparative study. The transistor surface was also protected with PECVD deposited 400 nm SiO_2 film for high voltage measurements.

The sheet and contact resistances were measured using TLM patterns. The ohmic contact resistance was found to be 1.7 Ω mm which is one of the lowest reported to date for UWBG $Al_xGa_{1-x}N$ channel HEMTs.[25] In addition, the fabricated MOSHFETs were characterized in both the DC and the pulse regimes to reduce heating effects at high drain currents. Short-pulse I-Vs were measured using DIVA D260 dynamic IV analyzer with pulse duration of 500 ns and low duty cycle of 0.1%. Current-voltage characteristics of the MOSHFET with $L_{SD} \approx 8$ μm ($L_{GD} = 4$ μm) are shown in Fig. 2 (a). The drain currents are normalized to the channel width. For the PC-device the channel width is taken as the total width of all straits. This way of accounting for the total channel width is very similar to that used in large periphery multi-finger FETs. In those devices, substantial (50 – 150 μm long) portions of the gate metal are used to connect elementary sections of multi-finger device; the length of these connections is not included in the total width when calculating the normalized current. In PC design the gate lines connecting straits perform the same function as section-to-section connections in multi-finger design. The combination of the hybrid barrier design and bi-layer gate dielectric allows operation at a positive gate bias as high as 12 V without any excessive gate-leakage. As seen, pulse drain saturation current is as high as 1.33 A/mm (at V_{GS}=+12V). Even in DC mode the peak drain current exceeds 1.17 A/mm. In Fig. 2(b) we include device transfer characteristics and the transconductance curve in DC mode. The measured transconductance value of 90 mS/mm for DC mode (as high as 110 mS/mm for pulse

mode) is also more than twice that of the reported value on identical geometry devices in the past.[20] The total on-resistances for the PC devices, extracted from the I-V slopes at low drain voltage are $R_{ON}(PC) \approx 10$ Ω-mm which is about of factor of two less than R_{ON} of the (CC) device with the same L_{SD}. The threshold voltage Vth = -11 V was the same for both the CC and the PC layouts and was not affected by introduction of additional epi-layers compared to previously reported results [20,23,26].

Relative contributions of the three key features employed in current design, namely – (1) reverse graded barrier layer, (2) perforated channel layout and (3) MOS- gate design – towards maximum drain current are shown in Fig. 3 (a). It was found that hybrid barrier just slightly increases saturation current; however, it significantly improves the contact resistance and reduces the leakage current which leads to a higher breakdown voltage as discussed below. Channel perforation doubles the maximum drain saturation current of previously reported HFET [20]. Figure 3 (b) shows reduction of the gate-leakage current that results from the introduction of the hybrid barrier and the composite high-*k* gate insulator. For the Al_2O_3/ZrO_2 MOSHFET, the gate leakage current remains in μA/mm range even at a gate voltage as high as +12V. The dramatic decrease of the gate leakage current allows device to be operated in positive gate bias regime thus pushing saturation current well above 1.3 A/mm.

As seen from Fig. 2(a) the difference between pulse and DC drain currents which we attribute to self-heating is relatively small. To evaluate the self-heating effects, we extracted the active region temperature in the CC and the PC-MOSHFETs by comparing short-pulse drain saturation currents (no self-heating) at different ambient temperatures with DC drain saturation current at the same drain voltage. The details of the temperature extraction procedure are outlined in [27,28]. The probe station stage temperature was varied from room to 250 °C in 50 °C increments. We found that the channel temperatures for the CC- and the PC-MOSHFET were 329 °C (at dissipated power 0.497 W) and 179.6 °C (at 0.560 W) respectively. The thermal resistance was then found as $R_{TH} = \Delta T / P$, where ΔT is the temperature increase due to self-heating. The obtained thermal resistance for the PC-MOSHFET was $R_{TH\text{-}PC}$ =13 K.mm/W; that of the CC-MOSHFET $R_{TH\text{-}CNV}$ = 29 K.mm/W; therefore, R_{TH}-PC ≈ 0.40 × $R_{TH\text{-}CNV}$. The obtained $R_{TH\text{-}PC}$ value is also smaller than 25K.mm/W reported for III-N HFETs on sapphire in ref. [27] Because the total channel width and hence the power density are about the same for CC- and PC-MOSHFETs, we conclude

that the PC design also offers significant improvement in the heat removal. We attribute this improvement to a better heat spreading in the buffer and the AlN template under the straits of PC-MOSHFET.

Figure 4 shows the breakdown voltage dependence for devices with different gate to drain spacings of 2, 4 and 8 μm. As seen from the data, breakdown voltage increases to nearly 1000V for the largest spacing. The maximum breakdown field of 2.08 MV/cm achieved for the 2 μm gate–drain spacing exceeds most reported for AlGaN-channel devices.[29,30] Note, these devices had no field-plates and they did not undergo any special surface treatment other than the SiO_2 coating. We therefore expect that the breakdown field and the device operating voltages to further go up with better surface treatment and field-plating.

An important characteristic of transistor switches is Baliga High-Frequency Figure of Merit BHFFOM.[31] BHFFOM = $f_{BHF} = 1/(R_{ON} \times Cin)$, where R_{ON} is the device on-resistance and C_{in} is the input capacitance. For FETs, $C_{in} \approx C_G$ where C_G is the gate capacitance. At zero gate voltage, $V_G = 0$, the capacitances of the CC- and PC- devices were 8.7 pF/mm and 2.7 pF/mm respectively. Hence, the gate capacitance C_G of the PC-MOSHFET is around 3 times smaller than that of the CC-MOSHFET. Experimentally obtained values of R_{ON} and C_G allow to compare the BHFFOM for conventional and PC-MOSHFETs: $f_{BHF\text{-}CC} = 4.6$ GHz and $f_{BHF\text{-}PC} = 8$ GHz. As evidenced by these results, the maximum switching frequency for PC-MOSHFET is significantly higher than that of a conventional continuous channel geometry device.

In summary, for the first time we have demonstrated perforated channel UWBG AlGaN MOSHFET, with the saturation drain current exceeding 1.3 A/mm. The devices with a new composite barrier and gate-insulator design exhibit a three terminal breakdown field higher than 2 MV/cm and an extremely low gate-leakage current. The PC-MOSHFET device design leads to a factor of two lower access resistance due to the current spreading that occurs between the conducting channel sections and the larger area source and drain contacts. As a result, the PC-device design has nearly a two times higher unit-width channel current and Baliga high-frequency figure of merit. In addition, due to enhanced heat spreading, their thermal resistance is also more than two times lower than a continuous channel device on the same epilayer structure.

Acknowledgments

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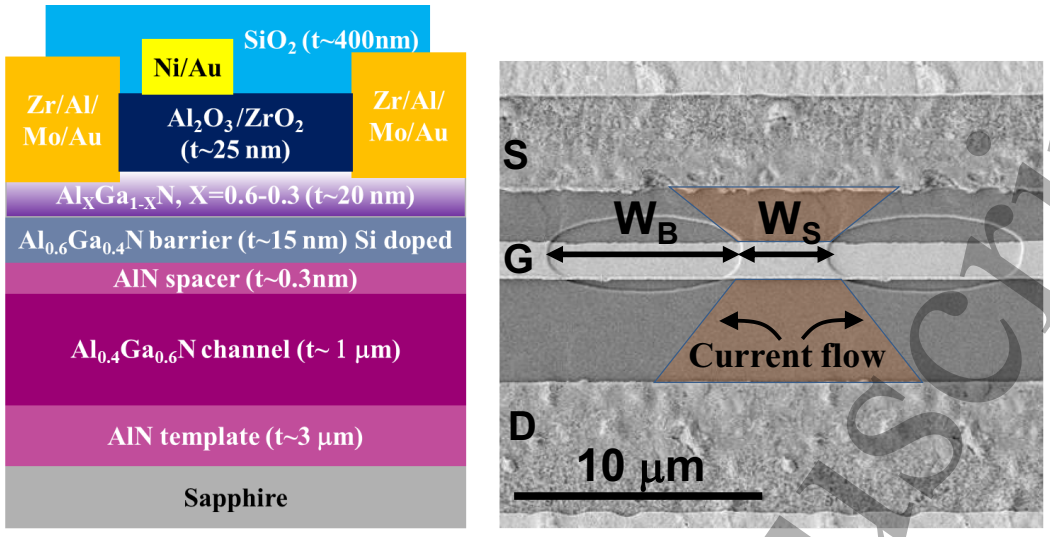
Figure Captions

Fig. 1. (a)Schematic structure, and (b) layout of the PC-MOSHFET.

Fig. 2. (a) IV characteristics of MOSHFET in DC (solid lines), and pulse mode (open circles). (b) DC transfer curve and transconductance at V_D=20 V.

Fig. 3. Effect of key factors incorporated in the MOSHFET design on (a) maximum drain current and (b) gate leakage current.

Fig. 4. Breakdown characteristics of MOSHFETs with different gate-drain spacing.



(a) (b)

Fig. 1.

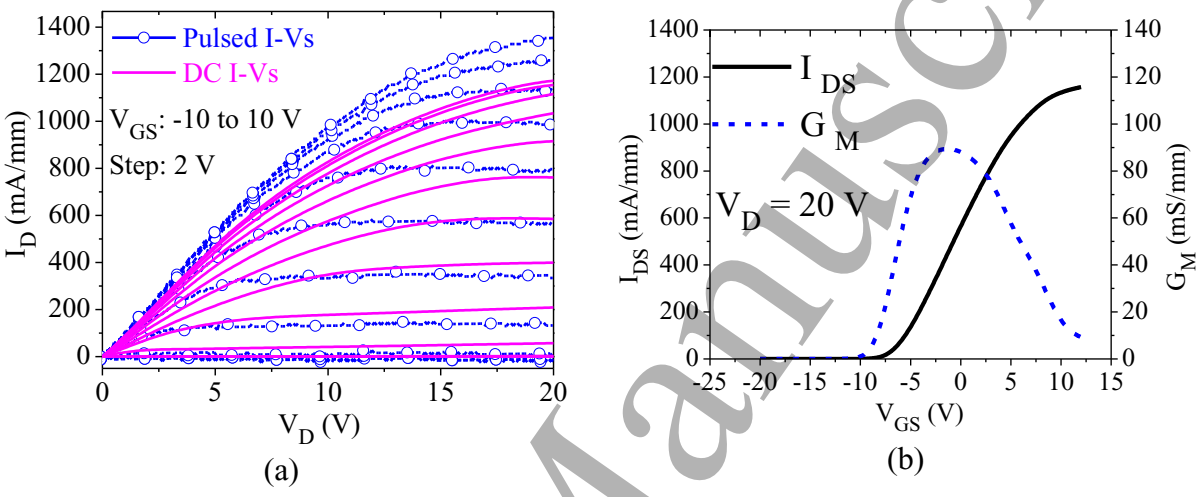


Fig. 2.

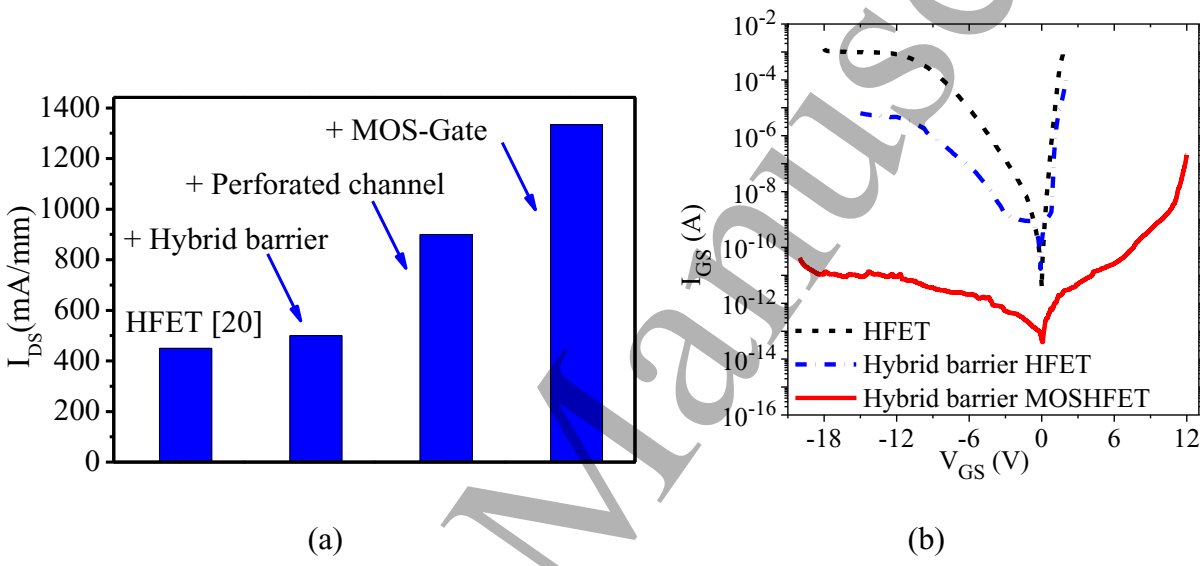


Fig.3.

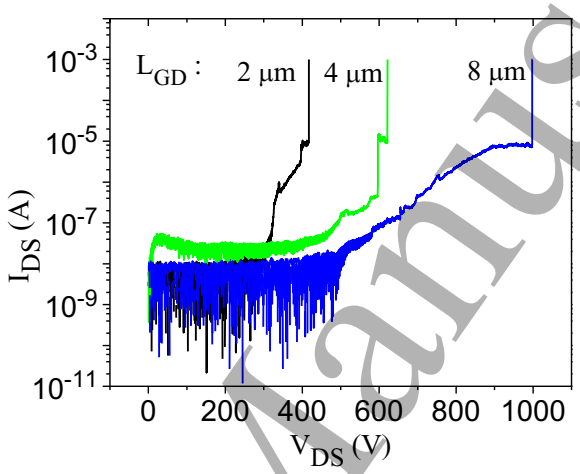


Fig. 4.