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High-Temperature Operation of $Al_xGa_{1-x}N$ ($x > 0.4$) Channel Metal Oxide Semiconductor Heterostructure Field Effect Transistors with High-k Atomic Layer Deposited Gate Oxides

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Due to their superior breakdown fields compared with GaN and SiC and high thermal conductivity, $Al_xGa_{1-x}N$ ($x > 0.4$) channel high-electron-mobility transistors (HEMTs) will find applications in extreme environments such as power electronics. Herein, the high-temperature operation of ultrawide-bandgap (UWBG) $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ metal oxide semiconductor heterostructure field effect transistors (MOSHFETs) with atomic layer-deposited (ALD) high-k gate dielectrics TiO_2, Al_2O_3, and ZrO_2 is reported. As compared with similar geometry HFETs, these devices exhibit a simultaneous reduction in gate-leakage current by $\approx 10^4$ and a positive shift of the threshold voltage as much as 4 V. This positive threshold shift indicates the introduction of negative charges at the oxide/barrier interface and within the thin oxide, attributed to the pre-ALD plasma treatment. The gate leakage increases weakly with temperature up to 250 °C, whereas the peak drain currents decrease from $\approx$0.5 to 0.3 A mm^{-1}. An analysis of the C–V and I–V characteristics reveals that this drain current decrease is due to a reduction in channel electron mobility. The potential mechanisms responsible for this are discussed. Up to the measured temperature of 250 °C, the devices withstand repeated temperature cycles without catastrophic degradation or breakdown, underscoring the promise of these materials.

1. Introduction

AlGaN channel high-electron-mobility transistors (HEMTs) are potential candidates for the next-generation power switching transistors because of their ultrawide bandgap (UWBG).[1–7] The advantages of using wider-bandgap AlGaN material are to enhance the breakdown voltage, which leads to higher output power densities. The breakdown voltage of high-Al composition $Al_xGa_{1-x}N$ ($x > 0.5$) is expected to be approximately three times higher than that of GaN, and the thermal conductivity of AlN is six times higher than sapphire and 1.5×–2× higher than GaN.[8] So the thermal conductivity of AlGaN channel is higher than that of GaN and below AlN. Thus, the Baliga Figure of Merit (BFOM) of $Al_xGa_{1-x}N$ ($x > 0.5$) channel devices is higher than those of GaN and SiC channels.[8–10] They also have been shown to have excellent radiation hardness[11] with a cut-off wavelength in the solar-blind spectral region. Thus UWBG III-N materials are promising candidates for compact next-generation power electronics,[8,12–16] solar-blind photodetection,[17,18] and nuclear reactor controls requiring radiation hardness.[19] As was previously shown, the wider bandgap of material also improves the temperature stability of heterostructure field effect transistor (HFET) devices with high Al content. A dramatic reduction in gate leakage at a high temperature was achieved when atomic layer-deposited (ALD) high-k oxides were used in metal oxide semiconductor heterostructure field effect transistors (MOSHFETs) operating at temperatures up to 500 °C.[20,21]

Our research group recently reported on $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ MOSHFETs with SiO_2 gate dielectric. SiO_2 was deposited using a plasma-enhanced chemical vapor deposition (PECVD) process.[22] These devices showed a record drain current of 0.6 A mm^{-1}. However, an oxide thickness greater than 100 Å was required for a factor of 10^3 reduction in the gate current compared with HFET fabricated on the same material. Therefore, the use of SiO_2 increased the threshold voltage (toward more negative) by about 2 V. Our past work with GaN channel MOSHFETs also established that the use of high-k gate oxides mitigates this problem by producing very low gate-leakage current without a substantial increase in the threshold voltage.[23]

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This is the motivation behind the study reported in this article. To circumvent the issue of the threshold voltage increase in SiO_2 AlGaN MOSHFETs, we for the first time report the fabrication and characterization of $Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ MOSHFETs with ALD high-*k* gate dielectrics (TiO_2, Al_2O_3, and ZrO_2).

2. Experimental Section

Figure 1a shows the epitaxial heterostructure and device geometry. The AlGaN HEMT structure was epitaxially grown on a 3 μm-thick AlN /sapphire template using the metalorganic–chemical-vapor deposition (MOCVD) process. The details of the MOCVD growth procedure can be found in a study by Fareed et al.[24] The off axis (102) X-ray peak line width for the AlN layers of our templates was measured to be 330 arcsecs, which translated to an overall defect density of $(1–3) \times 10^8\ cm^{-2}$ based on our past calibration. The growth of 500 nm $Al_{0.40}Ga_{0.60}N$ followed by the 30 nm Si-doped $Al_{0.65}Ga_{0.35}N$ barrier layer completed the structure. The barrier layer was doped to enable both better contact and a higher sheet charge density in the channel. Post-growth contactless sheet resistance mapping indicated a sheet resistance (R_{SH}) of 1900 Ω. The barrier layer carrier concentration due to Si doping measured from the $1/C^2$ versus V plot was $\approx 4–6 \times 10^{18}\ cm^{-3}$.

The device processing started with mesa-isolation using Cl_2-based inductively coupled plasma reactive ion etching (ICP-RIE). The device source/drain electrodes of 15 nm Zr/100 nm Al/40 nm Mo/30 nm Au were deposited using electron-beam evaporation followed by rapid thermal annealing (RTA) at 950 °C for 30 s in N_2 environment. The ohmic contact resistance measured by the transmission line model (TLM) method was found to be 1.64 Ω mm, which gives an equivalent ohmic specific contact resistivity of $\approx 1.4 \times 10^{-5}\ \Omega\ cm^2$. The gate metal that consisted

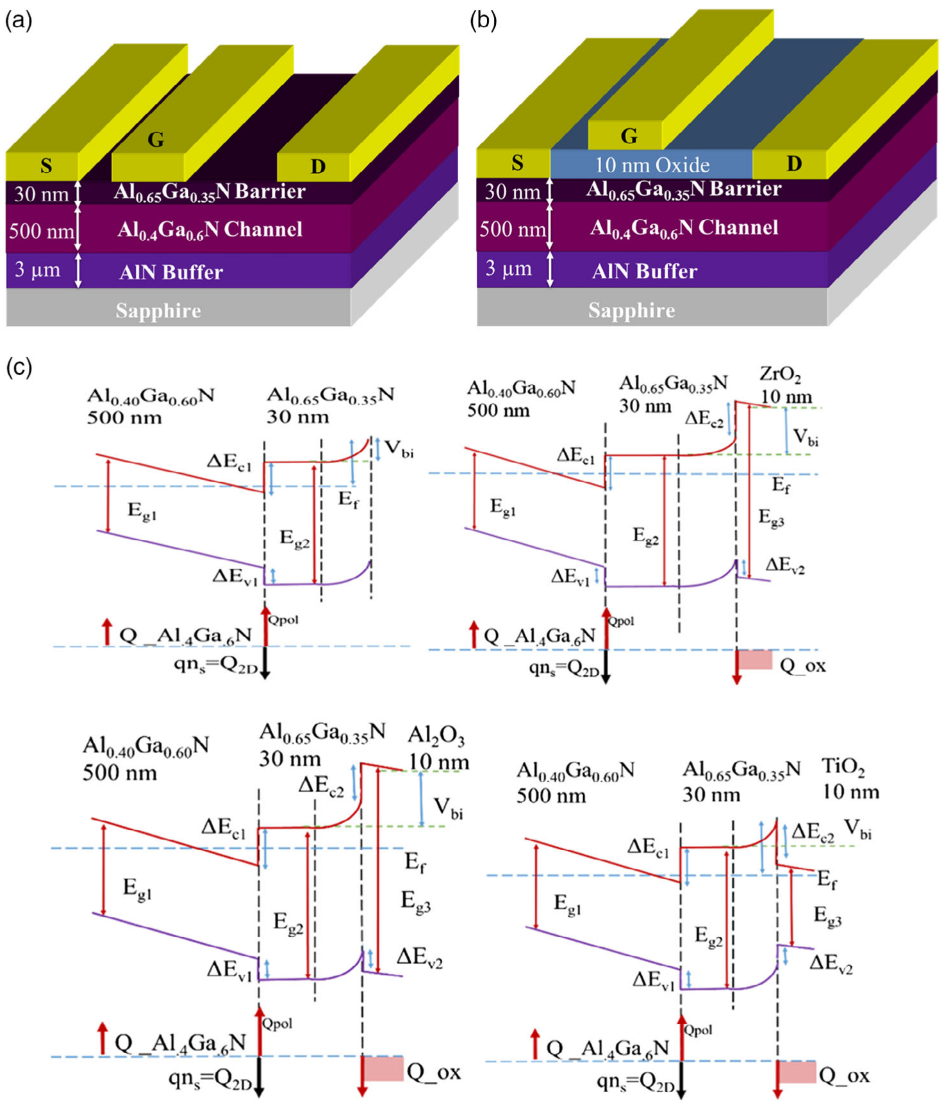

Figure 1. The device structure of the a) HFET and b) MOSHFET. c) Band diagram of HFETs and MOSHFETs, following values are for ZrO_2 as representative from this oxide group: $E_{g1} = 4.52$ eV, $E_{g2} = 5.22$ eV, $E_{g3} = 6$ eV $\Delta E_{v1} = 0.21$ eV, $\Delta E_{c1} = 0.49$ eV, $\Delta E_{v2} = 0.234$ eV, $\Delta E_{c2} = 0.546$ eV, $V_{bi} = 2.7$ V, and $Q_{ox} = -3.1 \times 10^{13}$ q Ccm^{-2}.

of 100 nm Ni/200 nm Au was deposited using electron-beam evaporation. In addition to devices with gate length 1.8 μm, gated transmission line model (GTLM) test structures with gate lengths ranging from 10 to 100 μm were also fabricated.

Four sets of devices with identical geometries were fabricated on same wafer for this study. These consisted of devices with Schottky gates and with three different oxides under the gate metals. The ALD oxide thickness was 10 nm. The TiO_2 film was deposited by the plasma-enhanced ALD (PE-ALD) system at 350 °C, using tetrakis (dimethylamido) titanium (IV) (TDMAT) and Ar/O_2 plasma (80/20 sccm) as precursors. The TDMAT precursor was heated to 75 °C to ensure sufficient vapor pressure to attain a saturated linear growth rate of 0.6 Å $cycle^{-1}$. The deposition of the TiO_2 film was initiated by 15 in situ plasma pulses prior to the alternating precursor pulses for film growth.[25–27] For the ZrO_2 and Al_2O_3 gate oxide films, thermal ALD processes at 200 and 250 °C, respectively, were used, with trimethylaluminum (TMA), tetrakis (dimethylamido) zirconium (IV) (TDMAZ), and deionized water as the precursors. The TDMAZ precursor was also heated to 75 °C to achieve a linear growth rate of 0.7 Å $cycle^{-1}$. For both the Al_2O_3 and the ZrO_2 films, deposition was initiated with 15 water pulses prior to the typical AB pulsing sequence to deposit the gate dielectric to ensure saturation of hydroxyl groups at the AlGaN surface required for conformal ALD nucleation.[25,28–30] The thickness of the ALD films was obtained by ellipsometry, using witness samples grown on Si substrates in the same run, giving a thickness of 10 nm. These deposition processes have been thoroughly characterized on III-N devices in previous studies for ZrO_2,[31] Al_2O_3,[30] and TiO_2[25,32] and were shown to give amorphous dielectrics as deposited.

3. Results and Discussion

The transfer (I_{DS} vs V_G) and the output I–V characteristics were measured using a parameter analyzer and the capacitance voltage (C–V) measurements were done using a HP 4284 A Precision LCR Meter. **Figure 2**a shows the drain I–V characteristics of the fabricated AlGaN channel ZrO_2 MOSHFET, with a 1.8 μm-long gate (L_G), in a 6 μm source–drain spacing. Clear saturation and pinch off are observed. Figure 2b,c shows the peak currents of same geometry ALD MOSHFETs with different dielectrics compared with that of the HFET at room temperature and 250 °C, respectively. The I–V characteristics of Al_2O_3, ZrO_2, and TiO_2 MOSHFETs are similar with peak currents ≈0.44 A mm^{-1} at $V_G = +2$ V, ≈0.5 A mm^{-1} at $V_G = +6$ V, and ≈0.54 A mm^{-1} at $V_G = +6$ V correspondingly at room temperature. These currents are higher than the HFET (i.e., no oxide under gate) peak currents of ≈0.4 A mm^{-1}, at $V_G = +2$ V, which is maximum gate voltage that can be applied without triggering high gate leakage current. Higher peak currents in MOSHFETs are due to the higher positive voltage that can be applied to the gate. At 250 °C, the peak drain currents of Al_2O_3, ZrO_2, and TiO_2 MOSHFETs are 0.3, 0.31, and 0.35 A mm^{-1}, respectively, whereas for HFET, it is 0.38 A mm^{-1} under same gate voltage condition of room temperature. Thus, at 250 °C, the peak currents decrease by 35%, 38%, 32%, and 5% from room-temperature peak current for TiO_2, ZrO_2, Al_2O_3, and HFET, respectively.

The room-temperature transfer characteristics of Figure 2d were measured using 10 μm-long gate MOSHFETs. This was done to ensure that in the subthreshold regime, the gate leakage current is dominated by bulk rather than the surface leakage. This allows a direct comparison of the gate isolation by the different dielectrics. The transfer curves show that the ON/OFF ratio of $\approx 10^3$for the HFET increases to $\approx 6 \times 10^6$ for devices with ZrO_2 and Al_2O_3 gate dielectrics. This improvement is primarily from the reduction in the gate leakage current (Figure 2d inset). The I_G–V_G curves in the inset of Figure 2d show a reduction in gate leakage current by five orders of magnitude for Al_2O_3 and ZrO_2 and by approximately two orders of magnitude for TiO_2 gate devices. We attribute the poorer reduction of gate leakage current in TiO_2 devices to a smaller bandgap of this material compared with the other two dielectrics used in our study (**Table 1**). Using data in Figure 2d, the values of the threshold voltage V_{th} were obtained as V_G voltages at which the drain current decreases to 30 μA. Figure 2e shows the transfer characteristics of these devices at 250 °C. From room temperature (RT) to 250 °C, the threshold voltage changes from −9.8 to −10 V, −12.7 to −12.8 V, −10 to −10.5 V, and −13.5 to −14 V for ZrO_2, Al_2O_3, TiO_2, and HFET, respectively.

The transfer characteristics of Figure 2d show a positive shift in V_{th} for all the ALD MOSHFETs as compared with that of HFET. This is opposite to what is observed for the PECVD SiO_2 MOSHFETs,[23] where a reduction in gate leakage current is usually accompanied by a more negative V_{th}.[33] The threshold voltage, V_{th}, showed a "positive shift" by ≈4 V for the ZrO_2 and TiO_2 dielectrics and by ≈1 V for the Al_2O_3 gate devices. A positive threshold voltage shift is an important effect that may help creating normally off (enhancement mode) MOSHFETs which are very important for use in power electronics applications. The shift in V_{th} can be caused by a fixed negative charge in the oxide or the oxide/barrier interface or both. Oxide and interfacial charges also play an important role in the switching and high-frequency performance of wide-bandgap MOSHFETs.[34] Frequency-dependent C–V measurements were done for all ALD MOSHFETs to determine these fixed charges.

For the study, large-area FETs with gate length $L_G = 100$ μm and gate width $W = 200$ μm were used to test C–V characteristics. Frequency-dependent C–V characteristics for MOSHFETs are shown in **Figure 3**a–c. The carrier depletion at $V_G = 0$ V only extends partially into the barrier layer and does not reach the two dimensional electron gas (2DEG), which is true for all the MOSHFETs. This phenomena simplifies the analysis. Because of high doping in the barrier layer, it is possible to clearly distinguish three regimes seen in all devices: 1) depletion through barrier layer $-2\,V < V_G < 0\,V$ with $1/C^2$ dependence showing constant doping; 2) 2D electron gas at the barrier/channel interface $\approx -8\,V < V_G < -2\,V$; and 3) pinch off, with depletion extending into the channel epitaxial layer $V_G << -8$ V.

For all the devices, the boundary between regimes (1) and (2) represents the voltage at which 2DEG is being depleted, from which the capacitance of the gate at 2DEG is measured, C_{2D}, which is true regardless of whether an oxide is present.

The donor concentration in the barrier layer N_d is extracted from the linear $1/C^2$ characteristics in regime (1). For all the ALD oxide devices, this was $\approx 4–5 \times 10^{18}$ cm^{-3}, whereas for the HFET, this was significantly higher at 6.8×10^{18} cm^{-3}.

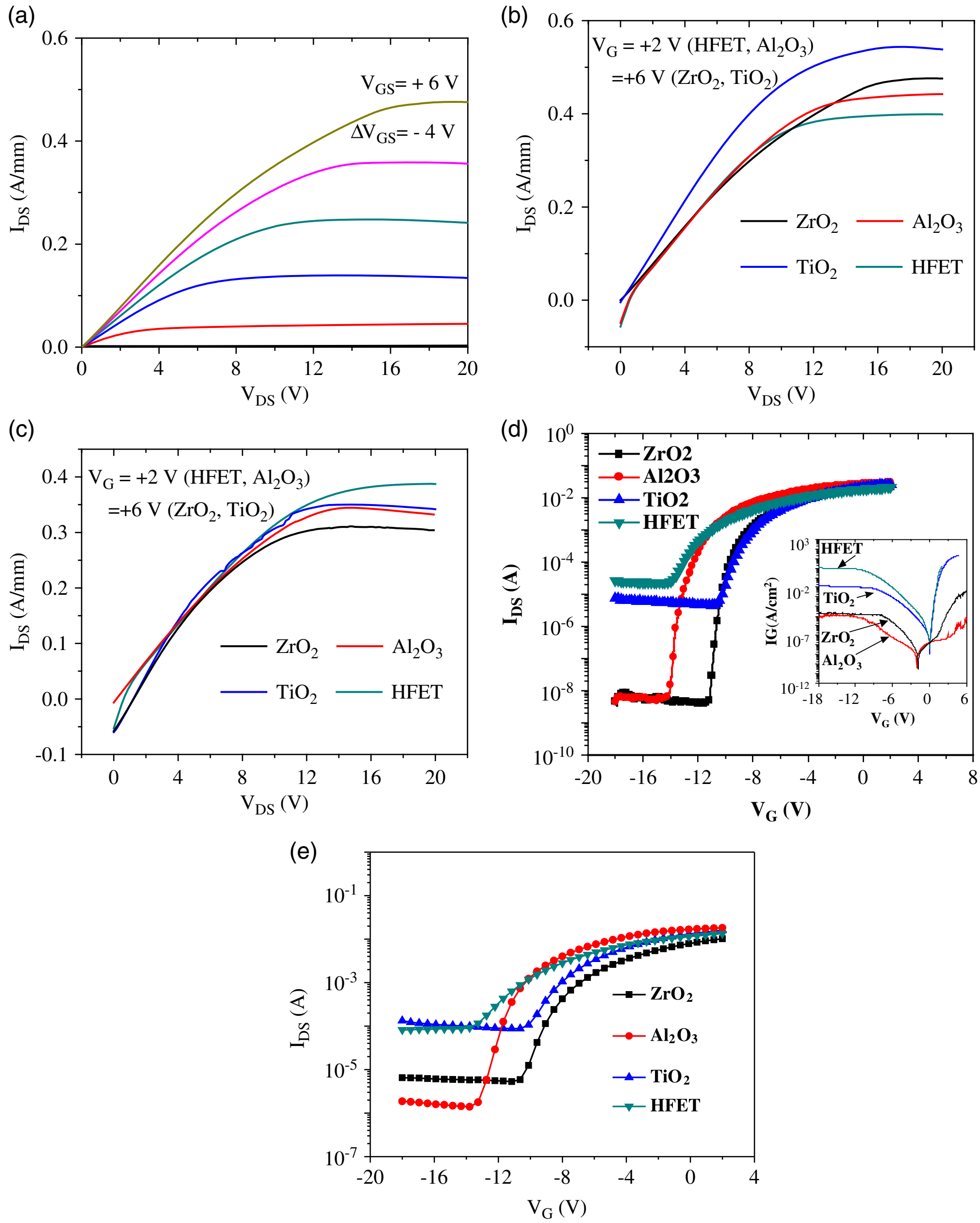

Figure 2. a) Output characteristics of ZrO_2 MOSHFET. b)The peak current comparison of different MOSHFETs and HFETs at RT. c)The peak current comparison of different MOSHFETs and HFETs at 250 °C. d) The transfer characteristics of HFETs and MOSHFETs at RT. Inset shows the gate leakage current of HFETs and MOSHFETs. e) The transfer characteristics of HFETs and MOSHFETs at 250 °C.

Table 1. Summary of key transistor parameters. Here *k* is the dielectric constant, E_g is the bandgap of the gate dielectric, and *q* is the elementary charge.

	k/E_g [eV]	V_{th} (*I–V*)	V_{bi} (*C–V*)	On/Off	SS [mV dec^{-1}]	$N_{d,b}$ [cm^{-3}]	Q_{2D} [C cm^{-2}]	Q_{ox} [C cm^{-2}]
HFET	None	−13.7	3.0	10^3	1290	6.8×10^{18}	1.9×10^{13}q	None
Al_2O_3	8/6 eV	−12.9	5.5	6×10^6	105	5.0×10^{18}	1.9×10^{13}q	$+0.8 \times 10^{12}$q
ZrO_2	25/6 eV	−10.3	2.6	6×10^6	190	4.2×10^{18}	1.5×10^{13}q	-3.1×10^{13}q
TiO_2	80/3.2 eV	−10.0	2.0	2×10^4	740	4.4×10^{18}	1.4×10^{13}q	-1.4×10^{13}q

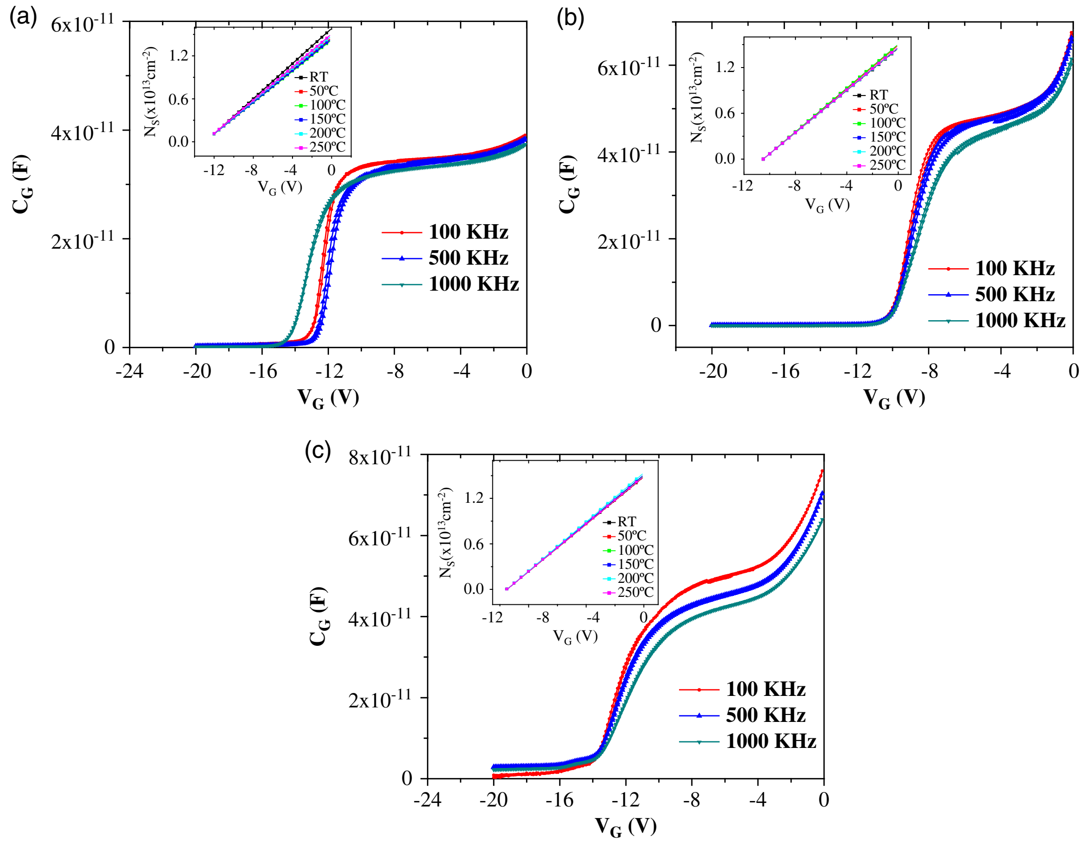

Figure 3. Frequency-dependent *C–V* characteristics of a) Al_2O_3, b) ZrO_2, and c) TiO_2 MOSHFETs. Inset figures show the temperature-dependent carrier concentration of corresponding MOSHFETs.

This change from HFET to MOSHFET in N_d value is due to the in situ pre-ALD surface preparation. From the boundary between regimes (1) and (2) for the HFET, where 2DEG is located at the barrier/channel interface, the barrier thickness is extracted using the formula $t_b = \varepsilon_s / C_{2D,}$ where C_{2D} is the capacitance of the boundary between regimes (1) and (2) for the HFETs. The extracted barrier thickness is 30 nm. We use this value of t_b for all the other MOSHFETs, which is justified, given that all these transistors were fabricated on quarters from the same wafer.

The built-in voltage V_{bi} (defined in Figure 1c band diagram), measured from the $1/C^2$ x-intercept in the figure, can be expressed in terms of x_d as follows[35]

$$V_{bi} = \frac{qN_d x_d^2}{2\varepsilon_s} + E_{ox} t_{ox} \tag{1}$$

For the HFET, $t_{ox} = 0$, so that from the measured N_d and V_{bi}, x_d is extracted to be 20 nm, in agreement with that extracted from the gate capacitance at $V_G = 0$ V i.e., $C(0)$, which is $x_d = \varepsilon_s / C(0) = 24$ nm, showing that our formalism here is self-consistent. The Q_{ox} extracted is shown in Table 1. The extraction procedure is outlined in our recent report.[36] Here, the negative Q_{ox} is responsible for depleting the 2DEG and making V_{th} more positive. Al_2O_3, being native to the AlGaN system, shows very low Q_{ox}. The small positive shift from the HFET to the Al_2O_3 MOSHFET is apparently due to the lower N_d in the barrier as discussed earlier.

From the difference in the high- and low-frequency *C–V* characteristics, the density of interface states, D_{it}, is obtained in cm^{-2}. It is a reasonable assumption that as the barrier here is doped, and relatively thick, ≈30 nm, the surface oxide charges, Q_{ox}, do not significantly impact trapping at the barrier/channel interface. At low frequencies, slow traps respond capacitively, whereas at high frequencies, they do not, leading to a decrease in measured capacitance at higher frequencies. Figure 3a–c shows this dispersion for the MOSHFETs. The total integrated trap density is $\approx 2–3 \times 10^{12}$ cm^{-2}. We also note that there is mild hysteresis near V_{th}, although the charge in the area bounded by this hysteresis is $\approx 0.5 \times 10^{12}$ cm^{-2}, small compared with that by the high–low method. **Figure 4**a–c shows the gate leakage characteristics of the MOSHFETs from RT up to 250 °C. The gate leakage is seen to be weakly dependent on temperature.

Considering the high ON/OFF ratio of these devices, we were also interested to calculate the subthreshold swing (SS), which characterizes how steep the device transition is from the ON to the OFF state as a function of gate voltage. Because the SS depends intrinsically on the barrier/channel interfacial trap density, and extrinsically on gate leakage, we provide our comparison of the SS values in HFETs and ALD MOSHFETs as follows. The results are shown in Table 1. The intrinsic SS is given by[37]

$$SS = \frac{60\,\text{mV}}{\text{decade}} \left[1 + \frac{qD_{it}(\text{cm}^{-2})}{C_G(V_{th})} \right] \tag{2}$$

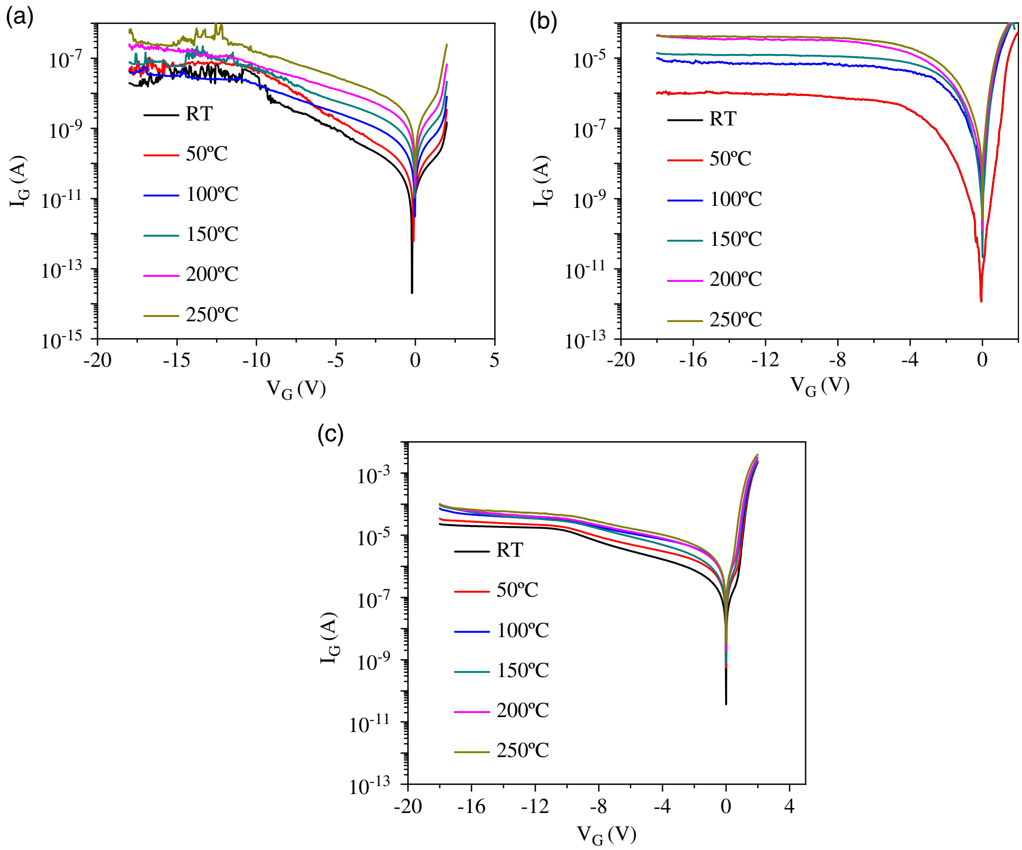

Figure 4. Temperature-dependent gate leakage of a) Al_2O_3, b) ZrO_2, and c) TiO_2 MOSHFETs.

where D_{it} (cm^{-2}) is the total interface charge density implying $^{\circ}2$–$3 \times 10^{12}\,cm^{-2}$, which is obtained by integrating the area under the low-frequency and high-frequency C_G dispersion curve. We note that the HFET and higher-leakage dielectric TiO_2 both display poor SS, which is artificially masked by the large gate leakage (Figure 2b inset) below V_{th} (Table 1), which also limits the ON/OFF ratio. By reducing the gate leakage with ZrO_2 and Al_2O_3, the intrinsic SS of the barrier/channel interface was recovered, as given by Equation (2), which is comparable with the SS values of previously reported AlGaN channel HEMTs.[8,38]

The gate voltage- and temperature-dependent mobilities of HFET and MOSHFETs were extracted using a technique that we have successfully used in the past for our AlGaN channel MOSHFETs,[22] as well as GaN channel MOSHFETs.[39] The 2D channel electron mobility μ is extracted from the measured channel conductance[22]

$$G_{ch} = qN_s\mu\frac{W}{L_G} \tag{3}$$

where W is the width of the channel and L_G is the gate length. The electron sheet concentration N_s can be found from the capacitance–voltage measurement using the following formula[22,39]

$$qN_S = (V_G - V_{TG})C_G \tag{4}$$

where q is the charge of electron, V_T is threshold voltage, V_G is the range of voltage aforementioned threshold, and C_G is the measured gate capacitance per unit area. Figure 3a–c insets show that the N_S value for ZrO_2 MOSFET at zero gate voltage is $\approx 1.5 \times 10^{13}\,cm^{-2}$ which is independent of temperature. In Equation (3), the G_{ch}, N_s, and μ are functions of gate voltage V_G. The channel conductance G_{ch} in turn, can be calculated from the measured drain–source resistance R_{DS}, the contact resistances of drain and source ($2R_C$), and access region resistances from gate drain (R_{GD}) and gate source (R_{GS})[22]

$$G_{ch}(V_G) = 1/[R_{DS}(V_G) - 2R_c - R_{GD} - R_{GS}] \tag{5}$$

The contact resistance (R_C) and sheet resistances (R_{SH}) were extracted from the TLM measurements. R_{GS} and R_{GD} were found from the extracted R_{SH} value and calculated with corresponding contact spacing L_{GS} and L_{GD}.

Figure 5 shows the MOSHFET channel electron mobility plot as a function of gate voltage and temperature, whereas the inset figures show the power law fitting of temperature-dependent mobility. At room temperature, the mobility for ZrO_2, Al_2O_3, and TiO_2 MOSHFETs varies from $\approx$200 to $\approx$550 $cm^2\,V^{-1}\,s^{-1}$, $\approx$300 to $\approx$650 $cm^2\,V^{-1}\,s^{-1}$, and $\approx$240 to $\approx$480 $cm^2\,V^{-1}\,s^{-1}$ at zero gate voltage and depleted channel conditions, respectively, whereas for HFETs, it varies from $\approx$250 to $\approx$1200 $cm^2\,V^{-1}\,s^{-1}$. The extracted mobility and sheet carrier density are comparable

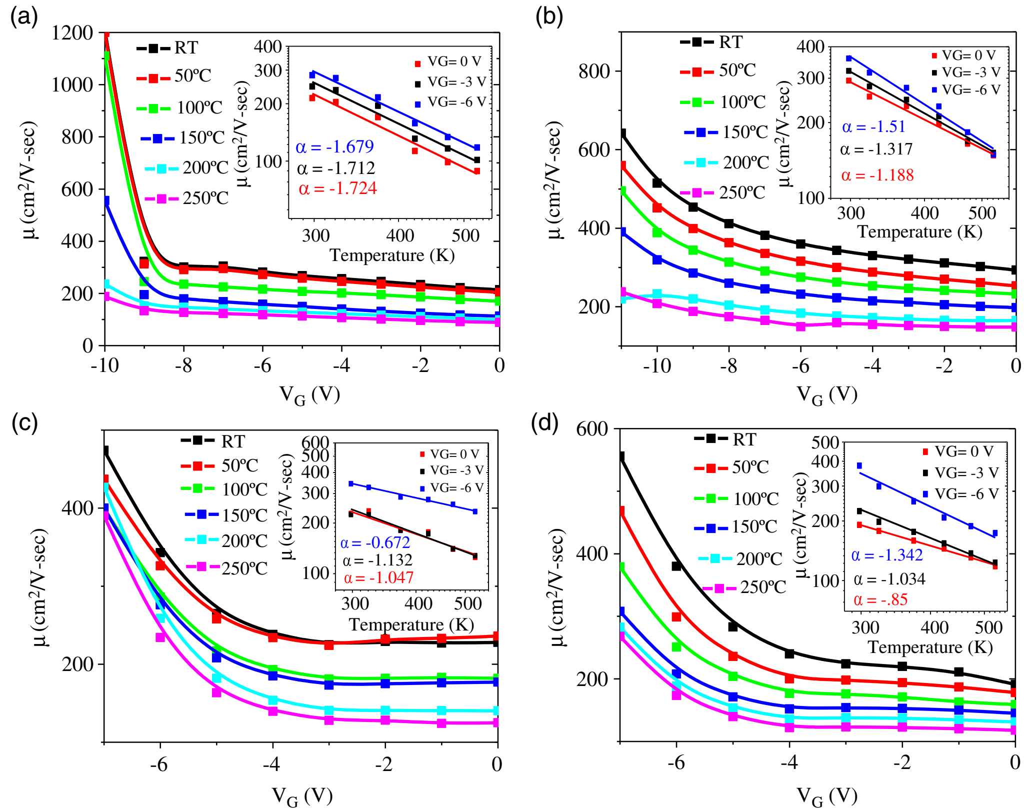

Figure 5. a) Temperature-dependent mobility as a function of gate voltage for a) HFET, b) Al_2O_3, c)TiO_2, and d) ZrO_2. Inset figures show power law fitting of mobility versus temperature plot to extract the power coefficient α.

with the earlier reported mobility and sheet carrier density of AlGaN channel HEMTs from our research group,[22] as well as reports of other groups. Baca et al. reported the 70–85% HEMT with RT mobility value of 390 $cm^2 V^{-1} s^{-1}$ and sheet carrier density of 7.2×10^{12} cm^{-2}.[40] Klein et al, in their AlGaN channel HEMT reported a value of mobility 240 $cm^2 V^{-1} s^{-1}$ and sheet carrier density of 1.4×10^{13} cm^{-2}.[41]

Table 2 shows that, at $V_G = 0$ V, ZrO_2 MOSHFET mobility is least affected by temperature change. The ZrO_2 MOSHFET mobility drops by <40% from RT mobility where all other oxides' mobility drops by up to ≈60% of RT mobility. In contrast, in the depleted channel condition, TiO_2 is least affected by temperature. The mobility is decreased by ≈17% whereas in other MOSHFETs, it reduces by up to ≈85%. Thus, the mobility in MOSHFETs with a higher density of oxide charges (Q_{ox}) is less affected by increase in temperature.

Table 2. Summary of electron mobility variation with temperature for different dielectrics.

	RT mobility at $V_G = 0$ V [$cm^2 V^{-1} s^{-1}$]	250 °C mobility at $V_G = 0$ V [$cm^2 V^{-1} s^{-1}$]	RT mobility at depleted channel [$cm^2 V^{-1} s^{-1}$]	250 °C mobility at depleted channel [$cm^2 V^{-1} s^{-1}$]
HFET	207	87 (58% drop)	1188	188 (84% drop)
Al_2O_3	293	146 (50% drop)	641	240 (62% drop)
ZrO_2	191	118 (38% drop)	554	267 (51% drop)
TiO_2	233	125 (46% drop)	473	388 (17% drop)

The carrier mobility, μ, increased with more negative gate voltage, i.e., as the carrier concentration decreases (see inset of Figure 3a–c). This N_s dependence implies the presence of phonon scattering.[42] The temperature dependence of the MOSHFET channel electron mobility follows a power law $\mu \approx T^{-\alpha}$, with α varying between 1 and 3, further supporting phonon scattering as the dominant mobility limiting process.[43] We exclude the possibility of roughness scattering as the epilayer roughnesses were measured to be <1 nm rms. However, alloy scattering cannot be conclusively excluded, we note that it will be similar for all the gate dielectrics, given that the samples were cut from the same epitaxial wafer. We ascribe the small variations in μ, and in the temperature dependence, between the different dielectrics to ionized impurity/Coulomb scattering, from charge introduced at the oxide/AlGaN barrier interface. The presence of this charge is shown in Table 1 and is reflected in the threshold voltage shift.

4. Conclusions

In summary, we report on room temperature up to 250 °C operation of UWBG MOSHFETs with ALD high-k gate dielectrics TiO_2, Al_2O_3, and ZrO_2. These devices show gate leakage reduction by four orders of magnitude as well as a positive shift of the threshold voltage as high as 4 V, as compared with similar geometry HFETs. The devices show stable *I–Vs* in the aforementioned temperature range with weak dependence of gate leakage on temperature. The peak drain current reduces from $\approx 0.5\ \mathrm{A\,mm^{-1}}$ at room temperature to $\approx 0.3\ \mathrm{A\,mm^{-1}}$ at 250 °C. We attribute this reduction to mobility–temperature dependence, as the carrier concentration was found nearly temperature independent. Our reported devices have excellent potential for use as high-temperature power electronic devices.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

$Al_{0.65}Ga_{0.35}N/Al_{0.4}Ga_{0.6}N$ metal oxide semiconductor heterostructure field effect transistors, high-*k* atomic layer-deposited oxides, high temperatures, temperature-dependent mobilities, threshold voltages

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[1] S. Hashaimoto, K. Akita, Y. Yamamoto, M. Ueno, T. Nakamura, N. Yafune, K. Sakuno, H. Tokuda, M. Kuzuhara, K. Takeda, M. Iwaya, H. Amano, *Phys. Status Solidi C* **2012**, *9*, 373.
[2] H. Tokuda, M. Hatano, N. Yafune, S. Hashimoto, K. Akita, Y. Yamamoto, M. Kuzuhara, *Appl. Phys. Express*, **2010**, *3*, 121003.
[3] N. Yafune, S. Hashimoto, K. Akita, Y. Yamamoto, H. Tokuda, M. Kuzuhara, *Electron. Lett.* **2014**, *50*, 211.
[4] H. Hahn, B. Reuters, H. Kalisch, A. Vescan, *Semicond. Sci. Technol.* **2013**, *28*, 074017.
[5] S. Bajaj, T. H. Hung, F. Akyol, D. Nath, S. Rajan, *Appl. Phys. Lett.* **2014**, *105*, 263503.
[6] J. Xie, S. Mia, R. Dalmau, R. Collazo, A. Rice, J. Tweedie, Z. Sitar, *Phys. Status Solidi C* **2011**, *8*, 2407.
[7] S. Mollah, M. Gaevski, K. Hussain, A. Mamun, R. Floyd, X. Hu, M. V. S. Chandrashekhar, G. Simin, A. Khan, *Appl. Phys. Express* **2019**, *12*, 074001.
[8] S. Muhtadi, S. M. Hwang, A. Coleman, F. Asif, G. Simin, M. V. S. Chandrashekhar, A. Khan, *IEEE Electron Device Lett.* **2017**, *38*, 914.
[9] W. C. Lien, N. Damrongplasit, J. H. Paredes, D. G. Senesky, T. J. K. Liu, A. P. Pisano, *IEEE J. Electron Devices Soc.* **2014**, *2*, 164.
[10] R. Menozzi, S. Member, G. A. Umana-membreno, B. D. Nener, G. Parish, G. Sozzi, L. Faraone, U. K. Mishra, *IEEE Trans. Device Mater. Reliab.* **2008**, *8*, 255.
[11] K. X. Sun, presented at CLEO: 2011 – Laser Applications to Photonic Applications, Baltimore, MD, May **2011**.
[12] J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, N. M. Johnson, K. A. Jones, R. J. Kaplar, S. Rajan, C. G. Van de Walle, E. Bellotti, C. L. Chua, R. Collazo, M. E. Coltrin, J. A. Cooper, K. R. Evans, S. Graham, T. A. Grotjohn, E. R. Heller, M. Higashiwaki, M. S. Islam, P. W. Juodawlkis, M. A. Khan, A. D. Koehler, J. H. Leach, U. K. Mishra, R. J. Nemanich, R. C. N. Pilawa-Podgurski, J. B. Shealy, Z. Sitar, M. J. Tadjer, A. F. Witulski, M. Wraback, J. A. Simmons, *Adv. Electron. Mater.* **2018**, *4*, 1600501.
[13] R. J. Kaplar, A. A. Allerman, A. M. Armstrong, M. H. Crawford, J. R. Dickerson, A. J. Fischer, A. G. Baca, E. A. Douglas, *ECS J. Solid State Sci. Technol.* **2017**, *6*, Q306.
[14] A. G. Baca, A. M. Armstrong, A. A. Allerman, E. A. Douglas, C. A. Sanchez, M. P. King, M. E. Coltrin, T. R. Fortune, R. J. Kaplar, *Appl. Phys. Lett.* **2016**, *109*, 33509.
[15] S. Bajaj, F. Akyol, S. Krishnamoorthy, Y. Zhang, S. Rajan, *Appl. Phys. Lett.* **2016**, *109*, 133508.
[16] S. Muhtadi, S. Hwang, A. Coleman, F. Asif, A. Lunev, M. V. S. Chandrashekhar, A. Khan, *Appl. Phys. Lett.* **2017**, *110*, 171104.
[17] S. Muhtadi, S. M. Hwang, A. L. Coleman, A. Lunev, F. Asif, V. S. N. Chava, M. V. S. Chandrashekhar, A. Khan, *Appl. Phys. Express* **2017**, *10*, 011004.
[18] S. Muhtadi, S. Hwang, A. Coleman, F. Asif, A. Lunev, M. V. S. Chandrashekhar, A. Khan, *Appl. Phys. Lett.* **2017**, *110*, 193501.
[19] A. Owens, A. Peacock, *Nucl. Instrum. Methods Phys. Res.* **2004**, *531*, 18.
[20] P. H. Carey, F. Ren, A. G. Baca, B. A. Klein, A. A. Allerman, A. M. Armstrong, E. A. Douglas, R. J. Kaplar, P. G. Kotula, S. J. Pearton, *J. Electron Devices Soc.* **2019**, *7*, 444.
[21] R. Gaska, M. Gaevski, R. Jain, J. Deng, M. Islam, G. Simin, M. Shur, *Solid-State Electron.* **2015**, *113*, 22.
[22] X. Hu, S. Hwang, K. Hussain, R. Floyd, S. Mollah, F. Asif, G. Simin, A. Khan, *IEEE Electron Device Lett.* **2018**, *39*, 1568.
[23] V. Adivarahan, S. Rai, N. Tipirneni, A. Koudymov, J. Yang, G. Simin, M. A. Khan, *Appl. Phys. Lett.* **2006**, *88*, 182507.
[24] Q. Fareed, V. Adivarahan, M. Gaevski, T. Katona, J. Mei, F. A. Ponce, A. Khan, *Jpn. J. Appl. Phys.* **2007**, *46*, L752.
[25] N. Y. Garces, D. J. Meyer, V. D. Wheeler, Z. Liliental-Weber, D. K. Gaskill, C. R. Eddy, *J. Vac. Sci. Technol. B* **2013**, *32*, 03D101.
[26] J. P. Niemelä, G. Marin, M. Karppinen, *Semicond. Sci. Technol.* **2017**, *32*, 093005.
[27] D. Wei, T. Hossain, N. Y. Garces, N. Nepal, H. M. Meyer, M. J. Kirkham, C. R. Eddy, J. H. Edgar, *ECS J. Solid State Sci. Technol.* **2013**, *2*, N110.
[28] T. J. Anderson, V. D. Wheeler, D. I. Shahin, M. J. Tadjer, A. D. Koehler, K. D. Hobart, A. Christou, F. J. Kub, C. R. Eddy, *Appl. Phys. Express.* **2016**, *9*, 071003.
[29] H. Jiang, C. W. Tang, K. M. Lau, *IEEE Electron Device Lett.* **2018**, *39*, 405.
[30] C. R. English, V. D. Wheeler, N. Y. Garces, N. Nepal, A. Nath, J. K. Hite, M. A. Mastro, C. R. Eddy, *J. Vac. Sci. Technol. B* **2013**, *32*, 03D106.
[31] D. I. Shahin, T. J. Anderson, A. Christou. *ECS Trans.* **2017**, *80*, 139.
[32] J. R. Avila, S. B. Qadri, J. A. Freitas, D. R. Boris, S. G. Walton, C. R. Eddy, V. D. Wheeler, *Chem. Mater.* **2019**, *31*, 3900.
[33] S. Rai, V. Adivarahan, N. Tipirneni, A. Koudymov, J. Yang, G. Simin, M. A. Khan, *Jpn. J. Appl. Phys.* **2006**, *45*, 4985.
[34] M. A. Khan, G. Simin, J. Yang, J. Zhang, A. Koudymov, M. S. Shur, R. Gaska, X. Hu, A. Tarakji, *IEEE Trans. Microwave Theory Tech.* **2003**, *51*, 624.

[35] S. M. Sze, K. K. Nag, *Physics of Semiconductor Devices*, Wiley, New York, NY **2006**.

[36] S. Mollah, M. Gaevski, M. V. S. Chandrashekhar, X. Hu, V. Wheeler, K. Hussain, A. Mamun, R. Floyd, I. Ahmad, G. Simin, C. Eddy, A. Khan, *Semicond. Sci. Technol.* **2019**, *34*, 125001.

[37] A. M. Ionescu, H. Riel, *Nature* **2011**, *479*, 329.

[38] R. J. Kaplar, A. A. Allerman, A. M. Armstrong, M. H. Crawford, J. R. Dickerson, A. J. Fischer, A. G. Baca, E. A. Douglas, *ECS J. Solid State Sci. Technol.* **2017**, *6*, Q3061.

[39] M. E. Levinshtein, P. A. Ivanov, M. Asif Khan, G. Simin, J. Zhang, X. Hu, J. Yang. *Semicond. Sci. Technol.* **2003**, *18*, 666.

[40] A. G. Baca, B. A. Klein, J. R. Wendt, S. M. Lepkowski, C. N. Nordquist, A. M. Armstrong, A. A. Allerman, E. A. Douglas, R. J. Kaplar, *IEEE Electron Device Lett.* **2019**, *40*, 17.

[41] B. A. Klein, E. A. Douglas, A. M. Armstrong, A. A. Allerman, V. M. Abate, T. R. Fortune, A. G. Baca, *Appl. Phys. Lett.* **2019**, *114*, 112104.

[42] X. Z. Dang, P. M. Asbeck, E. T. Yu, G. J. Sullivan, M. Y. Chen, B. T. McDermott, K. S. Boutros, J. M. Redwing, *Appl. Phys. Lett.* **1999**, *74*, 3890.

[43] A. Aminbeidokhti, S. Dimitrijev, A. Kumar Hanumanthappa, H. A. Moghadam, D. Haasmann, J. Han, Y. Shen, X. Xu, *IEEE Trans. Electron Devices* **2016**, *63*, 1013.