

4.4 A 28/37GHz Scalable, Reconfigurable Multi-Layer Hybrid/Digital MIMO Transceiver for TDD/FDD and Full-Duplex Communication

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This paper describes an advanced mm-wave MIMO transceiver with several innovative attributes. It introduces a multi-layer hybrid/digital MIMO architecture that comprises multiple tiles having fully connected (FC) RF-domain complex-weights in the first layer, followed by fully connected (analog or digital) baseband layer(s). This architecture mitigates complexity versus spectral-efficiency trade-offs of hybrid MIMO architectures (Fig. 4.4.1), and enables efficient upward scaling in the number of MIMO streams. The architecture can be configured into numerous multi-layer hybrid MIMO modes comprising FC or partially-connected (PC) RF tiles, or as the front-end of a fully digital MIMO array, or as a conventional phased-array [1]. Another important contribution of this paper is the demonstration of full-duplex (FD) multi-antenna communication, enabled by on-chip self-interference cancellation (SIC). In the RX path, the MIMO transceiver features three-step successive SIC with a per-element SIC step that cancels TX leakage in the RF domain independently for each element. It is important to note that such SIC is available only with tiles that have FC in the first layer. To realize autonomous SIC, an on-chip adaptation engine is implemented that optimally sets SIC weights for each element using a time-multiplexed least-mean square (LMS) algorithm.

Figure 4.4.1 shows signal-flow graph representations of several MIMO architectures. The single-layer PC architecture (H1) is equivalent to having a phased-array for each MIMO stream, but the price paid for its simplicity is that each stream is connected to only a subset of the antenna elements, which results in reduced per-stream beamforming gain. On the other hand, FC MIMO architectures (H2 [2,3], H4) achieve higher per-stream beamforming gain, but the complexity of single-layer FC MIMO architecture (H2) scales prohibitively with the number of antenna elements/streams.

Our scalable multi-layer MIMO architecture, similar to H4, uses K single-layer FC tiles, each connected to N_A/K antennas. Each FC tile comprises RF-domain complex weights in the first layer, N_{RF} up/downconversion chains, and a second layer of fully connected processing from N_{RF} baseband signals to N_S streams. In contrast to the single-layer FC architecture H2, our multi-layer architecture retains low complexity with increasing N_S . Also, its spectral-efficiency approaches that of digital MIMO architecture for the same N_S .

An intuitive understanding of two-layer MIMO operation can be gained from Fig. 4.4.2, which shows a two-layer/PC tile architecture with $N_A=8$, $K=2$ and $N_{RF}=N_S=2$. In each PC tile, the weights are set to synthesize a composite array pattern having two "main" lobes directed towards the incoming streams S_1 and S_2 . The first layer improves the SNR of both streams but does not provide any cross-stream isolation. Then, in the fully connected second layer, the weights can be set to achieve cross-stream cancellation, thereby allowing high-SNR reception of each stream. Thus, the second layer helps to achieve nearly the entire beamforming gain available from the aperture for each stream.

Replacing PC tiles with FC [2,3] tiles confers numerous advantages that have not been previously appreciated. First, as shown in Fig. 4.4.2 (inset), an FC tile can accommodate a higher number of streams (i.e., up/downconversion chains), with each stream having the same SNR as in the case of the PC tile. Second, each FC tile can accommodate streams occupying different channels or bands [3], thereby enabling carrier-aggregation (CA). Third, the FC tile enables front-end SIC, which is essential for FD communication.

Figure 4.4.3 shows a schematic of our MIMO transceiver. The first layer comprises two four-element/two-stream FC tiles that interface to four homodyne up/downconversion chains (i.e., $N_A=8$, $K=2$, $N_{RF}=4$, $N_S=4$). The Cartesian-combining technique [4] has been extended for bi-directional (TX+RX) complex-weighting and splitting/combining. Based on programmable-gain amplifiers (PGAs) and complex-quadrature mixers, this technique is easily adapted to dual-band operation. Each up/downconversion chain can independently select either 28 or 37GHz LO; hence, each FC tile can operate in either band. Our transceiver is reconfigurable as a digital MIMO front-end supporting the same number of elements ($N_{RF}=8$ here).

Front-end circuits in the first layer extensively use coupled-resonator designs (Z_{11} and Z_{21}) for dual-band 28/37GHz operation. Switching between TX and RX is achieved by using bi-directional PGA cells that avoid the use of explicit RF signal-path switches. Each of the N_A RF inputs/outputs is connected to a compact circuit containing a two-way power-combining PA, a three-stage CG LNA and a wideband TX/RX switching network [5]. These circuits are followed by bi-directional 5-bit complex-weights and a splitting/combining network [3] that also uses coupled resonators. The architecture, together with the use of extensive passive component reuse between TX and RX results in a compact footprint. The analog baseband second layer employs PGA-based Cartesian weights.

The 8-element 65nm CMOS chip (2.3x5.5mm², Fig. 4.4.7) is mounted on a probe station. For on-air testing, chip inputs are connected to a linear PCB patch antenna array mounted directly on the RF probe. Each element achieves 44/37dB RX gain, 7.9/8.8dB RX NF, 43.5/40dB TX gain, 15.5/15.6dBm P_{SAT} and 21.7/22.5% peak PA efficiency in 28/37GHz bands (Fig. 4.4.4). Measured on-air four-element ULA patterns are shown in Fig. 4.4.4 for angles between -50° and 50°.

Next, on-air MIMO operation with 4-ULA is characterized in three configurations C1-C3 (Fig. 4.4.5). The chip is configured to simultaneously receive two independent modulated signals transmitted using horn antennas from 0° and 30° relative to the RX array. Weights are first computed knowing the TX locations in order to steer beam/null towards desired/undesired TX, and then applied to the chip. The measured pattern (Fig. 4.4.5) matches theory in all configurations. As seen in the constellations in Fig. 4.4.5, the two co-channel streams are decoded with high EVM by the two downconversion chains. The multi-layer PC configuration (C3) is seen to achieve similar per-stream beamforming gain and EVM to the single-layer FC configuration (C1). This showcases the advantage of multi-layer MIMO processing. As discussed earlier, multi-layer MIMO with FC tiles further increases performance (i.e., number of streams) and enables CA and FDD/FD.

The transceiver can be configured for FD operation as follows: In each FC tile, two of the four elements are configured in TX mode and the other two in RX mode (Fig 4.4.6). In each RX element, two independent complex weights are available, of which one can be used as the RX beamforming weight, and the other can be used for SIC. SI leakage is canceled in three steps: (1) A copy of the TX signal is complex-weighted by the latter weight mentioned above, and injected into the LNA output node in each element in the RX path. This SIC step is most important as it cancels leakage closest to the input of the RX chain. Such SIC can only be implemented in the FC tile. An on-chip mixed-signal LMS loop updates the SIC weight sequentially for each element. (2) In the second SIC step, RX weights are set such that TX leakage is minimized via beam/null-forming. (3) In the third SIC step, another cancellation signal can be injected at the input of the downconversion stage. A delayed version of the original TX signal can be used to cancel out any SI copies that have large group delay. Additional SIC can be achieved in the digital domain. Figure 4.4.6 shows the SIC achieved across RF bandwidth with the three steps. Over 25(20)dB cancellation is achieved for 100(300)MHz RF bandwidth. For 30dB of TX-to-RX antenna isolation, the baseband output is dominated by TX-SI w/o the canceller ON (Fig. 4.4.6). The desired RX signal can be recovered by turning ON the three-step SIC. The on-chip LMS loop takes 20 to 40 baseband cycles per element to adapt optimal SIC weights. Benchmarking against [1-3,5] is shown in Fig. 4.4.7.

Acknowledgements:

This work was supported in part by the National Science Foundation under grant CRI-1823235.

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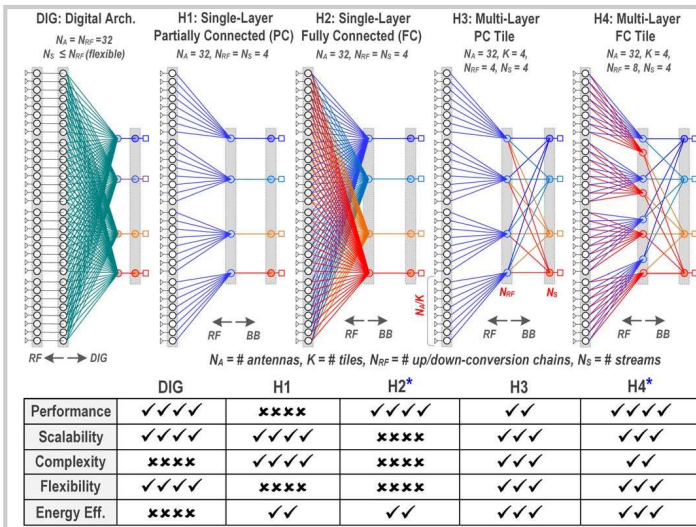


Figure 4.4.1: MIMO transceiver architectures: Performance, scalability and complexity.

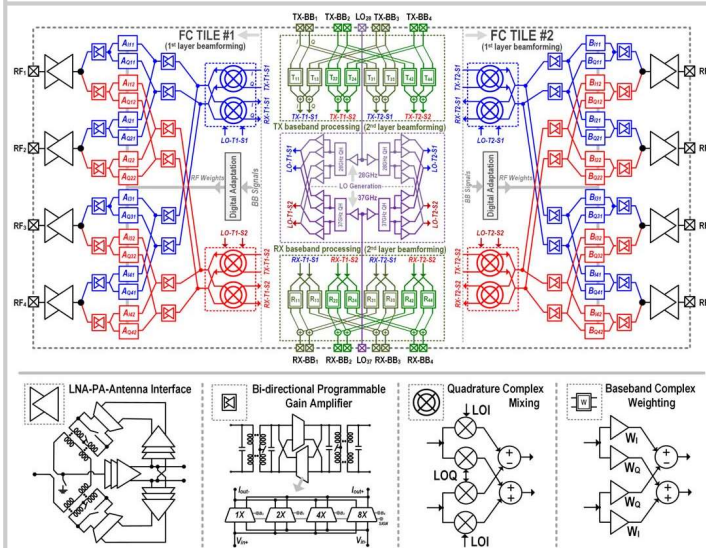


Figure 4.4.3: Simplified schematic of multi-layer hybrid beamforming transceiver prototype chip (top); Constituent circuit blocks (bottom).

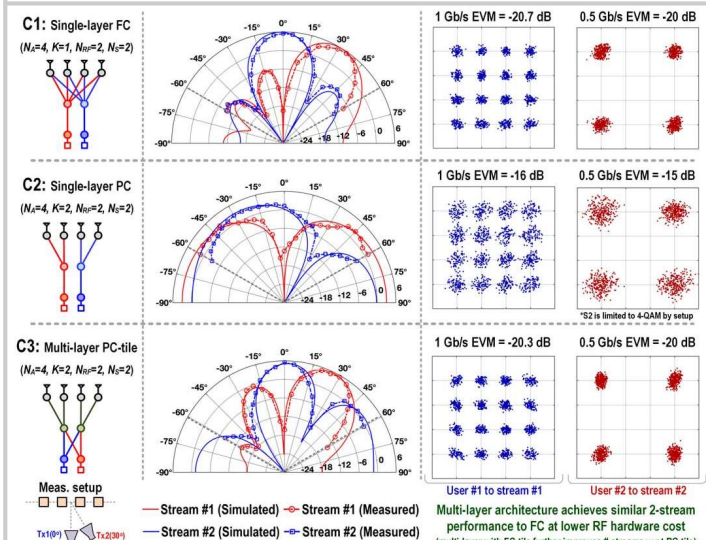


Figure 4.4.5: Characterization of two-stream MIMO receiver for four-element single-layer FC/PC and multi-layer PC architecture.

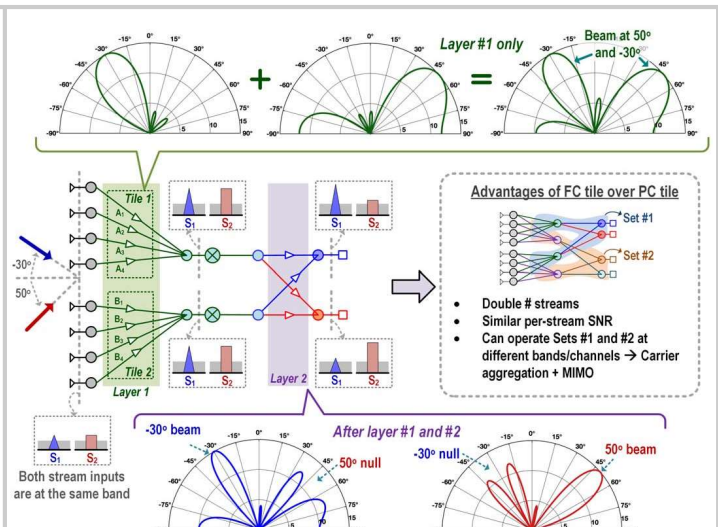


Figure 4.4.2: Multi-layer MIMO concepts: Mechanism of each layer and advantages of FC over PC.

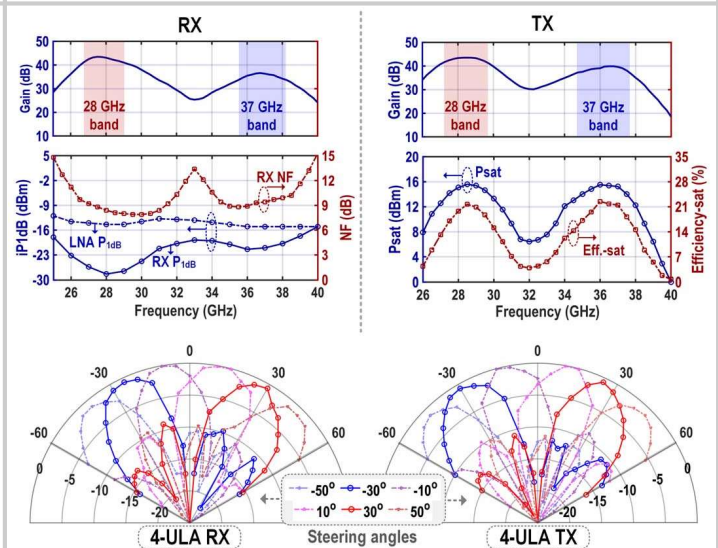


Figure 4.4.4: Single-element 28/37 GHz RX and TX characterization (top); Beam pattern measurements for four-element RX and TX beamsteering (bottom).

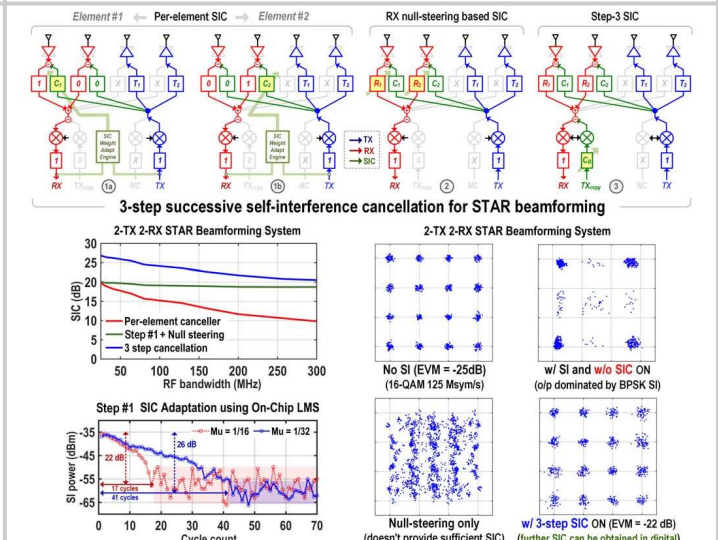
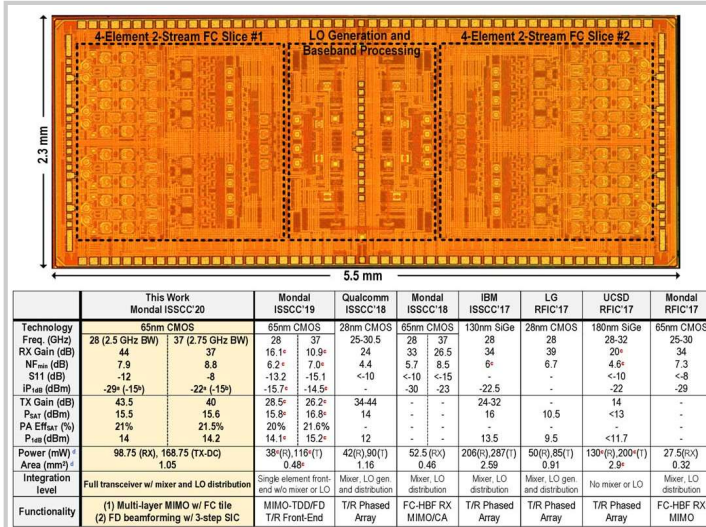


Figure 4.4.6: 3-step SIC for FD beamforming (top); Measured SIC in 2-TX 2-RX configuration and LMS adaptation for step #1 SIC (bottom).



^a full RX path, ^b LNA only, ^c Excluding up/down-conversion, ^d Estimated for per-element per-stream,

Figure 4.4.7: Die micrograph (top); Comparison against state-of-the-art beamformers (bottom).