1024-Electrode Hybrid Voltage/Current-Clamp Neural Interface System-on-Chip with Dynamic Incremental-SAR Acquisition

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Abstract

We present a neural interface system-on-chip (NISoC) with 1,024 channels of simultaneous electrical recording and stimulation for high-resolution high-throughput electrophysiology. The 2mm × 2mm NISoC in 65nm CMOS integrates a 32 × 32 array of electrodes vertically coupled to analog front-ends supporting both voltage and current clamping through a programmable interface, ranging over 100dB in voltage and 120dB in current, with $0.82\mu W$ power per channel at $5.96\mu V_{rms}$ input-referred voltage noise from DC to 12.5kHz signal bandwidth. This includes on-chip acquisition with a back-end array of 32 dynamic incremental SAR ADCs for 25Msps 11-ENOB acquisition at 2fJ/level FOM.

Introduction

The vast majority of integrated neural interfaces to date are limited to recording electrical potentials [1–4], while some are capable of simultaneous current stimulation through the same electrodes, implementing basic functionality of current-clamp electrophysiology [5]. However, few offer simultaneous current recording and voltage stimulation capabilities for voltage-clamp electrophysiology [6], essential to characterize ion currents through membranes, as well as voltammetry to measure redox currents from neurotransmitter electrochemical activity.

A conventional SAR ADC is most efficient for full-Nyquist memory-less, uniformly distributed signals, but is a poor match for typical neural (such as spike, local field potential LFP, and electrocorticogram ECoG) signals that are mostly very small in amplitude with substantial low-frequency content and infrequent large fast transients. To this end, an LSB-first SAR was proposed to increase energy efficiency [7]. Despite several advantages, the main drawback of the LSB-first SAR technique is that the number of cycles per conversion depends on the previous signal amplitude, and could be very long even for subtle (LSB-level) changes.

NISoC and *i*SAR Architecture

Here we present an integrated silicon neural interface system-on-chip (NISoC) that includes an on-chip ADC covering the entire frequency range of neural biopotentials from LFPs to action potentials, while providing fully configurable simultaneous electrical stimulation capability. The NISoC supports voltage and current clamping through a programmable interface (Fig. 1). Dedicated circuits underneath each electrode serve either current or voltage clamp functions from the local scalar coefficient and the global signal waveform (Fig. 1 top right). Global control variables also configure gain and bandwidth for either voltage or current recording, generating a proportional voltage output. One 12-b SAR ADC digitizes the 32 outputs in a column.

To cover wider signal range without compromising energy efficiency of signal dependent LSB-first SAR ADC [7], we here consider another strategy, dynamic incremental SAR (*i*SAR) with adaptive start index and overflow protecting circuit. It starts from the previous conversion level rather than mid-level, and proceeds from thereon with a smaller step, at a radix-2 scale index lower than MSB − 1 (Fig. 1, bottom right). If the sampled input is sufficiently close to the previous conversion level (blue traces), then the *i*SAR search continues to successively zoom in with the index stepping down each time the comparator flips, reaching the LSB in a number of cycles typically less than the number of bits, less than needed for conventional or LSB-first SAR ADC. If the input changes from its previous level to a greater extent (greater in step than the radix-2 scale of the start index), the search requires zoom-out operations to catch up, where the index undergoes upward excursions until the comparator flips to resume a downward settling trend towards the LSB (green dotted traces). *i*SAR is implemented using essentially the same hardware as the conventional SAR, except for a presettable indexed up/down counter [2] rather than a standard register, and additional index control logic (Fig. 1, right center). The control logic includes overflow protection avoiding the register to exceed the DAC range, otherwise causing DAC charge loss [7]. *i*SAR requires a frame memory buffer to store and recall 1,024 previous 12-b output values for preload in sequential scanned order; the negligible silicon area incurred by on-chip integration of a 12-kb buffer affords substantial energy savings beyond what is reported here.

Circuit Implementation

Circuit detail of the interface front-end circuit below each electrode is shown in Fig. 2. Current and voltage clamp functions are activated by analog switches controlled by local state variables based on local ternary coefficient and global signal waveform. Non-inverting voltage and integrating current amplification share a single folded double-cascode OTA (94dB open-loop DC gain at 500nA bias) with configurable capacitive feedback for gain and bandwidth control through global control variables. Analog switches directly in contact to the integrating node are centrally bulk-source connected for ultra-low leakage extending integration time for fA-range current acquisition. Unity gain, low-input capacitance buffering of the voltage output [8] is dynamically biased synchronous with time-multiplexed readout for substantial power savings with negligible kick-back noise. Measured voltage gain, bandwidth, and input-referred noise ($G = 60$) as a function of frequency are shown in Fig. 4.

System Characterization and Experimental Validation

Fig. 3 shows the measured performance of one ADC configured in SAR and *i*SAR modes, as a function of the number of cycles. *i*SAR requires choice of start index, the optimal value of which is signal dependent but can be dynamically tuned by tracking average peak consecutive level differences in the signal. For slowly varying signals, *i*SAR reaches higher ENOB than SAR (11.2 rather than 10.9), in less than half the number of cycles (fewer than 6 rather than 12). ENOB is defined here as the effective number of bits of the ideal quantizer producing the same SNDR as the measured output at the signal input level. As SAR energy per conversion is almost directly proportional to the number of cycles, the *i*SAR reaches an ADC FOM (measured ADC energy per conversion level at ENOB) more than twice lower than SAR (2fJ/level rather than 5fJ/level) for signals changing slower than 1mV/ms, typical of LFP, ECoG, dopamine, and other biopotential and electrochemical neural signals. Changes in these signals are frequently limited to a few levels only, so that a few cycles of LSB-level *i*SAR iteration help to boost signal-to-noise ratio beyond the quantization level.

Recording of pre-recorded spike data from a leech ganglion neuron, reconstituted to original amplitude and presented through an external electrode immersed in saline within an epoxy seal ring over the exposed depassivated top-metal electrode array, yields accurate reconstruction through the front-end ($G = 60$) and back-end even down to 3 *i*SAR cycles per conversion (Fig. 4 bottom right). Measured current extending from 30fA ($G = 60$, 1ms integration) to 100nA ($G = 1$, 5μs integration) at less than 1mV compliance, with loop-back recording of stimulation currents for self-calibration, are illustrated in Fig. 5. The NISoC micrograph and summary of key performance metrics are shown in Fig. 6, along with *in vitro* recordings from mice hippocampal brain slice. Stimulus evoked excitatory post-synaptic potentials (EPSP) in mice hippocampus validate versatile and biologically relevant functionality at high noise-energy efficiency.

References

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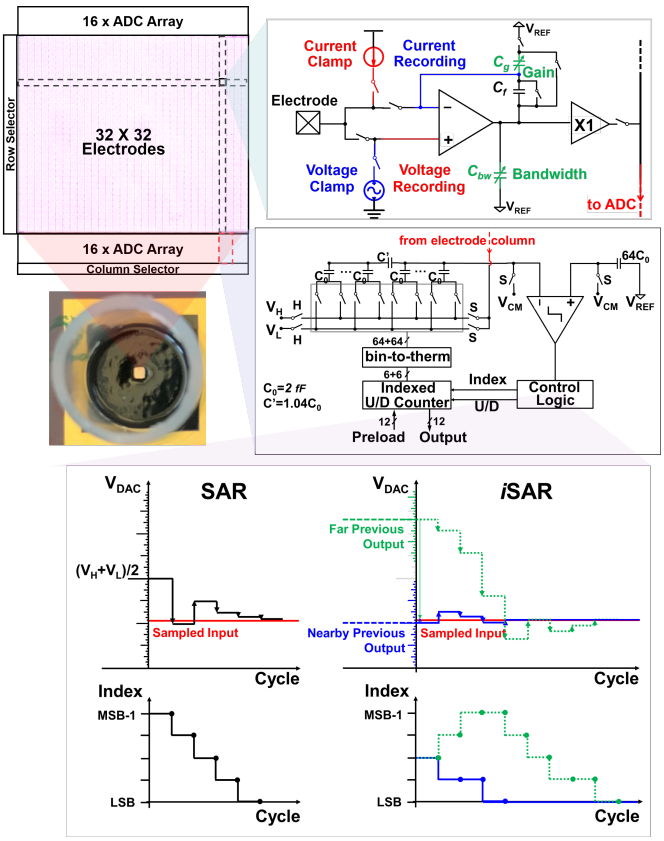


Fig. 1. Architecture of 1,024-electrode hybrid current/voltage-clamp neural interface-on-chip (NISoC), and operation of incremental SAR (*i*SAR) ADC.

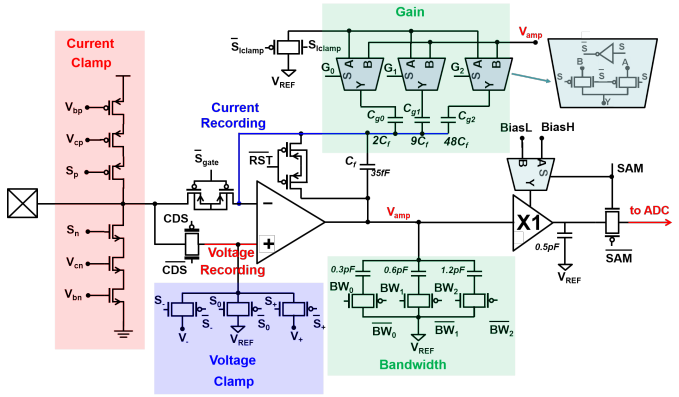


Fig. 2. Front-end circuit implementation.

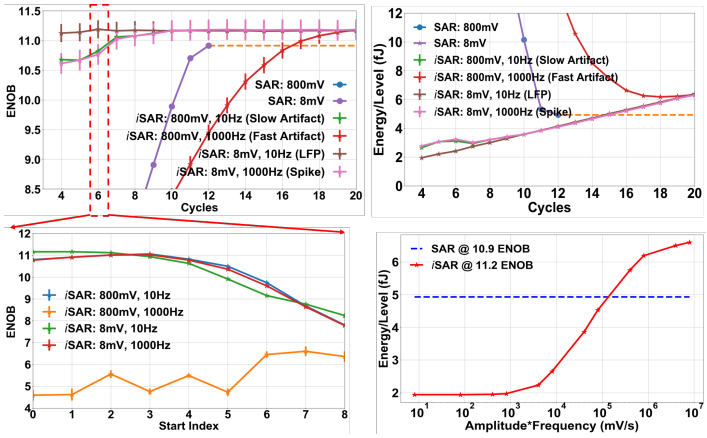


Fig. 3. Conventional SAR and incremental SAR (*i*SAR) ADC characterization: measured effective number of bits (ENOB) and ADC figure-of-merit (FOM).

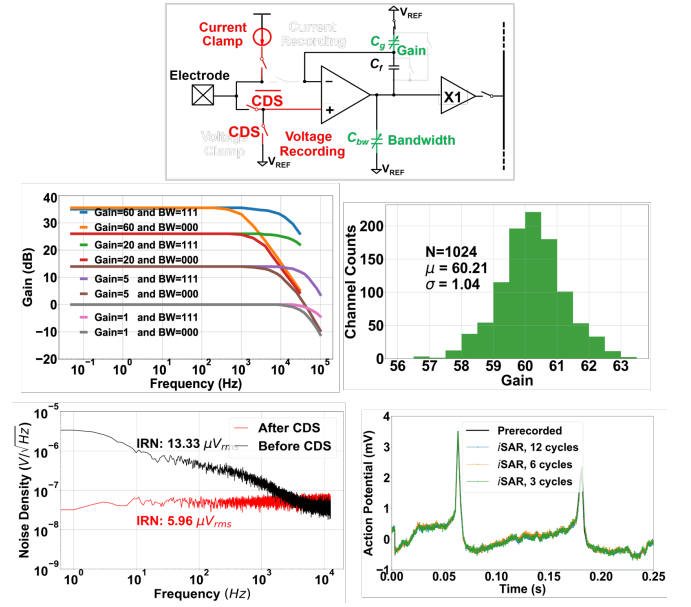


Fig. 4. Voltage recording mode characterization: measured gain, bandwidth, uniformity, input-referred noise, and pre-recorded spike neural data re-recorded through saline in contact with the electrodes, for different number of *i*SAR cycles per conversion.

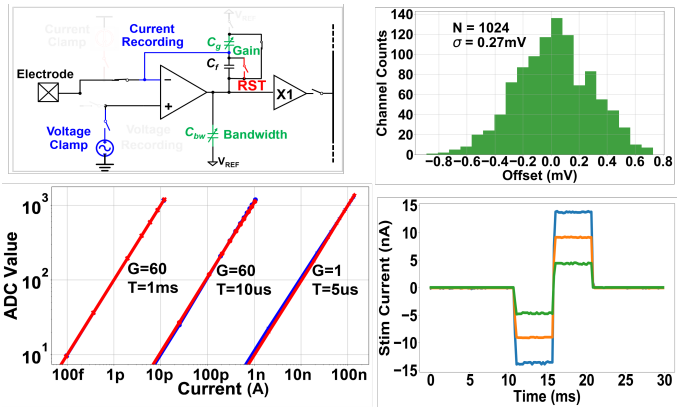
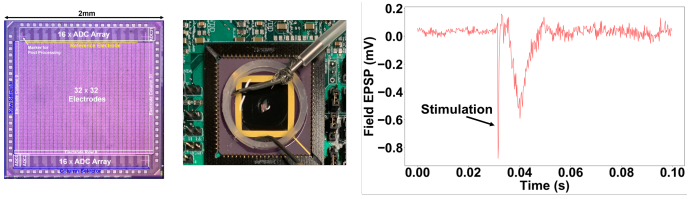


Fig. 5. Voltage clamp, current recording, and current clamp mode characterization: measured non-uniformity in voltage offset, range of current recording, and recording of self-calibrating current stimulation.



	ISSCC 07 [1]	ISSCC 18 [2]	JSSC 18 [3]	Neuralink 19 [4]	ISSCC 18 [5]	ISSCC 19 [6]	This Work
Technology (nm)	350	65	180	N/A	130	250	**65**
Supply Voltage (V)	3	0.8	1.8	N/A	N/A	N/A	**1.2**
Power/Ch (μW)	19.68	0.8	39 ~ 46	5.2 (analog)	95*	250	**0.82**
Number of Channels	256	16	144	256	1024	1024	**1024**
Area/Ch (mm^2)	0.04	0.024	0.0049	0.097	0.192	0.01	**0.0039**
Measurement	V	V	V	V	V	I (280fA ~ 12.5nA)	**V & I (30fA ~ 100nA)**
Stimulation	---	---	---	---	Yes (V & I)	---	**Yes (V & I)**
BW [Hz]	0.01- 5K	0.5- 500	0.5- 10K	3- 27K	0.5- 10K	100	**0.05-12.5K**
Input-referred Noise (μV_{rms})	7	0.99	9 ~ 19	5.9	12	---	**5.96**
Noise density (nV/√Hz)	99	44	190	59	120	N/A	**54**
NEF	9.94	1.81	37.66	N/A	N/A	N/A	**2.88 (after CDS)**
PEF	296.4	2.62	2552	N/A	N/A	N/A	**3.80**
ENOB (bits)	N/A	10.7	11 (resolution)	10 (resolution)	10	N/A	**11.2**

Fig. 6. Field excitatory post-synaptic potential (EPSP) recording of stimulation evoked action potential from mice hippocampal slice, and metric comparison with state of the art.