Controlling Silicon Bottom Cell Lifetime Variance in II-VI/Si Tandems

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***Abstract* — An intricate look is taken at the methods used to account for variance in minority-carrier lifetime in the silicon bottom cell of II-VI/Si tandem solar cells. A discussion on the modeling is provided. Lateral wafer variance is determined to be much less than wafer-to-wafer variance. Size testing indicates a minimum size of 4 × 4 cm is necessary for accurate results. The cleaning procedure and photoluminescence testing is described. Despite a small sample size, Si samples with CdTe deposition and $CdCl_2$ treatment maintain over 1 ms lifetimes, enabling the Si bottom cell in II-VI/Si tandem cells to reach state-of-the-art performance.**

***Index Terms* — II-VI, cadmium telluride, IZO, minority-carrier lifetime, multijunction, tandem**

I. Introduction

Accounting for and controlling the variance in the lifetimes of silicon wafers when conducting an experiment can be quite difficult. This difficulty can be compounded in the university lab setting, where the number of samples available is generally lower than an industrial setting, and the infrastructure cannot support the high volumes of processing that are seen in industry. This paper discusses in detail how this large amount of variance was controlled in the study by Tyler *et al.* [1], which analyzes the silicon degradation mechanisms and characteristics seen in the silicon bottom cell of II-VI/Si cells under the constraints of a very limited sample size. The lessons learned and best practices for controlling variance within the solar and silicon industries may help other small-scale labs conduct highly controlled experiments with confident outcomes when constrained by sample size.

The experiment in this study analyzes to what degree silicon lifetimes may degrade during II-VI top cell deposition, as well as why this degradation may occur. The need for tandem cells utilizing silicon is becoming more and more apparent as single-junction solar cells move closer to their Shockley-Queisser theoretical efficiency limits [2]. However, in many of the tandems that have been proposed and tried to date, degradation of the silicon bottom cell lifetime during tandem cell processing is a concern. This has been seen in III-V top cells and across different deposition methods. García-Tabarés *et al.* has studied the influence of III-V deposition on silicon morphology [3]. They also saw lifetime degradation seen in their silicon bottom cells during deposition, which they were able to recover in later processing steps [4], and have proposed three potential causes for this degradation [5]. Varache *et al.* [6] determined the cause of silicon lifetime degradation seen when fabricating their GaP/Si cells was most likely due to a fast diffusing impurity from their metal oxide chemical vapor deposition (MOCVD) chamber and devised a recovery process by doping their samples with phosphorous diffusion and chemically etching them in KOH. Martin *et al.* [7] investigated low-temperature passivation techniques for their III-V materials, yet it is expected that this may also reduce the silicon lifetime degradation. Ding *et al.* [8] saw similar degradation in their silicon bottom cells even when using a molecular beam epitaxy for III-V depositions, and devised a solution utilizing a sacrificial SiN layer that could be later etched off, leaving a high bulk silicon lifetime. Zhang *et al.* [9,10] further explored a SiN_x barrier to reduce extrinsic impurity diffusion, as well as gettering in n+ diffused layers, ultimately creating a 14.1% efficient GaP/Si solar cell. Ohlmann [11] investigated the use of a SiO_2/SiN_x diffusion barrier, achieving similar lifetimes.

Therefore, determining the precise amount of silicon lifetime degradation seen during II-VI deposition in Tyler *et al.* [1] is of utmost importance, and thus the variance in silicon lifetimes must be highly controlled, despite working with a small sample size.

II. Lateral vs. wafer-to-wafer variance

The first piece of vital information that must be understood is how the lateral lifetime variance on the silicon wafers compares to the wafer-to-wafer variance. This will vary from manufacturer to manufacturer, and the specific cleaning process used may affect this as well. For this experiment, the following variances are observed in Fig. 1.

The lateral lifetime was determined by dividing one wafer into a 4 × 4 matrix and measuring the lifetime of each square on a Sinton Instruments photoconductance decay (PCD) instrument after 50 nm of undoped amorphous silicon (a-Si) was deposited on both sides for surface passivation. The wafer-to-wafer lifetime was determined by measuring the lifetimes of 12 wafers processed through the same cleaning process within the same wafer holder. The lateral lifetime is demonstrated to be 2.13 ± 0.14 ms and the wafer-to-wafer lifetime is demonstrated to be 2.39 ± 0.50 ms, for these experimental sets. Therefore, ideally the controls and experimental conditions will

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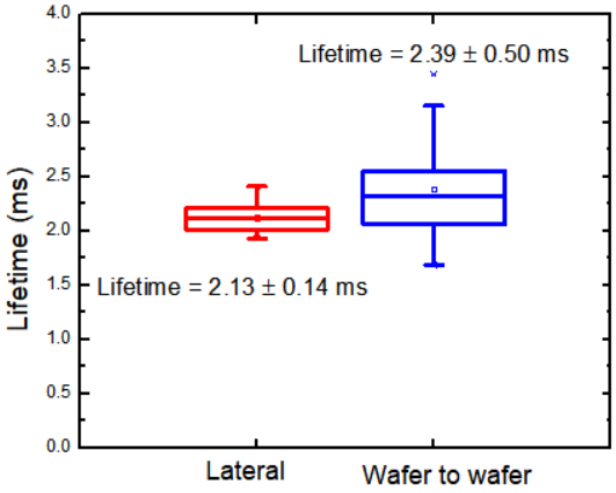

Fig. 1. Lifetime variance across a single wafer and from wafer to wafer.

be compared across lateral sections of a single wafer, rather than across multiple wafers, to minimize uncontrolled lifetime variance.

III. Wafer Size

Each wafer was divided into several sections to act as control and experimental pieces so that this larger wafer-to-wafer variance does not influence the results. This process can become risky when using lifetime testers, as the reported lifetime loses accuracy the smaller the wafer becomes. This was taken into account, and a minimum size of 4 × 4 cm was determined for the experiment, as seen in Fig. 2.

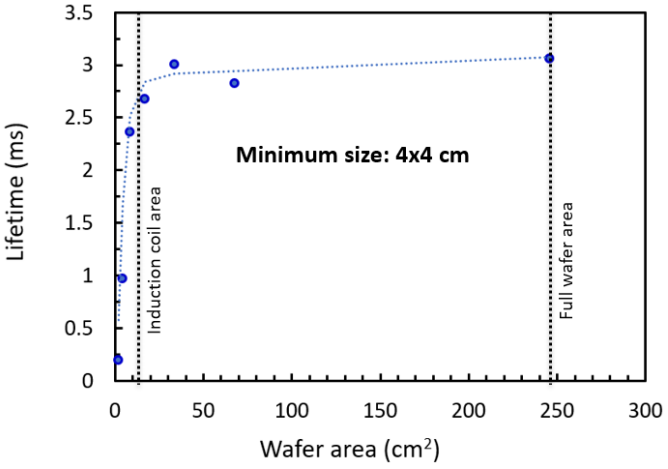

Fig. 2. Minimum wafer size determined to be 4 × 4 cm using the Sinton Lifetime Tester for measuring lifetimes.

IV. Modeling of Lifetime Effect on Efficiency

Modeling is done for a 1.1 eV silicon bottom cell and a 1.7 eV MgCdTe top cell at one sun (0.100 W/cm^2, AM1.5G) to extract what efficiencies can be achieved for varying silicon lifetimes, seen in Fig. 3.

(a)

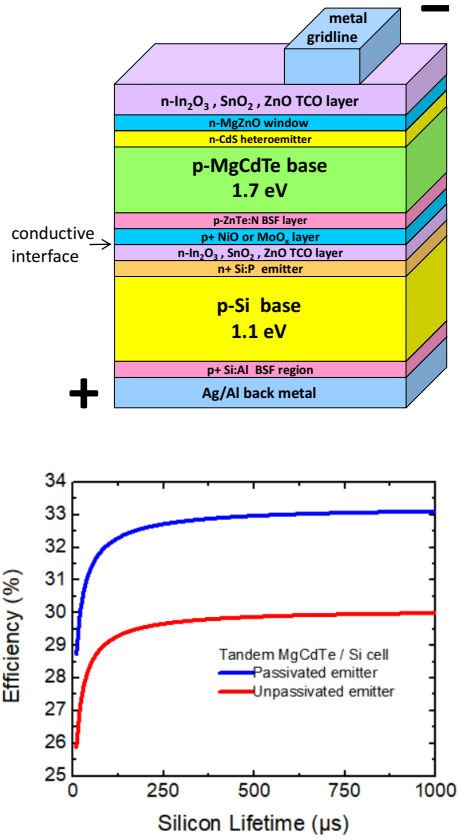

Fig. 3. (a) Cross-sectional schematic of an example MgCdTe/Si tandem solar cell. (b) Calculated tandem efficiencies for lifetimes between 0 and 1 ms for tandem MgCdTe/Si solar cells, with a passivated emitter surface recombination velocity (SRV) of 100 cm/s, and unpassivated emitter SRV of 1×10^5 cm/s.

In these calculations, the top and bottom cell are series connected in a 2-terminal tandem configuration. The emitter surface recombination velocity is set to 100 cm/s in the passivated case, while in the unpassivated case it is set to 1×10^5 cm/s. In both the passivated and unpassivatd cases, the surface recombination velocity at the back surface of the base is assumed to be 100 cm/s. In each case, the top cell is assumed to be current matched to the bottom cell. Efficiencies of up to 33% have been calculated for MgCdTe/Si tandem solar cells when silicon lifetimes are >500 µs, which is significantly higher than either cell could produce alone. After 1 ms the efficiency remains relatively the same. Therefore, 1 ms is an approximate threshold above which the silicon bottom cell base lifetime is high enough that 1) near state-of-the-art silicon cell

efficiencies can be reached, and 2) further increases in bulk lifetime have diminishing effects.

V. Cleaning and Control Procedure

The experimental goal is to determine how the variables of temperature, In_2O_3:ZnO (indium zinc oxide, or IZO) thickness between the Si and CdTe layers, and exposure to $CdCl_2$ treatment affect the state of lifetime degradation. With many variables being examined across a relatively small number of samples (due to deposition conditions and time constraints), it is important to ensure that any lifetime drops seen were a direct result of the cell structure and deposition conditions, and not a result of uncontrolled variables in the cleaning process and natural lifetime variance.

In order to reduce the amount of different cleaning runs, all wafers used in this study were cleaned in the same batch at the same time. This clean consisted of a piranha (3:1 H_2SO_4:H_2O_2) clean, KOH etch, and a RCA-B (1:1:6 HCl:H_2O_2:H_2O) clean [12]. Wafers were rinsed for 10 minutes in deionized water between each step. Once cleaned, the wafers were arranged in four groups, each undergoing differing thicknesses of IZO deposition (0 nm, 20 nm, 40 nm, and 60 nm).

Now, due to the lateral lifetime across wafers having less variance than the wafer-to-wafer lifetime, as seen in Section II, each wafer was cleaved into three separate sections: One to have no more processing done on it, serving as the control wafer; one to go through CdTe deposition by close spaced sublimation (CSS) at a specific temperature with no $CdCl_2$ treatment, and one to go through the same CdTe deposition temperature, but with the $CdCl_2$ treatment. Care was taken to make certain that each piece was larger than 4 × 4 cm, as determined in Section III. The silicon substrates were prepared and IZO DC sputter depositions were done in the Arizona State University (ASU) Solar Power Lab, and CdTe CSS depositions were done at Colorado State University (CSU) at 400°C, 450°C, and 500°C, bracketing the typical CdTe deposition temperature in this deposition system of 480°C. The wafers were then shipped back to ASU for lifetime testing.

To prepare for lifetime testing, the CdTe-deposited experimental samples went through a nitric-phosphoric acid etch (7:3:1 H_3PO_4:H_2O:HNO_3) to remove the CdTe and IZO layers. This was followed by another cleaning sequence of piranha etch and RCA-B solution. The samples were then etched in 6:1 NH_4F:HF buffered oxide etch (BOE) for 5 minutes to remove surface oxides immediately before passivating both front and back surfaces with 50 nm of undoped, hydrogenated amorphous silicon (a-Si:H) deposited by plasma enhanced chemical vapor deposition (PECVD). The baseline control Si wafers that did not have any CdTe deposition or $CdCl_2$ treatment, and had already received the initial KOH, RCA-B, piranha, RCA-B clean that all silicon samples had, were given a 5-minute BOE clean immediately prior to the standard 50 nm a-Si:H deposition to passivate both sides of the samples.

For each step in the cleaning process, it was important to process as many wafers as possible at a time in each solution in order to reduce variation that was seen when processing one sample at a time, which could be due to contamination. It was also important to include wafers with different experimental conditions (*e.g.*, not all 60 nm IZO thickness wafers in one batch) to ensure variation in the cleaning process was not mistaken for lifetime degradation due to one of the specific experimental variables.

Photoluminescence (PL) images were taken for each sample. Fig. 4 demonstrates how the uniformity of these images helped determine whether the source of lifetime degradation was induced by the experimental matrix of wafer treatments, or by a non-uniform contamination source.

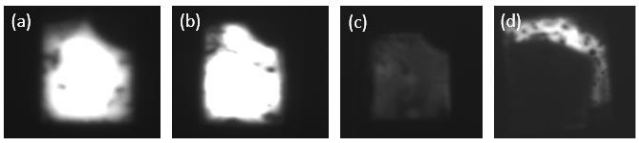

Fig. 4. (a) Control piece (lifetime (τ) = 2.55 ms), (b) experimental piece (τ = 3.24 ms), (c) experimental piece (τ = 0.230 ms), (d) experimental piece (τ = 0.168 ms). (a)-(c) were in the same batch, while (d) was in a separate batch.

The samples in Figs. 4a-4c were cleaned in the same wafer container at the same time. The control (a) showed a high lifetime and bright, uniform PL, as did one experimental piece (b). Another experimental piece (c) showed low lifetime, yet because the PL is uniformly dark, and (a) and (b) performed well, confidence could be high that it was due to the CdTe deposition process, rather than a cleaning error. Sample (d), which was in a separate batch from (a)-(c), is one example of a likely cleaning fault we encountered, due to the low overall lifetime measured on the sample coupled with a very dark section in the PL image (high recombination area) Data from this sample, as well as those from the same cleaning batch, were then assumed flawed and discarded.

VI. Silicon Lifetime Results

Despite the limited sample size, the focus on controls and documenting the variance allows for the determination that the $CdCl_2$ process itself causes the most degradation seen in the silicon, as can be seen in Fig. 5.

Compared to the baseline wafer lifetimes as well as the average lifetimes seen on the non-$CdCl_2$ samples, the lifetimes of those samples that went through $CdCl_2$ deposition are overall dampened. While the IZO thickness has a lesser effect, it does seem that at lower temperatures, a thicker IZO layer provides some protection against the degradation. While this trends slightly the other way at the higher temperatures, these values fall within the previously determined variance values and thus do not hold much merit. Temperature also, as expected, tends to lower the silicon lifetime as it increases.

While further, more extensive studies can be done for more conclusive results, this initial study points to the general trends seen across all three variables discussed with reasonable confidence given the natural variances established. These results are particularly exciting as lifetimes above 1 ms have

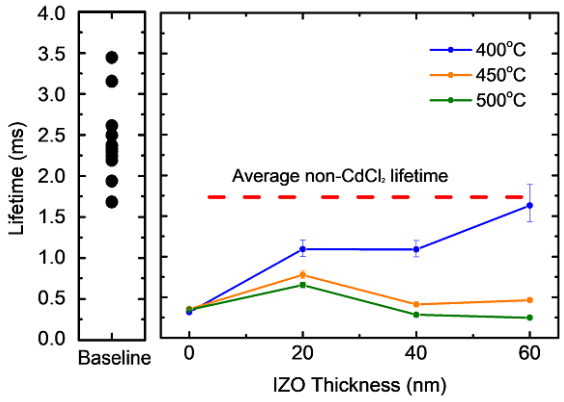

Fig 5. Lifetime results for the $CdCl_2$ treated samples at 400°C, 450°C, and 500°C at 0, 20, 40, and 60 nm IZO thickness. Baseline and non-$CdCl_2$ average lifetime included for comparison.

been established for silicon that is grown as a bottom cell in a II-VI/Si tandem. A more in-depth analysis involving the characterization on the samples used in this study, including diffusion modeling, defect energy levels, and secondary ion mass spectroscopy can be found in Tyler *et al.* [1]. Balancing the information learned here with optical and growth considerations should allow for a tandem II-VI/Si cell to push to the high efficiencies that have been theoretically modeled.

VII. Conclusion

In this paper, the considerations and care that must be taken to control and account for the variance in lifetimes that occurs within silicon wafers has been explained. While using the Tyler *et al.* [1] paper as an example to showcase these considerations, these best practices can be applied when designing many other experiments involving a limited sample size of photovoltaics. The lateral, wafer-to-wafer lifetimes, minimum size, and modeling are key considerations. Consistent controls are important to ensuring that data is not unduly influenced by small changes in the cleaning process and from batch to batch.

Due to these variation controls in the II-VI/Si study, despite a small sample size, there is confidence is arguing that high silicon lifetimes (>1 ms) can be maintained in silicon subcells in II-VI/Si tandem stacks. The $CdCl_2$ treatment step has the largest effect on an overall decrease in wafer lifetimes, while higher IZO thicknesses may preserve lifetime and higher temperatures will decreases lifetimes. These encouraging results were made possible due to these best practices in controlling variance, and it is the hope this paper will positively influence other labs design process when researching solar cell lifetimes using a limited sample size.

Acknowledgements

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