

Wideband Two-Way Hybrid Doherty Outphasing Power Amplifier

Chenyu Liang^{ID}, *Member, IEEE*, Jose I. Martinez-Lopez, *Member, IEEE*, Patrick Roblin^{ID}, *Senior Member, IEEE*, Yunsik Hahn^{ID}, *Graduate Student Member, IEEE*, Dominic Mikrut, *Graduate Student Member, IEEE*, and Vanessa Chen, *Member, IEEE*

Abstract—A new type of wideband dual-input hybrid Doherty outphasing power amplifier (HDO-PA) is developed in which the load-modulation scheme continuously converts as the frequency increase, from the previously reported HDO-PA mode with maximum flat efficiency response versus power to the conventional Doherty PA mode. For a symmetric HDO-PA implementation, this corresponds to the peak-to-backoff fundamental voltage ratio of the auxiliary amplifier linearly varying from 9/7 to 2 with frequency. A transmission-line-based wideband HDO-PA prototype is first established at the current-source reference planes to cover the frequency band from 1.4-GHz to 2.5-GHz. The wideband HDO-PA is implemented next at the package reference planes by synthesizing the wideband combiner circuit required to sustain the intrinsic load-modulation behavior across the entire frequency bandwidth. A 1.4-GHz to 2.5-GHz wideband HDO-PA is fabricated and characterized using both continuous-wave and modulated signals. The 6-dB backoff efficiency varies from 60% to 44% and the maximum power from 44.8 dBm to 42.9 dBm as the frequency increases. When the PA is excited with a 20 MHz bandwidth long-term evolution signal at 1.7 GHz with 6.5 dB peak-to-average-power ratio (PAPR), the PA achieves an average drain efficiency of 50.3% with -32.0 dBc adjacent-channel-power leakage ratio (ACLR) and an average drain efficiency of 47.8% with -54.0 dBc ACLR after digital predistortion linearization.

Index Terms—Doherty power amplifiers (DPA), outphasing power amplifiers (OPA), wideband power amplifiers.

I. INTRODUCTION

THE fifth generation of wireless communication (5G) infrastructure is designed to support communication systems with ultrafast data transmission rate and large capacity.

Manuscript received March 11, 2020; revised June 24, 2020; accepted August 4, 2020. This work was supported in parts by the NSF under Grant 1952907. The work of J. I. Martinez-Lopez was supported by the Programa de Apoyos para la Superación del Personal Académico de la UNAM (DGAPA-PASPA). This article is an expanded version from the IEEE MTT-S Radio and Wireless Week (RWW), San Antonio, TX, USA, January 26–29, 2020. (Corresponding author: Patrick Roblin.)

Chenyu Liang, Patrick Roblin, Yunsik Hahn, and Dominic Mikrut are with the Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210 USA (e-mail: roblin.1@osu.edu).

Jose I. Martinez-Lopez is with the Department of Electrical and Computer Engineering, The Ohio State University, Columbus, OH 43210 USA, and also with the Division de Ingeniería Eléctrica, Universidad Nacional Autónoma de México, Mexico City 04150, México.

Vanessa Chen is with the Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA 15213 USA.

Color versions of one or more of the figures in this article are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TMTT.2020.3019430

The 5G communication signals adopted rely on complex modulation schemes, exhibiting large peak-to-average power ratios (PAPR) and wide modulation bandwidth. To reduce the energy consumption in 5G wireless communication networks, power amplifiers (PAs) in transmitter systems should be designed to operate with high output power backoff efficiency and wide bandwidth.

Doherty power amplifiers (DPA) invented in [1] have been extensively explored and became amongst the most popular PA topologies for efficiently amplifying signals with large PAPR. The classical DPA is implemented with a quarter-wave ($\lambda/4$) transformer and a common load connecting the main and auxiliary amplifiers. A high average efficiency is achieved when the DPA is excited with signals exhibiting large PAPR, since the load impedance seen by the main transistor is dynamically modulated by the auxiliary drain currents from low- to high-power levels to maintain a constant drain voltage swing [2]–[7]. The conventional DPA architecture suffers from bandwidth limitation due to the narrowband $\lambda/4$ transformer used. In view of this limitation, there have been numerous efforts to extend the bandwidth of DPAs [8]–[13], [15]–[19], [48].

Outphasing power amplifiers (OPA) from [20]–[26] provide an alternative approach to perform load modulation and enhance backoff efficiency. The conventional voltage mode outphasing amplifier in [20] consists of two voltage sources connected differential to a common RF load. Two reactive components are added to compensate the reactance generated by the outphasing modulation. Mixed-mode OPA operation has been investigated in [24] and [25], in which both phase and amplitude of the PA input signals are modulated. It has been demonstrated that the mixed-mode OPA operation provides higher efficiency at backoff power level when compared with that of the conventional mode OPA. However like the conventional DPA, the OPA suffers from bandwidth limitation due to the narrow bandwidth characteristics of the conventional outphasing combiners.

A promising type of load modulation scheme that combines both the Doherty and outphasing operations into one PA design has been proposed [27]–[34]. This load modulation scheme benefits from both the Doherty and outphasing modes typically to maintain a high efficiency across a large backoff range. The wideband Doherty-outphasing PAs are of particular interest to this work. Andersson *et al.* [32] developed a dual-input

power amplifier based on a Doherty-outphasing continuum analysis. The optimal PA combiner solution which achieves the desired bandwidth performance is found in simulation. The incident power levels and outphasing angles applied to the two input ports of the PA are numerically swept in a systematic way to search for the best performance. This empirical optimization has been also adopted in several recent works [33] and [34]. In contrast to this empirical approach, a new approach to design the wideband hybrid Doherty outphasing power amplifier (HDO-PA) is presented in this work. It relies on the previously proposed Doherty-Chireix continuum theory reported in [30] and [31]. The wideband PA combiner is theoretically configured instead of using the numerical search approach used in [32]. The proposed design theory provides a systematic method to directly determine the dual-incident power levels and outphasing angles. This method also facilitates the PA characterization, since it is not necessary to conduct the four-dimensional experimental search associated with the joint dual-input power and phase sweeps for all frequencies.

The Doherty-Chireix continuum theory established in [30] is first reviewed and summarized here. The theory reported in [30] was established based on four current- and voltage-ratio factors: $K_{vm} = |V_{mp}|/|V_{mb}|$, $K_{va} = |V_{ap}|/|V_{ab}|$, $K_{im} = |I_{mp}|/|I_{mb}|$ and $K_{ia} = |I_{ap}|/|I_{ab}|$, where the subscripts m and a refer to the main and auxiliary PAs and the subscripts p and b refer to the peak and backoff power levels, respectively. Thereby, the factors $K_{vm/a}$ and $K_{im/a}$ refer to the peak-to-backoff fundamental drain voltage and current ratios, respectively. A continuum of solution for PA output combiners at the device current-source reference planes including the Doherty and Chireix outphasing modes was analytically derived in term of these ratio factors, which revealed the performance trade-off achieved by all of the possible PA combiners within the continuum of solution. An optimal PA design was found by choosing $K_{va} = \text{OBO}/(\text{OBO} - 2)$, where OBO refers to the output power backoff range. This mode of PA operation is referred to *hybrid Doherty maximum* (HDmax) PA in [30] and [31], inasmuch the efficiency drop between backoff and peak power level typically observed in the conventional Doherty PA is compensated and a maximum flat efficiency response versus output power can be obtained as is experimentally verified in [31]. Similarly with the approach in [31], the wideband HDO-PA combiner theory is established by setting $K_{vm} = 1$ (same drain voltages at peak and backoff) and $K_{ia} = \infty$ (auxiliary PA is off at backoff). However, compared with the work reported in [31], the main novelty of this work is that the K_{va} is now changing along with the frequency, which results in the PA mode of operation dynamically shifting versus frequency from the HDmax ($K_{va} = 9/7$) mode to the Doherty mode ($K_{va} = 2$) so as to maintain the desired backoff efficiency for a symmetric HDO-PA. The rationale for selecting these values of K_{va} is inspired in [30, Table I]. In this work, it has been found that the PA output combiner circuit can be physically realized when the asymmetry fundamental peak power ratio between the auxiliary and main amplifiers n is set to be 1 for all frequencies. At the minimum and maximum frequencies, $K_{va} = 9/7$ was obtained by selecting $\text{OBO} = 9$

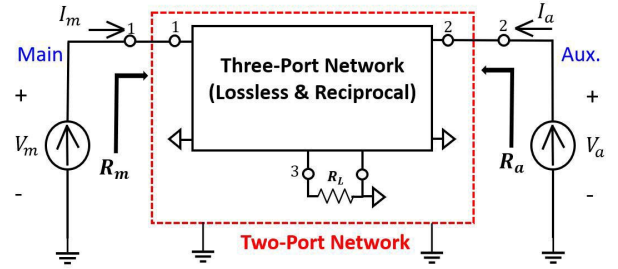


Fig. 1. Conceptual diagram for a wideband HDO-PA at the device current-source reference planes.

(9.54 dB) and $K_{va} = 2$ by selecting $\text{OBO} = 4$ (6 dB) for the HDmax and Doherty PAs respectively, as will be explained in further details in the following sections. This wideband combiner theory based on K_{va} is first verified in simulation at the current-source reference planes of the transistors, using an ideal equation-based output combiner. The wideband combiner at the package reference planes is then approximately realized by incorporating the device's output parasitic. Finally, to validate the proposed theory, the fabricated wideband HDO-PA is measured from 1.4 to 2.5 GHz.

This work is organized as follows. In Section II, the wideband hybrid Doherty-Outphasing combiner theory is introduced. The design and simulation results are presented in Section III. The experimental results of the dual-input wideband HDO-PA are reported in Section IV. Finally, the conclusion is drawn in Section V.

II. WIDEBAND HYBRID DOHERTY-OUTPHASING COMBINER THEORY

The wideband combiner theory in this work is developed as an extension of the single frequency combiner theory presented in [30] and [31]. The wideband hybrid Doherty-Outphasing combiner theory at the device current-source reference plane is based on the conceptual diagram presented in Fig. 1. The main and auxiliary transistors are represented by two ideal current sources associated with their fundamental drain currents. A wideband combiner network represented by the two-port Z parameters $Z(\omega)$ is connected between the two current sources to perform the load modulation within the frequency range of interest.

A. Combiner Network Analysis Based on a Two-Port Network

The two-port combiner network consists of a reciprocal and lossless three-port network terminated with an output load R_L as shown in Fig. 1. It is assumed that the power and frequency dependent load impedances seen by the main and auxiliary devices are both real (at peak and backoff) and are thus denoted by R_m and R_a in Fig. 1. Comprehensive analytical formulas [(8)–(16)] have been provided in [30] to fully describe the generalized combiner theory at a single frequency. The wideband combiner theory in this work is developed from a special case of [30] or [31], which assumes that the auxiliary device is completely off at backoff power

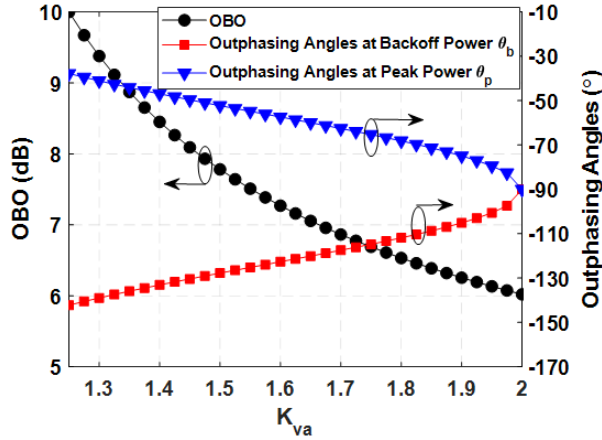


Fig. 2. OBO and peak and backoff outphasing angles versus K_{va} .

level ($|I_{ab}| = 0$). By reducing the design space from four dimension in [30] to two dimension here using $K_{ia} = \infty$ and $K_{vm} = 1$, the design equations in [30] are further simplified as follows. The asymmetry fundamental peak power ratio n between the main and auxiliary amplifiers reduces to

$$n = \frac{P_{ap}}{P_{mp}} = \frac{|V_{ap}||I_{ap}|}{|V_{mp}||I_{mp}|} = K_{va} \left(\frac{K_{im} - 1}{K_{im}} \right). \quad (1)$$

It is noted that the value of the currents and voltages in this work are frequency dependent. Solving and obtaining the relationship of $K_{im} = K_{va}/(K_{va} - n)$, the output power backoff (OBO) is derived to be

$$\text{OBO} = \frac{P_{ap} + P_{mp}}{P_{mb}} = \frac{K_{va}(n+1)}{K_{va} - n}. \quad (2)$$

Enforcing the combiner lossless-ness condition $\mathcal{R}\{Z_{12}\} = \mathcal{R}\{Z_{11}\}\mathcal{R}\{Z_{22}\}$ upon the three-port network for all frequencies, the outphasing angles at backoff and peak power levels are then obtained in terms of n and K_{va}

$$\theta_b = \pm \cos^{-1} \left(\pm \sqrt{\frac{K_{va}(1+n) - K_{va}^2}{2K_{va} - n}} \right) \quad (3)$$

$$\theta_p = \pi - \theta_b. \quad (4)$$

We shall set $n = 1$ for the same main and auxiliary peak power levels and $K_{va} \in [9/7, 2]$ for the mode-of-operation varying from the HDmax [31] to Doherty modes. The OBO is plotted versus K_{va} in Fig. 2. The outphasing angles at backoff θ_b and at peak power θ_p are also plotted versus K_{va} as shown in Fig. 2. In this work, the two negative signs are selected in (3) to reduce the physical length of the transmission line implemented in the wideband combiner circuit, as will be further illustrated in the following section. $K_{va} = 2$ corresponds to a symmetrical inverted Doherty PA operation, since the $\theta_b = \theta_p = -90^\circ$ [35]. When K_{va} is reduced to 9/7, the operating mode relaxes to the same mode reported in [31].

The load impedance seen by the main amplifier at peak and backoff power level are defined as $R_{mp} = V_{mp}/I_{mp}$ and $R_{mb} = V_{mb}/I_{mb} = K_{im}R_{mp}$, respectively. The load impedance seen by the auxiliary amplifier at peak and backoff power level are similarly defined as $R_{ap} = V_{ap}/I_{ap}$ and $R_{ab} = V_{ab}/I_{ab}$,

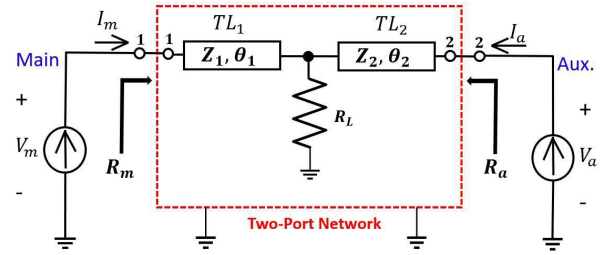


Fig. 3. Transmission line based wideband HDO-PA prototype at the device current-source reference planes.

respectively. Given $K_{ia} = \infty$, the Z parameters in Fig. (1) are simplified to be

$$\mathbf{Z} = \begin{bmatrix} R_{mb} & \frac{nR_{ap}\gamma_{vp}}{K_{va} - n} e^{-j\theta_b} \\ \frac{nR_{ap}\gamma_{vp}}{K_{va} - n} e^{-j\theta_b} & R_{ap} \frac{1 + \frac{1}{K_{va} - n} + (1 - \frac{1}{K_{va} - n}) \cdot j \tan \theta_b}{1 + j \tan \theta_b} \end{bmatrix} \quad (5)$$

where $\gamma_{vp} (= |V_{mp}|/|V_{ap}|)$ is defined to be the fundamental drain voltage ratio between the main and auxiliary devices. In this work, γ_{vp} is selected to be 1.

The analysis presented above results in important analytical formula characterizing the HDO-PA output combiner network at the current-source reference planes. This “black-box” type of combiner network can be directly synthesized using either transmission lines [31], [40] or LC-type networks [41] for single-frequency PA designs. However, it is usually time consuming or even impossible to directly synthesize a two-port wideband combiner network using the optimization tools available in microwave circuit simulators. Indeed, the optimizer is usually unable to converge to an acceptable global minima given the multiple targeted design goals over within wide bandwidth and the presence of multiple local minima.

In this work, motivated in [30] and [31], a transmission line-based combiner circuit prototype as shown in Fig. 3 will be first synthesized at the current-source reference planes to realize the two-port wideband combiner network. In this prototype, the main and auxiliary fundamental peak voltages are assumed to be the same, resulting in $\gamma_{vp} = n/\gamma_{ip} = 1$ as mentioned in [30].

As shown in Fig. 3, the two-port combiner network consists of two transmission lines with the characteristic impedance of Z_1 and Z_2 and the electrical length of θ_1 and θ_2 , respectively. A common load R_L , to which the output power is delivered, is connected between the two transmission lines.

For $K_{ia} = \infty$ and $n = 1$ the equations reported in [30] for the design parameters Z_1 , Z_2 , θ_1 , θ_2 and R_L are simplified and given by

$$\begin{aligned} Z_1 &= R_{mp} \\ Z_2 &= R_{ap} \\ R_L &= \frac{R_{mp}}{2} \\ \theta_1 &= \tan^{-1} \left(\frac{K_{va}}{K_{va} - 1} \tan[\theta_b(K_{va})] \right) \\ \theta_2 &= \tan^{-1} \left(\frac{K_{va} - 2}{K_{va} - 1} \tan[\theta_b(K_{va})] \right). \end{aligned} \quad (6)$$

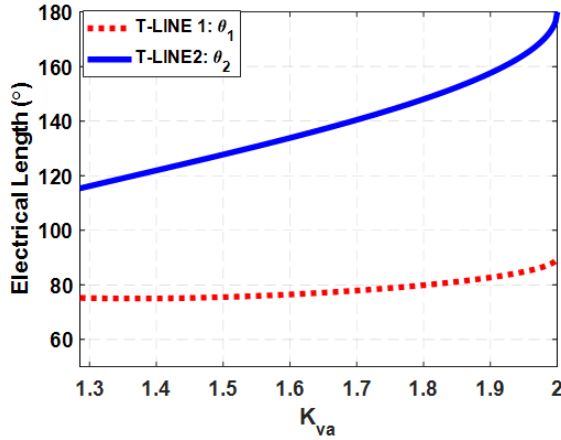


Fig. 4. Electrical length θ_1 and θ_2 of the wideband HDO-PA prototype versus K_{va} .

The electrical lengths θ_1 and θ_2 are plotted versus K_{va} as shown in Fig. 4. The solution for θ_b selected for calculating θ_1 and θ_2 is the same as the one shown in Fig. 2. In Fig. 4, the electrical lengths θ_1 and θ_2 are both monotonously increasing as K_{va} increases from 9/7 (referred as the optimal HDO-PA in [31] or the HDmax in [30]) to 2 (the symmetric inverted Doherty PA mode). The electrical lengths θ_1 and θ_2 are a function of K_{va} . The frequency dependence of θ_1 and θ_2 are then introduced by the designer by making K_{va} frequency dependent. A realizable combiner can be obtained by selecting the HDmax and Doherty modes at the minimum f_{\min} and maximum f_{\max} frequency limits, respectively, given that the electrical lengths of the transmission lines in Fig. 3 increase with frequency. A linear distribution of K_{va} versus frequency can be initially used for the intermediate frequencies

$$K_{va} = \frac{5}{7} \frac{f - f_{\min}}{f_{\max} - f_{\min}} + \frac{9}{7}. \quad (7)$$

It is noted that the ratio f_{\max}/f_{\min} can reach up to an octave depending on the topology selected for the physical combiner at the package reference planes. As K_{va} varies, the characteristic impedances Z_1 and Z_2 and the common load R_L remain constant, hence, these values are independent on the operating frequency, which significantly simplifies the design of the wideband combiner.

By selecting the peak-to-backoff voltage ratio K_{va} to monotonously increase with frequency with the proper rate, the two transmission lines TL_1 and TL_2 shown in Fig. 3 can be approximately synthesized using physical circuits. A wideband combiner circuit prototype based on Fig. 3 can then be realized in which the mode of the operation gradually switches from the HDmax mode to the symmetric inverted Doherty PA mode as the frequency increases. Based on Fig. 2, the OBO will drop from above 9.58 to 6.0 dB as the frequency increases. The backoff outphasing angles θ_b required by the wideband combiner decreases from -41° to -90° as the frequency increases, whereas, the peak outphasing angles θ_p increases from -139° to -90° as the frequency increases. Thereby a dual-input implementation is required to realize this wideband

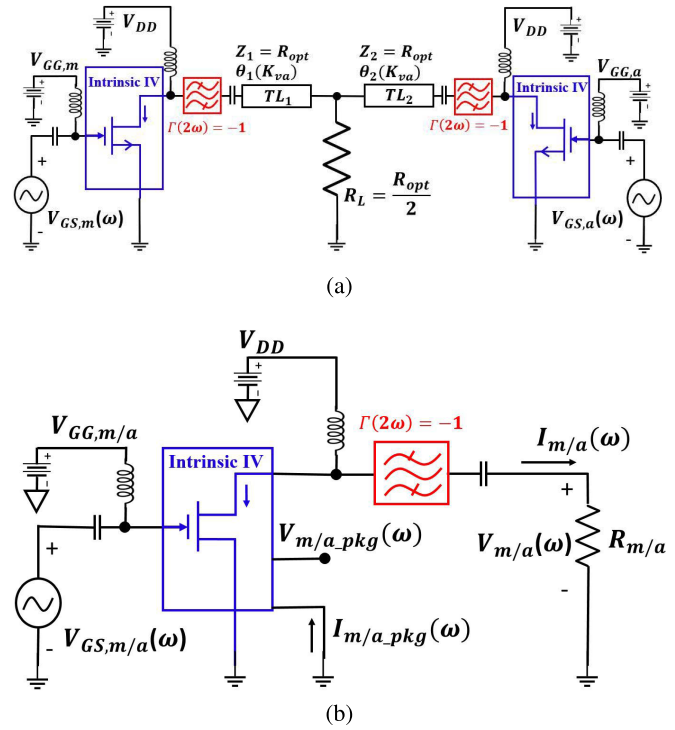


Fig. 5. Schematic of (a) wideband HDO-PA prototype built with the nonlinear embedding device model and transmission line based combiner and (b) single transistor PA terminated with an input-RF voltage source and a resistive load.

outphasing PA operation. The design and synthesis of the wideband combiner circuit will be discussed in Section III.

III. DESIGN AND SIMULATIONS

A wideband HDO-PA with maximum power of 44 dBm operating from 1.4 to 2.5 GHz can now be readily designed at the device package reference planes. In this section, the proposed wideband HDO-PA theory is first verified by performing ideal simulations at the device's current source reference planes using an nonlinear embedding device model [37]. The wideband combiner circuits and the input matching circuits are then synthesized at the device's package reference planes. Finally, the simulation results for the fabrication-ready PA circuits are presented and discussed.

A. Wideband Hybrid Doherty-Outphasing PA Theory Verification Using an Ideal PA Prototype

A wideband ideal HDO-PA prototype is shown in Fig. 5(a). Two identical nonlinear embedding device models at the current-source reference planes are used to represent the main and auxiliary PAs. The main and auxiliary PAs operate in class-B and class-C mode, respectively. The second harmonic impedances are properly terminated using two ideal filters. It is to be noted that these ideal filters at the current-source reference planes might not be physically realizable at the package reference planes, but using ideal harmonic filters allows us to perform simulations at this step to verify the proposed theory. The wideband combiner connected in

TABLE I
DESIGN PARAMETERS FOR THE WIDEBAND HDO-PA PROTOTYPE

f_0	1.4 GHz	1.6 GHz	1.8 GHz	2.0 GHz	2.2 GHz	2.4 GHz	2.5 GHz
Z_1	18.3 Ω	18.3 Ω	18.3 Ω	18.3 Ω	18.3 Ω	18.3 Ω	18.3 Ω
Z_2	18.3 Ω	18.3 Ω	18.3 Ω	18.3 Ω	18.3 Ω	18.3 Ω	18.3 Ω
R_L	9.15 Ω	9.15 Ω	9.15 Ω	9.15 Ω	9.15 Ω	9.15 Ω	9.15 Ω
θ_1	74.6°	74.4°	75.4°	77.4°	80.5°	86.6°	90.0°
θ_2	115.0°	123.0°	131.3°	140.4°	151.5°	170.1°	180.0°
$ V_{GS,mp} $	3.1 V	3.1 V	3.1 V	3.1 V	3.1 V	3.1 V	3.1 V
$ V_{GS,mb} $	0.74 V	0.98 V	1.20 V	1.39 V	1.57 V	1.72 V	1.74 V
$ V_{GS,ap} $	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V
θ_b	-139.7°	-131.4°	-124.2°	-117.0°	-109.0°	-96.5°	-90.0°
θ_p	-40.3°	-48.6°	-55.8°	-63.0°	-71.0°	-83.5°	-90.0°
K_{va}	1.25	1.39	1.53	1.67	1.81	1.95	2.00

between consists of two transmission lines TL_1 and TL_2 and the common load R_L .

For this ideal HDO-PA prototype design, the operating frequency range is selected from 1.4 to 2.5 GHz. The value of K_{va} is approximately linearly varied to shift the PA mode from HDmax to Doherty PA as the frequency increases to sustain the desired wideband backoff efficiency. The values of K_{va} are selected to be: $K_{va} = [1.25, 1.39, 1.53, 1.67, 1.81, 1.95, 2.00]$ as the frequency varies linearly from 1.4 to 2.5 GHz. The main and auxiliary PAs are designed to deliver the same peak power, which results in $n = 1$. The required main peak-to-backoff current ratios K_{im} are then obtained by using (1). A fixed dc drain bias $V_{DD} = 25$ V is adopted for both devices and the amplitude of the fundamental drain voltage for both the main and auxiliary PAs at the peak power level are set to be equal at each frequency: $|V_{mp}| = |V_{ap}| = 22$ V. By selecting the maximum fundamental drain current of the auxiliary device to be: $|I_{ap}| = 1.2$ A, the maximum fundamental drain current for the main device is calculated to be given by: $|I_{mp}| = |I_{ap}|/n = 1.2$ A. Knowing K_{va} , K_{im} and the fundamental drain voltages and currents at peak power, the amplitude of the fundamental drain voltages and currents at backoff power level can easily be calculated. Thereby, the load impedances seen by both PAs at peak power level are readily verified to be given by: $R_{mp} = R_{ap} = 18.3 \Omega$. The variation of the outphasing angle at the backoff power level versus frequency is obtained using (2) and (3). The design parameters Z_1 , Z_2 , R_L , θ_1 and θ_2 can be determined from (6) for the transmission-line based wideband combiner shown in Fig. 5(a).

The required RF-input voltages for the main and auxiliary PAs, which sustain the desired fundamental drain currents when the output ports are terminated with the correct load impedances (R_m or R_a) at each fundamental frequency, are found by performing single-transistor simulations as shown in Fig. 5(b) [39]. Specifically, the RF-input voltages at backoff and peak power levels for the main PA ($|V_{GS,m}|$) or the auxiliary PA ($|V_{GS,a}|$) are automatically extracted by sweeping the RF gate voltages and using interpolation. The main and auxiliary PAs are biased in class-B and class-C modes, respectively, with the second harmonic impedances properly terminated.

The simulations based on the schematic shown in Fig. 5(a) are performed at each frequency from 1.4 to 2.5 GHz to verify

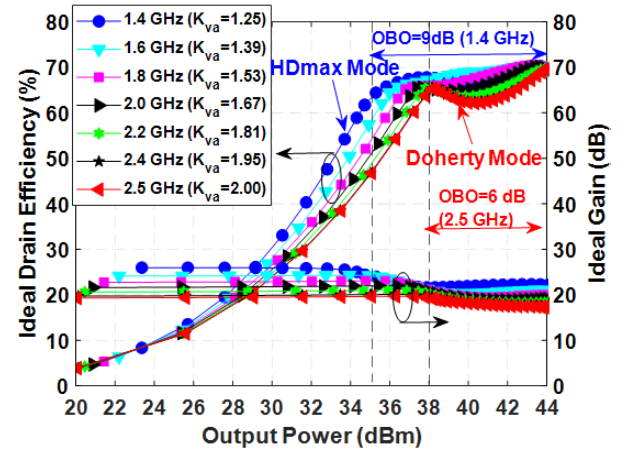


Fig. 6. Simulated drain efficiency versus frequency at the current-source reference planes.

the proposed theory. It is worth mentioning that the RF-input voltages and the outphasing angles between the backoff and peak power levels are simply selected to vary linearly with the input drive when characterizing the output power response of the PA at each frequency. The design parameters used in these simulations versus frequencies are summarized in Table I. In the simulations K_{ia} is set to be 65 to turn off the auxiliary PA at backoff power level, so that the values of the electrical length shown in Table I are slightly deviated from the theoretical values calculated by (6), where K_{ia} is assumed to be infinity. Fig. 6 shows the simulated efficiency and power gain versus output power from 1.4 to 2.5 GHz. As is indicated in this figure, the auxiliary peak-to-backoff voltage ratio K_{va} is varied as the operating frequency increases to change the PA load modulation behavior from the HDmax to Doherty PA modes. The OBO reduces from approximately 9 dB at low frequency to 6 dB at high frequency, as predicted by the proposed theory. The dual-input power gain (in dB) as shown in Fig. 6 is defined by the difference between the output power (in dBm) and the combined input power (in dBm) assuming perfect input matching networks are implemented. The load modulation behaviors seen by the main and auxiliary PAs are respectively depicted in Fig. 7(a) and (b), which indicate that the PA mode varies from the HDmax to Doherty PA

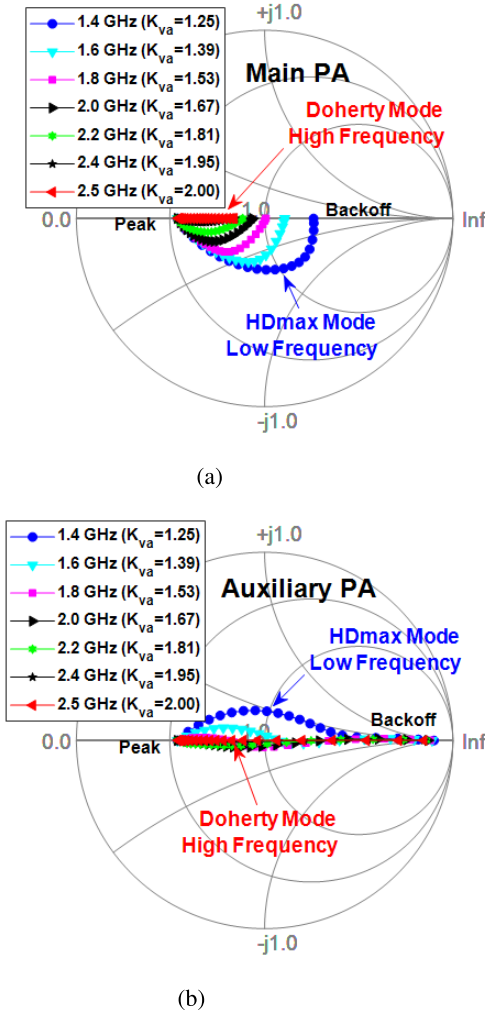


Fig. 7. Simulated load modulation trajectories versus frequency for (a) main and (b) auxiliary PAs at the current-source reference planes. (a) Main PA. (b) Auxiliary PA.

modes as the frequency increases. The load impedance at both backoff and peak power levels are maintained to be real at each frequency as targeted. The backoff impedance seen by the main PA becomes smaller as the frequency increases, which explains the reduction of the OBO versus frequency. Meanwhile, the load modulation trajectory gradually changes from a curve to a straight line as expected, when the PA mode changes from the outphasing operation to the Doherty operation.

B. Design of the Wideband Output Combiner

The wideband combiner circuit connected to the transistor's package reference planes is first designed and optimized by incorporating the linear parasitic L - C model of this GaN device reported in [36]. The nonlinear response of the transmission line's electrical length versus frequency obtained from (6) and shown in Table I, cannot be realized using a single-section transmission line as shown in Fig. 3. Therefore, a multisection transmission line topology as shown in Fig. 8 is adopted to synthesize the frequency dependence of the

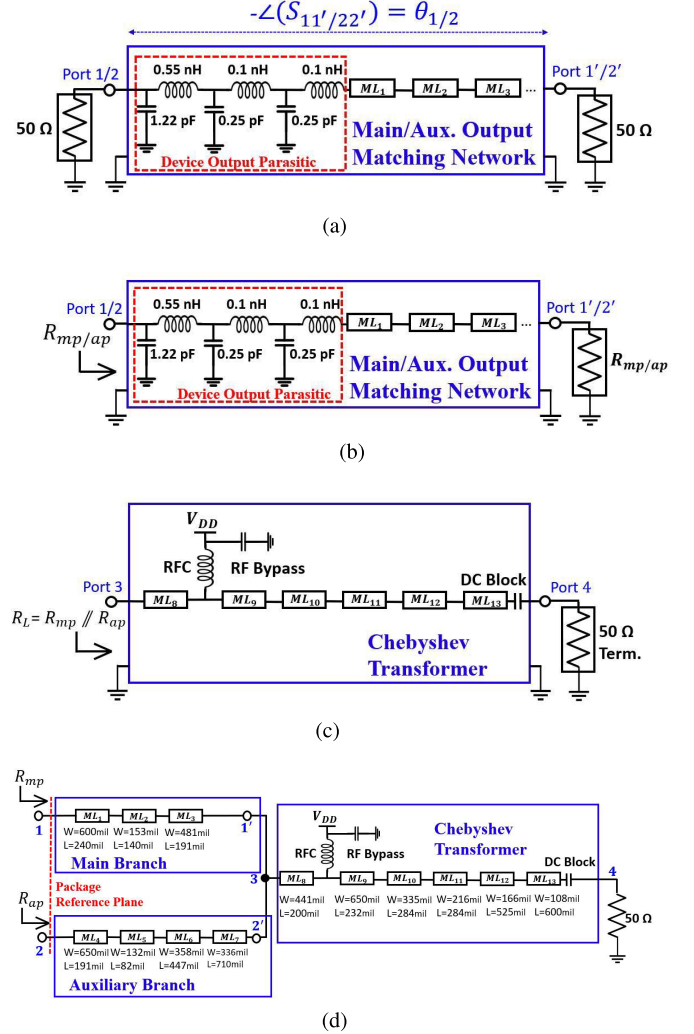
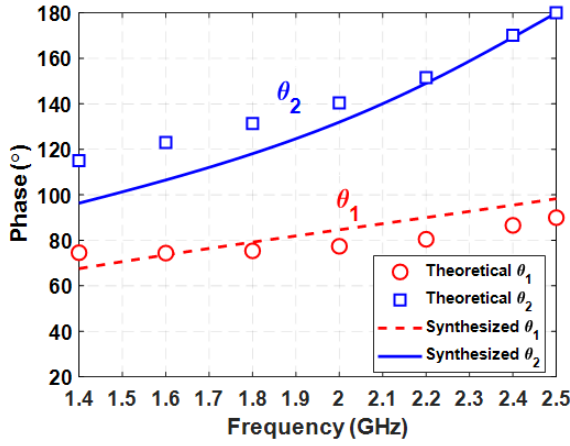


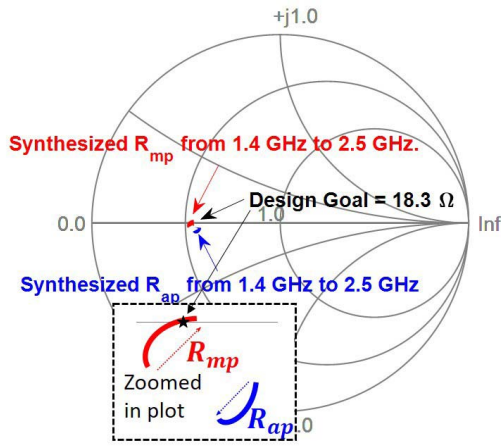
Fig. 8. (a) Synthesis of the overall electrical lengths of the main/auxiliary branches, (b) synthesis of R_{mp} and R_{ap} , (c) synthesis of the output impedance transformer, and (d) synthesis and optimization for the overall wideband combiner circuit.

electrical length. The characteristic impedance Z_1 and Z_2 of the two transmission lines implemented in Fig. 5 which are frequency independent according to (6), are determined via the impedance transformation from R'_{mp} (or R'_{ap}) to R_{mp} (or R_{ap}). The design procedure used is summarized below in *Step 1* to *Step 3*:

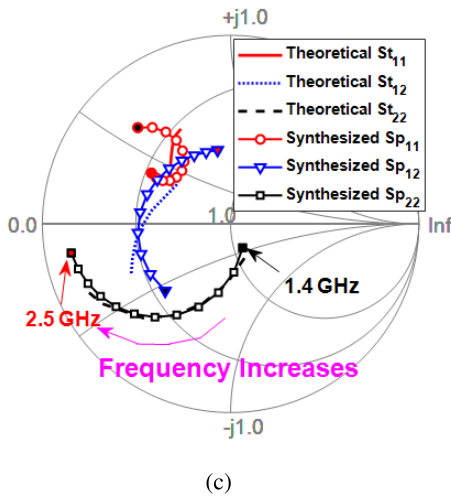
Step 1: The wideband output matching network (OMN) connected to the main PA (or auxiliary PA) is designed from 1.4 to 2.5 GHz as shown in Fig. 8. As shown in Fig. 8(a), the first design goal is to independently synthesize the main and auxiliary multisection transmission line circuits such that the absolute value of the phase of S_{21} be close to the theoretical values of the electrical lengths θ_1 and θ_2 listed respectively in Table I at each frequency. The results are shown in Fig. 9(a) for the main and auxiliary branches. The red circles indicate the theoretical θ_1 and the red-dashed line the synthesized θ_1 for the main branch. The blue rectangles indicate the theoretical θ_2 and the blue solid line the synthesized θ_2 for the auxiliary branch. For this electrical lengths optimization 50 Ω



(a)



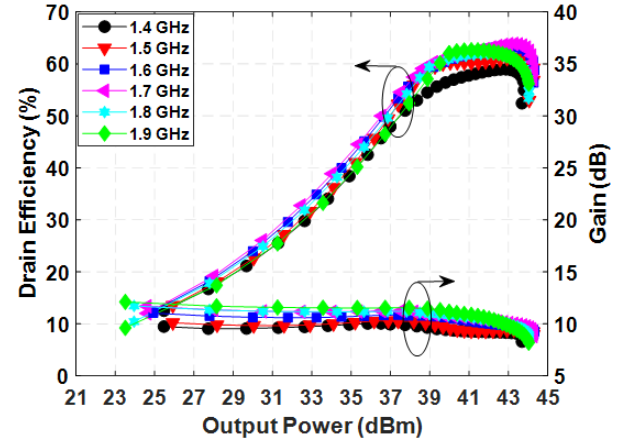
(b)



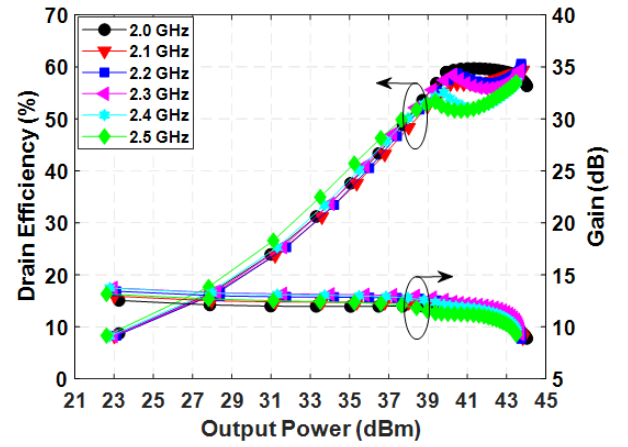
(c)

Fig. 9. (a) Comparison between the theoretical and synthesized electrical length, (b) comparison between the theoretical and synthesized R_{mp} (or R_{ap}) and (c) comparison between the theoretical and synthesized 2-port S-parameters of the wideband output combiner at the package reference planes.

impedance terminations are used. The second simultaneous design goal in the synthesis of the multisection transmission line circuits as shown in Fig. 8(b), is to transform the



(a)



(b)

Fig. 10. Simulated drain efficiency and gain from 1.4 to 2.5 GHz: (a) from 1.4 to 1.9 GHz and (b) from 2.0 to 2.5 GHz.

impedance R'_{mp} (or R'_{ap}) seen at the junction point to the impedance R_{mp} (or R_{ap}) seen by the main PA (or auxiliary PA) at each frequency at peak power. It is noticed from the zoomed-in view in Fig. 9(b), that the synthesized wideband fundamental impedance seen by the main PA (in red solid line) and the fundamental impedance seen by the auxiliary PA (in blue solid line) are close to the design target of 18.3Ω . The two-port output matching circuits as shown in Fig. 8 for the main or auxiliary branch including the device output parasitics and transmission lines are separately synthesized by simultaneously targeting these two design goals under all frequencies from 1.4 GHz to 2.5 GHz.

Step 2: The wideband output transformer that transforms the 50Ω output load to the common load R_L is implemented by adopting a Chebyshev transformer topology as shown in Fig. 8(c). The drain dc biasing circuit is co-designed together with this Chebyshev transformer.

Step 3: The initial design of the main branch, auxiliary branch in Step 1 were realized by taking account of the linear device parasitic using the linear model reported in [36]. This initial design enables to avoid the optimizer to settle in a local minimum. However, only using the linear device

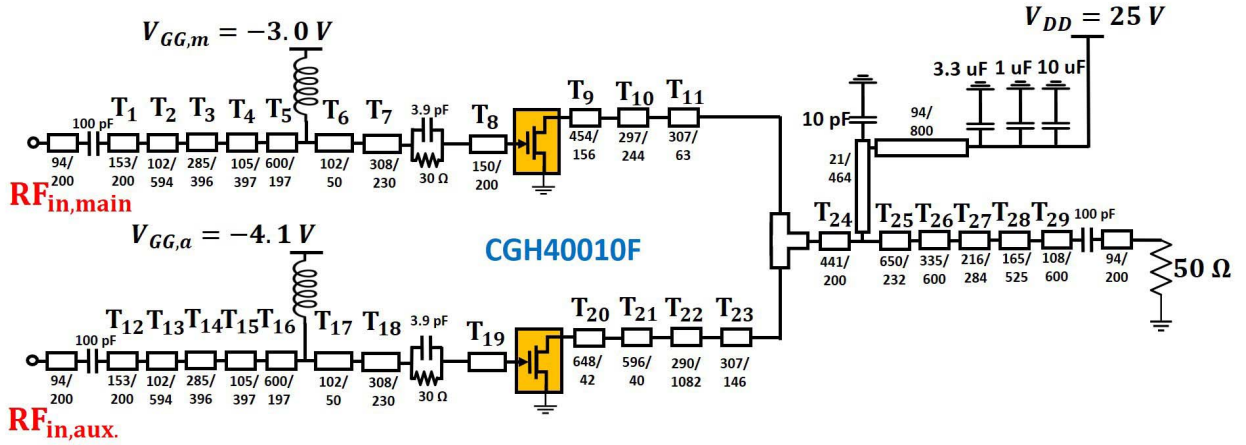


Fig. 11. Schematic of the propose dual-input wideband HDO-PA circuit operating from 1.4 to 2.5 GHz (unit: mils).

parasitic network may not be accurate enough in the presence of the nonlinear device capacitance. The wideband two-port S-parameters $S_p(\omega)$ for the entire output combiner as shown in Fig. 8(d) are then further optimized based on this initial wideband combiner design at all frequencies from 1.4 to 2.5 GHz by minimizing the error $\varepsilon(\omega)$

$$\varepsilon(\omega) = \min |S_p(\omega) - S_t(\omega)|$$

where $S_t(\omega)$ refers to the targeted S-parameters of the wideband combiner at each frequency from 1.4 GHz to 2.5 GHz at the package reference planes, as predicted by the nonlinear embedding model [37].

It is noted that in Step 3, the required fundamental drain currents and voltages at the package reference planes sustaining the desired theoretical load modulation behaviors at the current-source reference planes at backoff and peak power, are predicted using the nonlinear embedding device model introduced. The resulting two-port S-parameter $S_t(\omega)$ of the combiner at the package reference planes obtained by nonlinear embedding process are plotted using plain, dashed, and dotted lines in Fig. 9(c). The optimized two-port S-parameters $S_p(\omega)$ of the combiner are also presented in Fig. 9(c) for comparison with $S_t(\omega)$. In this work, it was difficult to precisely overlap the designed S-parameters $S_p(\omega)$ with the targeted S-parameters $S_t(\omega)$ at each frequency from 1.4 GHz to 2.5 GHz. However, the simulated wideband PA performance will turn out to be acceptable, as will be seen in Section III-C.

C. Design of the Input Matching Network and the Wideband HDO-PA Simulation Results

For the input matching network, a stepped impedance topology is adopted to realize a wideband, low-Q input matching from 50 Ω to the targeted input impedance seen at the gate of the transistors [32]. An R-C network implemented with a 3.9-pF capacitor and 30 Ω resistor in parallel is used to stabilize the PA. The simulated drain efficiency and gain versus output power at each frequency from 1.4 to 2.5 GHz are plotted in Fig. 10(a) and (b). The schematic of the wideband

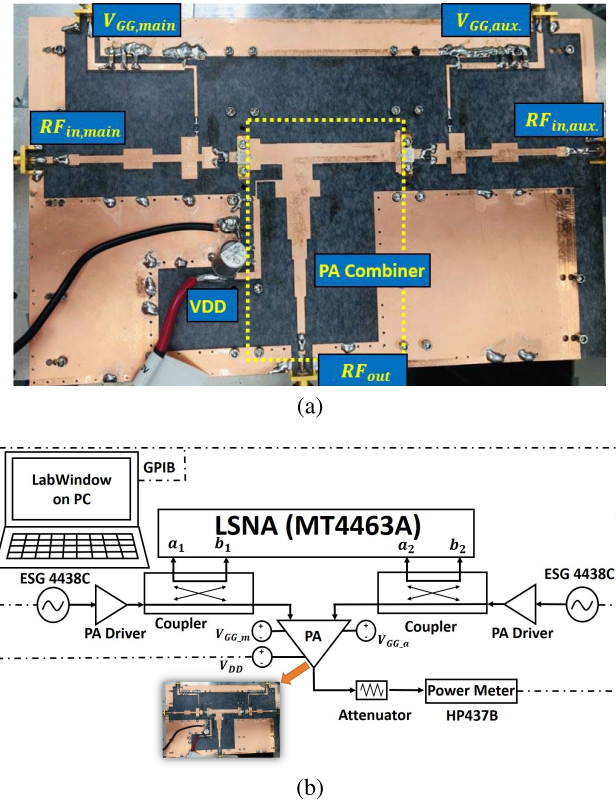


Fig. 12. (a) Fabricated wideband dual-input HDO-PA demonstrator circuit and (b) LSNA test bench used for CW measurements.

dual-input PA realized by microstrip lines is shown in Fig. 11. The incident powers at the gate of the transistors are first calculated based on the prediction of the nonlinear embedding model at the package reference planes given the value of input-RF voltages listed in Table I. The incident powers at the RF ports of the PA are calculated by taking account of the S-parameters of the Electromagnetic (EM) models of the wideband input matching networks and the R-C stability circuits. The outphasing angles at the gate current-source reference planes versus power at each frequency are first calculated

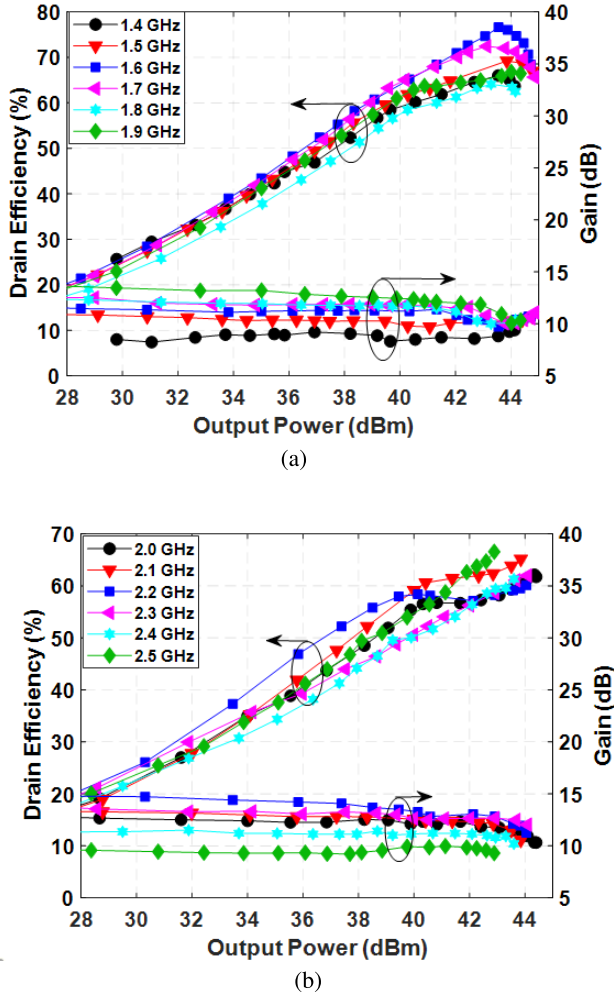


Fig. 13. Measured drain efficiency and gain from 1.4 to 2.5 GHz: (a) from 1.4 to 1.9 GHz and (b) from 2.0 to 2.5 GHz.

using (3) and (4). After nonlinear embedding of the transistor's gate parasitics and taking account of the entire input matching network and the R-C stability circuits, the outphasing angles at the RF ports of the PA at each frequency are slightly updated, which are readily used in the simulations. The wideband EM models of the input matching and output combiner circuits are obtained by performing the ADS Momentum simulations. Then the PA large signal simulations results are obtained from the ADS EM Co-Simulations by jointly running the harmonic balance simulator and EM models of the passive networks. The simulated drain efficiency and gain from 1.4 to 2.5 GHz are presented in Fig. 10. The fabricated dual-input wideband HDO-PA shown in Fig. 12(a) was built on a Rogers IsoClad 917 with a relative dielectric constant of 2.2 and a thickness of 31 mil. Two Wolfspeed's gallium nitride (GaN) high-electron-mobility transistors (HEMT) CGH40010F are used for both the main and auxiliary PAs. The main PA is set to operate in the class-AB mode with a gate bias voltage of -3.0 V and a dc quiescent current of 55 mA. The auxiliary is set to operate in the class-C mode with a gate bias voltage of -4.1 V. It is noted that the main and auxiliary PAs share the

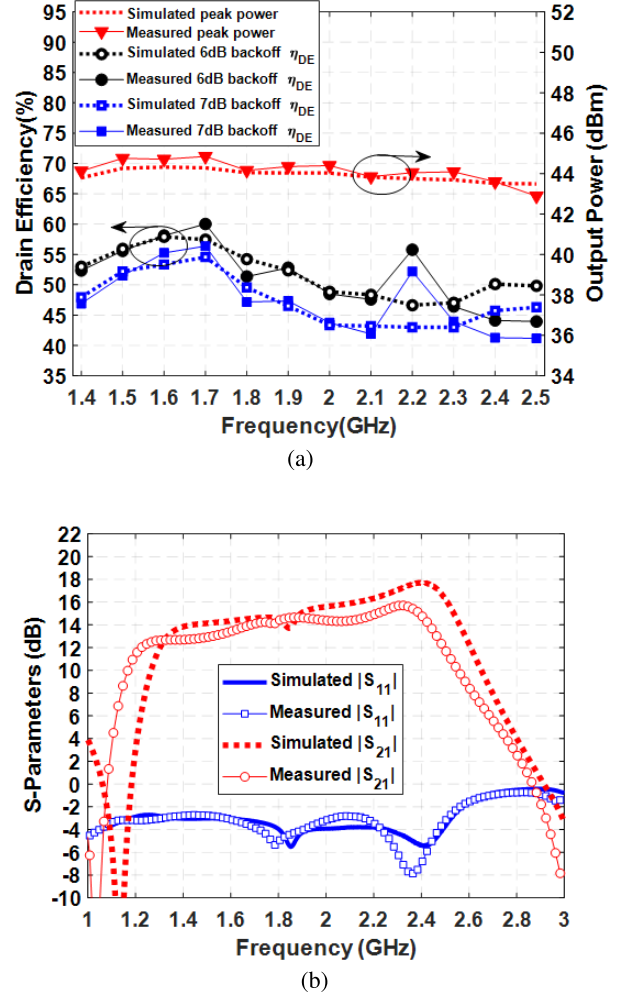


Fig. 14. (a) Comparison between simulated and measured 6 dB backoff efficiency, 7 dB backoff efficiency and peak power from 1.4 to 2.5 GHz. (b) Comparison between simulated and measured small-signal S-parameters versus frequency.

same drain dc bias of 25 V, and because of that, the two PAs are able to deliver the same amount of peak power ($n = 1$). The measurement results are presented next in Section IV.

IV. EXPERIMENTAL RESULTS

A. Continuous-Wave Measurements

The test bench based on the large signal network analyzer (LSNA) as shown in Fig. 12(b) is used for performing continuous-wave (CW) measurements from 1.4 to 2.5 GHz. For the CW measurements at each frequency, the dual-input RF ports of the HDO-PA are driven by two phase-locked signal-source generators (Keysight ESG 4438C) and are injected with the same incident power data used in the ADS EM Co-Simulation.

The measured drain efficiency and gain versus output power are plotted from 1.4 to 2.5 GHz in Fig. 13. The simulated and measured maximum output power, at 6- and 7-dB backoff efficiency are also extracted and plotted versus frequency as shown in Fig. 14(a), respectively. It is noted that the measured results and simulated results are comparable across the entire

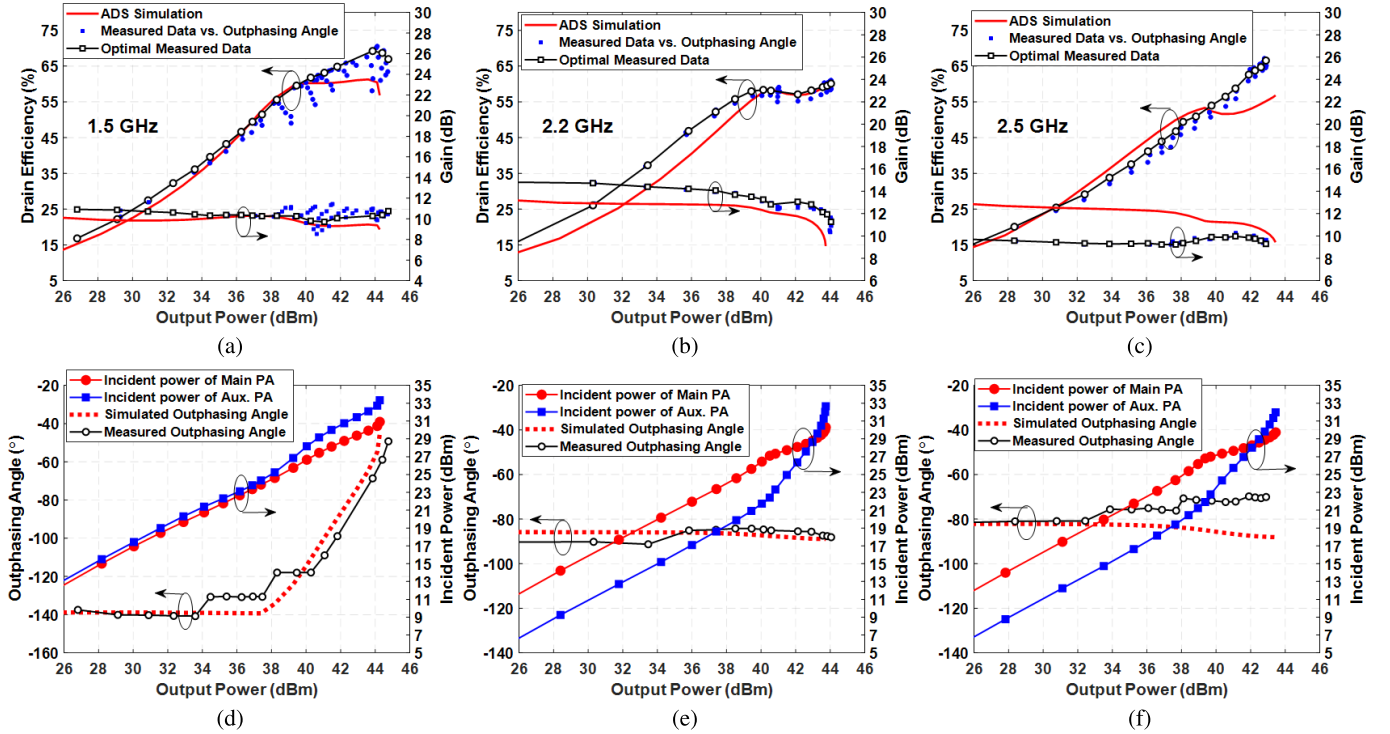


Fig. 15. Comparison between the measured and simulated optimal drain efficiency and gain at (a) 1.5 GHz, (b) 2.2 GHz, and (c) 2.5 GHz. Associated dual-incident power and comparison between the measured and simulated outphasing angles at (d) 1.5 GHz, (e) 2.2 GHz, and (f) 2.5 GHz.

frequency range. The measured 6 dB backoff efficiencies are from 44% to 60% and the measured 7-dB backoff efficiencies are from 41% to 55% across the frequency range from 1.4 to 2.5 GHz. The measured maximum output powers are around 44 dBm from 1.4 to 2.5 GHz. The small signal measurements and simulations are presented and compared in Fig. 14(b) to further evaluate the fabrication accuracy of the wideband HDO-PA circuit. Since the auxiliary PA is off under small-signal excitation, port 1 refers to the RF input port of main PA and port 2 refers to the output of the HDO-PA. $|S_{11}|$ and $|S_{21}|$ in dB are simulated and measured with the auxiliary RF input port terminated with a 50 Ω load. Fig. 15 compares the ADS EM Co-Simulations with the CW measurements results at 1.5, 2.2, and 2.5 GHz, respectively. From Fig. 15(a)–(c), the measured optimal drain efficiency (indicated by black hollow circles) and gain (indicated by black hollow rectangles) are comparable to the simulated data (indicated by red lines). The measured drain efficiency and gain associated with the outphasing angles are also depicted by the blue dots. It is noted that the outphasing angles applied in the CW measurements between the dual-input RF ports were swept at each power level based on the same range of outphasing angles used in the ADS simulations instead of relying on the exact simulation value. This was done to compensate for performance degradation caused by imperfections in both the PA fabrication and the device model. The outphasing angles (indicated by the black circles) based on the optimal PA performance at these frequencies are compared with the theoretical outphasing angles used in the ADS simulations (indicated by the red-dashed lines) in Fig. 15(d)–(f). The

difference between these outphasing angles is reasonable. It is also noted that the difference between the outphasing angle at backoff θ_b and the outphasing angle at peak θ_p reduces as the frequency increases from 1.5 to 2.5 GHz, which implies that the wideband PA operates in the outphasing mode at lower frequencies and gradually shifts to the Doherty mode at higher frequencies.

B. Modulated Signal Measurements

The fabricated wideband HDO-PA has also been evaluated with 20-MHz LTE signals exhibiting 6.5-dB PAPR at 1.7, 2.2, and 2.5 GHz, respectively. The linearization method in this work is the same as the one mentioned in [25]. A lookup table (LUT) is extracted based on the CW measurement results in Fig. 14. This LUT includes the PA output power as a function of the dual incident powers and the outphasing angles for the above three carrier frequencies. An inverse PA model is implemented using the generalized cubic-spline basis algorithm [53] and it is used to generate the predistorted waveforms. It is worth mentioning that for demonstration purpose the same waveforms were used for both extracting the inverse model and linearizing the PA. When the wideband HDO-PA is excited with the 20-MHz LTE signals at 1.7 GHz, 47.8% of average drain efficiency and around -54.0 -dBc adjacent-channel-leakage-ratio (ACLR) are achieved at an average output power of 37.7 dBm after applying DPD. When the wideband HDO-PA is excited with the 20-MHz LTE signals at 2.2 GHz, 44.0% of average drain efficiency and around -49.4 -dBc ACLR are achieved at an

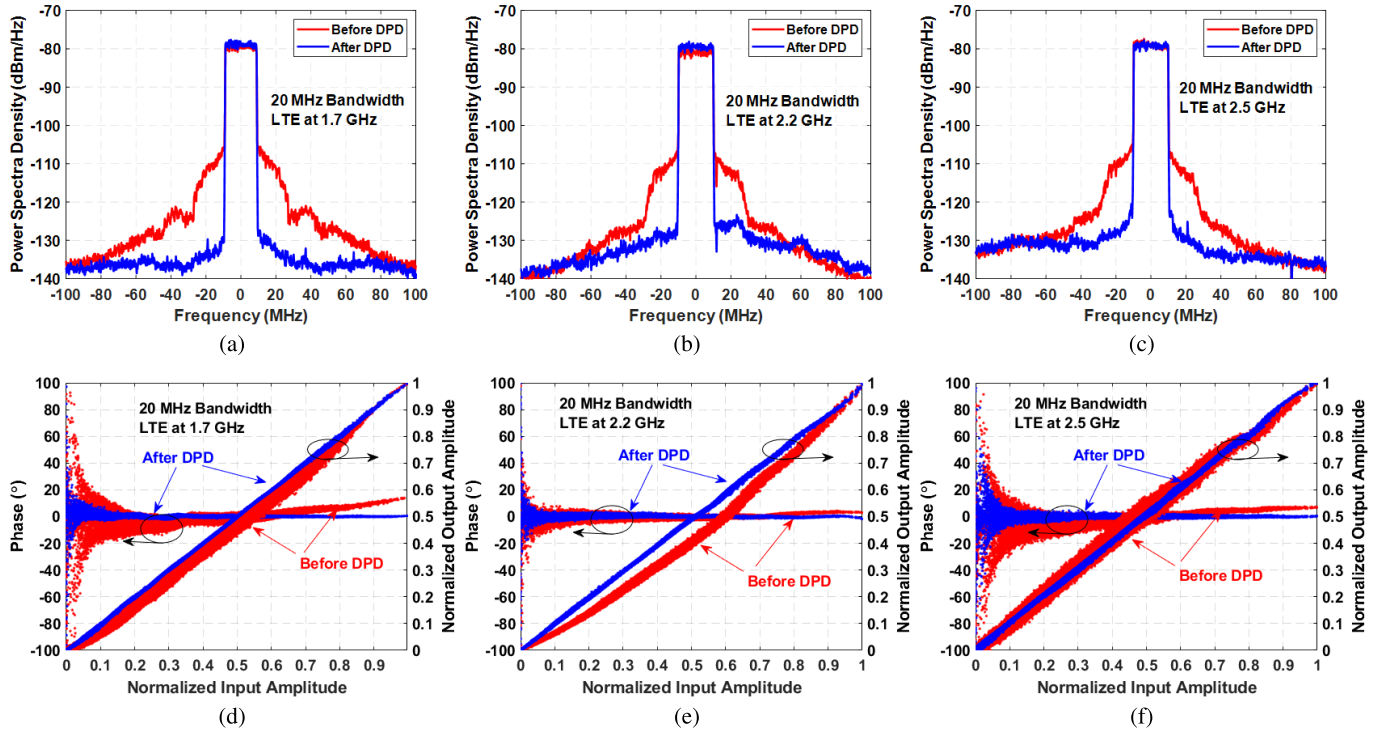


Fig. 16. Output power spectral density before (red) and after (blue) applying the DPD under (a) 1.7 GHz, (b) 2.2 GHz, and (c) 2.5 GHz. AM/AM and AM/PM before (red) and after (blue) applying the DPD under (d) 1.7 GHz, (e) 2.2 GHz, and (f) 2.5 GHz.

TABLE II
MODULATED SIGNAL MEASUREMENT WITH 20 MHz LTE SIGNAL

	f_0 (GHz)	Output PAPR (dB)	$P_{inc,avg.}$ (dBm)	$P_{out,avg.}$ (dBm)	Gain _{avg} (dB)	$\eta_{DE,avg.}/PAE_{avg.}$ (%)	ACLR _{L,H} (dBc)	NMSE (dB)
Before DPD	1.7	6.9	25.3	37.2	11.9	50.3/47.1	-32.4, -31.8	-20.5
After DPD	1.7	6.4	25.3	37.7	12.4	47.8/45.0	-54.0, -52.3	-42.9
Before DPD	2.2	8.0	24.3	35.2	10.9	40.0/36.7	-30.2, -30.5	-14.7
After DPD	2.2	6.6	25.3	36.7	11.4	44.0/40.8	-49.4, -46.5	-32.7
Before DPD	2.5	6.1	27.5	35.5	8.0	40.0/33.7	-30.8, -32.7	-22.9
After DPD	2.5	6.2	28.4	35.4	7.0	40.4/32.3	-47.6, -49.2	-33.8

TABLE III
COMPARISON AND SUMMARY OF THE RECENT DUAL-INPUT DOHERTY-OUTPHASING POWER AMPLIFIERS

Technology	PA Operation Methodology	Frequency (GHz)	Backoff η^* (%)	Saturation η^* (%)	Signal Bandwidth (MHz)	η_{avg} (%)	PAPR (dB)	ACLR (dBc)	Reference
GaN	Numerical Sweep	2.14	50 (12-dB OBO)	66	-	-	-	-	[27]**
GaN	Numerical Sweep	0.58	74 (10-dB OBO)	80.0	10	70.2	10.4	-47.7	[29]
GaN	Numerical Sweep	1.2-3.7	48-68 (6-dB OBO)	45-68	5.0	44-51	6.7	-59	[32]
GaN	Numerical Sweep	1.4-4.8	45-62 (6-dB OBO)	45-65	-	-	-	-	[33]**
GaN	Numerical Sweep	0.7-3.0	40.4-65.8 (6-dB OBO)	49.8-60.3	20	42.8-64.6	6.04	-50.9	[34]
GaN	Analytical Solution	1.4-2.5	44.0-60.0 (6-dB OBO)	60.1-68.4	20	40.4-47.8	6.5	-54.0	This work

* η refers to drain efficiency under CW measurements.

** No modulated signal measurements were performed.

average output power of 36.7 dBm after applying DPD. When the wideband HDO-PA is excited with the 20 MHz LTE signals at 2.5 GHz, 40.4% of average drain efficiency and around -49.2-dBc ACLR are achieved at an average output power of 35.4 dBm after applying DPD. It is noted that the measured average gain at 2.5 GHz is low, which may be due to the degraded input return loss and small signal gain at

the edge of the bandwidth of the PA. The modulated signal measurements are also summarized in Table II. The output power spectral density tested by the 20-MHz LTE signals centered at 1.7, 2.2 and 2.5 GHz before and after applying DPD are shown in Fig. 16(a)–(c), respectively. The AM/AM and AM/PM before and after applying DPD are also shown in Fig. 12(d)–(f), respectively. In Table III, the performance

of the wideband HDO-PA proposed in this article is compared with other recent works found in the literature reviews. It is to be noted that all the PAs in Table III rely on a dual-input PA configuration using outphasing to enhance the Doherty operation over a wide range of frequencies or at single frequency. The three reference broadband PAs already reported in the literature [32]–[34] are all optimized using an empirical search relying on the 3-D sweep of the two input power and outphasing angle at each frequency. This systematic 3-D search approach usually yields disjointed solutions in terms of outphasing angle and input power as the frequency varies. This is expected to limit the high-efficiency operation of these PAs for wide bandwidth 5G signals both before and after DPD. On the contrary, the dual-input HDO-PA proposed in this article relies on an analytic theory in which the PA mode of operation gradually shifts from the HDmax to Doherty modes. As a consequence, the input power levels and the outphasing angles vary smoothly as the frequency changes.

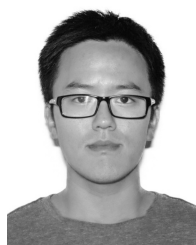
V. CONCLUSION

A wideband HDO-PA combiner theory has been developed. The theory was initially established and verified using the HDO-PA prototype implemented by the nonlinear embedding device model and ideal combiner two-port network. Based on the theory, wideband combiner circuits were realized at the package reference planes by incorporating the device's output parasitic. A wideband hybrid Doherty-Outphasing PA demonstrator circuits operating from 1.4 to 2.5 GHz was implemented and fabricated. The fabricated PA was evaluated using both CW measurements and modulated signal measurements across the entire bandwidth of interest to further validate the theory and design methodology proposed in this work.

REFERENCES

- [1] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.
- [2] F. Raab, "Efficiency of Doherty RF power-amplifier systems," *IEEE Trans. Broadcast.*, vol. BC-33, no. 3, pp. 77–83, Sep. 1987.
- [3] M. Iwamoto, A. Williams, P.-F. Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2472–2479, Dec. 2001.
- [4] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE Microw. Mag.*, vol. 7, no. 5, pp. 42–50, Oct. 2006.
- [5] A. Grebennikov and S. Bulja, "High-efficiency Doherty power amplifiers: Historical aspect and modern trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.
- [6] R. Darraji, F. M. Ghannouchi, and O. Hammi, "A dual-input digitally driven Doherty amplifier architecture for performance enhancement of Doherty transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1284–1293, May 2011.
- [7] R. Darraji, P. Mousavi, and F. M. Ghannouchi, "Doherty goes digital: Digitally enhanced Doherty power amplifiers," *IEEE Microw. Mag.*, vol. 17, no. 8, pp. 41–51, Aug. 2016.
- [8] K. Bathich, A. Z. Markos, and G. Boeck, "Frequency response analysis and bandwidth extension of the Doherty amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 4, pp. 934–944, Apr. 2011.
- [9] D. Y.-T. Wu and S. Boumaiza, "A modified Doherty configuration for broadband amplification using symmetrical devices," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3201–3213, Oct. 2012.
- [10] R. Giorio, L. Piazzon, P. Colantonio, and F. Giannini, "An ultra-broadband GaN Doherty amplifier with 83% of fractional bandwidth," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 11, pp. 775–777, Nov. 2014.
- [11] J. M. Rubio, J. Fang, V. Camarchia, R. Quaglia, M. Pirola, and G. Ghione, "3–3.6-GHz wideband GaN Doherty power amplifier exploiting output compensation stages," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 8, pp. 2543–2548, Aug. 2012.
- [12] J. Xia, M. Yang, Y. Guo, and A. Zhu, "A broadband high-efficiency Doherty power amplifier with integrated compensating reactance," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2014–2024, Jul. 2016.
- [13] J. Pang, S. He, C. Huang, Z. Dai, J. Peng, and F. You, "A post-matching Doherty power amplifier employing low-order impedance inverters for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4061–4071, Dec. 2015.
- [14] X. Y. Zhou, S. Y. Zheng, W. S. Chan, S. Chen, and D. Ho, "Broadband efficiency-enhanced mutually coupled harmonic postmatching Doherty power amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1758–1771, Jul. 2017.
- [15] X. Chen, W. Chen, F. M. Ghannouchi, Z. Feng, and Y. Liu, "A broadband Doherty power amplifier based on continuous-mode technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4505–4517, Dec. 2016.
- [16] W. Shi *et al.*, "Broadband continuous-mode Doherty power amplifiers with noninfinity peaking impedance," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1034–1046, Feb. 2018.
- [17] C. Huang, S. He, and F. You, "Design of broadband modified class-J Doherty power amplifier with specific second harmonic terminations," *IEEE Access*, vol. 6, pp. 2531–2540, 2018.
- [18] Y. Li, X. Fang, A. Jundi, H. Huang, and S. Boumaiza, "Two-port network theory-based design method for broadband class J Doherty amplifiers," *IEEE Access*, vol. 7, pp. 51028–51038, Apr. 2019.
- [19] S. Ghosh and K. Rawat, "Hybrid analog/digital continuous class B/J mode for broadband Doherty power amplifiers," *IEEE Access*, vol. 7, pp. 74986–74995, Jun. 2019.
- [20] H. Chireix, "High power outphasing modulation," *Proc. Inst. Radio Eng.*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.
- [21] F. Raab, "Efficiency of outphasing RF power-amplifier systems," *IEEE Trans. Commun.*, vol. COMM-33, no. 10, pp. 1094–1099, Oct. 1985.
- [22] T. W. Barton, J. L. Dawson, and D. J. Perreault, "Experimental validation of a four-way outphasing combiner for microwave power amplification," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 1, pp. 28–30, Jan. 2013.
- [23] T. W. Barton and D. J. Perreault, "Four-way microstrip-based power combining for microwave outphasing power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2987–2998, Oct. 2014.
- [24] T. W. Barton and D. J. Perreault, "Theory and implementation of RF-input outphasing power amplification," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4273–4283, Dec. 2015.
- [25] H.-C. Chang, Y. Hahn, P. Roblin, and T. W. Barton, "New mixed-mode design methodology for high-efficiency outphasing chireix amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 4, pp. 1594–1607, Apr. 2019.
- [26] L. C. Nunes, F. Barradas, D. Barros, P. Cabral, and J. C. Pedro, "Current mode outphasing power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1160–1163.
- [27] A. R. Qureshi, M. Acar, J. Qureshi, R. Wesson, and L. D. Vreede, "A 112 W GaN dual input Doherty-outphasing power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4.
- [28] H. Jang *et al.*, "RF-input self-outphasing Doherty-Chireix combined amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4518–4534, Nov. 2016.
- [29] A. Yamaoka, T. Hone, and K. Yamaguchi, "70% efficient dual-input Doherty-outphasing power amplifier for large PAPR signals," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2019, pp. 556–559.
- [30] C. Liang, P. Roblin, Y. Hahn, Z. Popovic, and H.-C. Chang, "Novel outphasing power amplifiers designed with an analytic generalized Doherty-Chireix continuum theory," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 2935–2948, Aug. 2019.
- [31] C. Liang, T. Niubo-Aleman, Y. Hahn, P. Roblin, and J. A. Reynoso-Hernandez, "Optimal two-way hybrid Doherty-outphasing power amplifier," in *Proc. IEEE Topical Conf. RF/Microw. Power Modeling Radio Wireless Appl. (PAWR)*, Jan. 2020, pp. 26–29.
- [32] C. M. Andersson, D. Gustafsson, J. C. Cahuana, R. Hellberg, and C. Fager, "A 1–3-GHz digitally controlled dual-RF input power-amplifier design based on a Doherty-outphasing continuum analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3743–3752, Oct. 2013.

- [33] Y. Komatsuzaki *et al.*, "A novel 1.4–4.8 GHz ultra-wideband, over 45% high efficiency digitally assisted frequency-periodic load modulated amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 706–709.
- [34] W. Shi, S. He, J. Peng, and J. Wang, "Digital dual-input Doherty configuration for ultrawideband application," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7509–7518, Sep. 2020.
- [35] S. Kwon *et al.*, "Inverted-load network for high-power Doherty amplifier," *IEEE Microw. Mag.*, vol. 10, no. 1, pp. 93–98, Feb. 2009.
- [36] P. Tasker and J. Benedikt, "Waveform inspired models and the harmonic balance emulator," *IEEE Microw. Mag.*, vol. 12, no. 2, pp. 38–54, Apr. 2011.
- [37] H. Jang, P. Roblin, and Z. Xie, "Model-based nonlinear embedding for power-amplifier design," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 1986–2002, Sep. 2014.
- [38] C. Liang, P. Roblin, Y. Hahn, and Y. Xiao, "Automatic algorithm for the direct design of asymmetric Doherty power amplifiers," in *Proc. IEEE PAWR Conf.*, Jan. 2019, pp. 1–4.
- [39] C. Liang, P. Roblin, and Y. Hahn, "Accelerated design methodology for dual-input Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 10, pp. 3983–3995, Oct. 2019.
- [40] M. Ozen, K. Andersson, and C. Fager, "Symmetrical Doherty power amplifier with extended efficiency range," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1273–1284, Apr. 2016.
- [41] M. Ozen, N. Rostomyan, K. Aufinger, and C. Fager, "Efficient millimeter wave Doherty PA design based on a low-loss combiner synthesis technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 12, pp. 1143–1145, Dec. 2017.
- [42] M. Ozen, M. van der Heijden, M. Acar, R. Jos, and C. Fager, "A generalized combiner synthesis technique for class-E outphasing transmitters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 5, pp. 1126–1139, May 2017.
- [43] W. Hallberg, M. Ozen, D. Gustafsson, K. Buisman, and C. Fager, "A Doherty power amplifier design method for improved efficiency and linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4491–4504, Dec. 2016.
- [44] X. H. Fang and K.-K.-M. Cheng, "Extension of high-efficiency range of Doherty amplifier by using complex combining load," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2038–2047, Sep. 2014.
- [45] X. Fang, A. Chung, and S. Boumaiza, "Linearity-enhanced Doherty power amplifier using output combining network with predefined AM-PM characteristics," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 1, pp. 195–204, Jan. 2019.
- [46] H. Jang, P. Roblin, C. Quindroit, Y. Lin, and R. D. Pond, "Asymmetrical Doherty power amplifier designed using model-based nonlinear embedding," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3436–3451, Dec. 2014.
- [47] T. Sharma *et al.*, "High-efficiency input and output harmonically engineered power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1002–1014, Feb. 2018.
- [48] X. Y. Zhou, W. S. Chan, S. Chen, W. Feng, J. Pang, and D. Ho, "Linearity enhanced harmonic-modulated impedance inverter Doherty-like power amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 6, pp. 2029–2041, Jun. 2020.
- [49] X. Y. Zhou *et al.*, "A mixed topology for broadband high-efficiency Doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 3, pp. 1050–1064, Mar. 2019.
- [50] A. Raffo, F. Scappaviva, and G. Vannini, "A new approach to microwave power amplifier design based on the experimental characterization of the intrinsic electron-device load line," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 7, pp. 1743–1752, Jul. 2009.
- [51] V. Vadalà, A. Raffo, S. Di Falco, G. Bosi, A. Nalli, and G. Vannini, "A load-pull characterization technique accounting for harmonic tuning," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 7, pp. 2695–2704, Jul. 2013.
- [52] P. Roblin, H.-C. Chang, C. Liang, R. Alsulami, F. Martinez-Rodriguez, and J. A. G. Aguilar, "Direct design of Doherty and chireix PAs using a nonlinear embedding device model," in *Proc. IEEE Topical Conf. RF/Microw. Power Modeling Radio Wireless Appl. (PAWR)*, Jan. 2017, pp. 44–47.
- [53] N. Narahariseti, P. Roblin, C. Quindroit, and S. Gheitanichi, "Efficient least-squares 2-D-cubic spline for concurrent dual-band systems," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 7, pp. 2199–2210, Jul. 2015.



Chenyu Liang (Member, IEEE) received the B.S. degree in electrical and computer engineering from New Mexico State University, Las Cruces, NM, USA, in 2013, the B.Eng. degree in electrical engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2013, and the M.S. degree in electrical and computer engineering from The Ohio State University, Columbus, OH, USA, in 2016, where he is currently pursuing the Ph.D. degree.

He was with Qorvo, San Jose, CA, USA, as a millimeter-wave/RFIC power amplifier design engineer intern, from May to August 2020. His main interests include sub-6-GHz high efficiency wideband Doherty power amplifiers for base-station applications, RF/millimeter-wave on-chip power amplifier design and nonlinear RF measurement using nonlinear vector network analyzer.

Mr. Liang was the recipient of 2019 Fall Outstanding Teaching Assistant Award of the Department of Electrical and Computer Engineering of The Ohio State University.



Jose I. Martinez-Lopez (Member, IEEE) was born in Mexico City, Mexico. He received the B.S., M.Eng., and Ph.D. degrees in electrical engineering from the National Autonomous University of Mexico (UNAM), Mexico City, in 1994, 1998, and 2005, respectively.

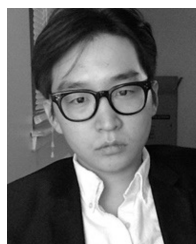
In 2006, he was with the Schlumberger Technology Center, Sugar Land, TX, USA, where he was developing antennas for deep induction array tools for the oil industry. In 2009, he was a Visiting Scholar with the ElectroScience Laboratory, The Ohio State University (OSU), Columbus, OH, USA. He is currently a Professor of electrical engineering with UNAM. He is currently on a sabbatical leave as a Visiting Scholar with the Nonlinear RF Lab, Department of Electrical and Computer Engineering, ECE-OSU. His current research interests include antenna arrays, frequency selective surfaces and microwave and millimeter-wave circuits.



Patrick Roblin (Senior Member, IEEE) received the Maitrise de Physics degree from Louis Pasteur University, Strasbourg, France, in 1980, and the M.S. and D.Sc. degrees in electrical engineering from Washington University, St. Louis, MO, USA, in 1982 and 1984, respectively.

In 1984, he joined the Department of Electrical Engineering, The Ohio State University (OSU), Columbus, OH, USA, as an Assistant Professor, where he is currently a Professor. He is also the Founder of the Non-Linear RF Research Laboratory, OSU. He is also the lead author of the two textbooks *High-Speed Heterostructure and Devices* (Cambridge University Press, 2002) and *Nonlinear RF Circuits and Nonlinear Vector Network Analyzers* (Cambridge University Press, 2011). His current research interests include the measurement, modeling, design, and linearization of nonlinear RF devices and circuits such as oscillators, mixers, and power amplifiers.

Dr. Roblin served as a Distinguished Microwave Lecturer in 2016, 2017, and 2018.



Yunsik Hahn (Graduate Student Member, IEEE) was born in Seoul, South Korea. He received the B.Eng. degree in electronic engineering from Dong-A University, Busan, South Korea, in 2012. He is currently pursuing the Ph.D. degree in electrical and computer engineering at The Ohio State University, Columbus, OH, USA.

His main research interest is linearization of high efficiency nonlinear power amplifiers with digital predistortion techniques.



Dominic Mikrut (Graduate Student Member, IEEE) received the B.Sc. degree in electrical and computer engineering from The Ohio State University, Columbus, OH, USA, in 2018, where he is currently pursuing the Ph.D. degree in electrical and computer engineering.

His current research interests are focused on high efficiency wideband power amplifiers and nonlinear behavioral modeling.



Vanessa Chen (Member, IEEE) received the Ph.D. degree in electrical and computer engineering from Carnegie Mellon University, Pittsburgh, PA, USA, in 2013.

She was with Qualcomm, San Diego, CA, USA, working on energy-efficient data-acquisition systems for mobile devices. From 2010 to 2013, at Carnegie Mellon, she focused her research on self-healing systems and high-speed ADCs, and held a research internship position at IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, in 2012. She was an Assistant Professor with The Ohio State University, Columbus, OH, USA. She is currently an Assistant Professor of electrical and computer engineering with Carnegie Mellon University. Her research interests focus on data conversion interfaces for machine learning, RF/analog hardware security, ubiquitous sensing and communication systems.

Dr. Chen is a Technical Program Committee Member of the IEEE Custom Integrated Circuits Conference (CICC) and the IEEE Asian Solid-State Circuits Conference (A-SSCC). She was a recipient of the NSF CAREER Award in 2019, the Analog Devices Outstanding Student Designer Award in 2013, and the IBM Ph.D. Fellowship in 2012. She is also an Associate Editor of the IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS.