Trapped Charge Effect on Composite Lithium Niobate-Silicon Acoustoelectric Delay Lines

Hakhamanesh Mansoorzare and Reza Abdolvand
Department of Electrical and Computer Engineering
University of Central Florida
Orlando, USA
hakha@knights.ucf.edu

***Abstract*—Acoustoelectric delay lines (AEDL) fabricated on a composite lithium niobate-silicon (LN-Si) platform could enable acoustoelectric (AE) nonreciprocity and gain provided that the material properties of the LN-Si heterostructure are properly selected. Among such properties are the carrier density and mobility in the Si substrate. However, the bulk Si properties are subject to substantial perturbation at the LN-Si interface as a result of interfacial trapped charges at dislocations and dangling bond sites. The metal-insulator-semiconductor (MIS) capacitor inherently formed in such heterostructures, however, could allow for some level of control over the Si carrier distribution at the LN film interface. In this work, we demonstrate that the AE gain achieved by the momentum transfer from the carriers drifting in Si and the subsequent nonreciprocity could be fine-tuned and the efficiency of the device could be improved by utilizing the MIS capacitor. The device efficiency is found to be enhanced once the majority electron carriers in n-type Si are slightly depleted at the LN-Si interface resulting in ~1.5 times improvement in the AE gain at a lower bias current, increasing the efficiency by ~60%.**

Keywords—acoustic delay line; acoustoelectric effect; lithium niobate; non-reciprocal; interface charges

I. INTRODUCTION

Acoustic waves (AW) propagating in a piezoelectric material create a periodic electric and stress field which exchanges momentum with nearby charge carriers. This can result in loss, more noticeably within the metallic electrodes, or gain, known as the acoustoelectric (AE) loss/gain [1]. While the AE effect has been extensively reported in surface acoustic wave (SAW) devices, such investigations for bulk acoustic waves are rather limited [2], [3]. Our group has recently reported significant AE gains and nonreciprocal transmission ratios (NTR) in composite lithium niobate-silicon (LN-Si) Lamb wave acoustoelectric delay lines (AEDL) [4]. The criteria for AE gain calls for the carriers to drift along the AW with a speed that exceeds the phase velocity of the AW. The extent to which the AE gain is possible is mainly a function of the electromechanical coupling and conductivity of the structure [5]. While the properties of the semiconductor layer (i.e. Si) can be tailored to achieve a high efficiency, the inevitable perturbation of the free carrier concentration and mobility at the LN-Si interface could lead to a lower than expected efficiency.

In this work, we report on the possible utilization of the metal-insulator-semiconductor (MIS) capacitor inherent in such heterostructures (Fig. 1 (a)) to adjust the carrier densities and subsequently the device efficiency. Our preliminary results suggest that the efficiency is improved by slightly depleting the Si surface. The effect of the free carrier density and carrier mobility on the theoretical values of AE gain is plotted in Fig. 1 (b), showing a very strong dependency on the former.

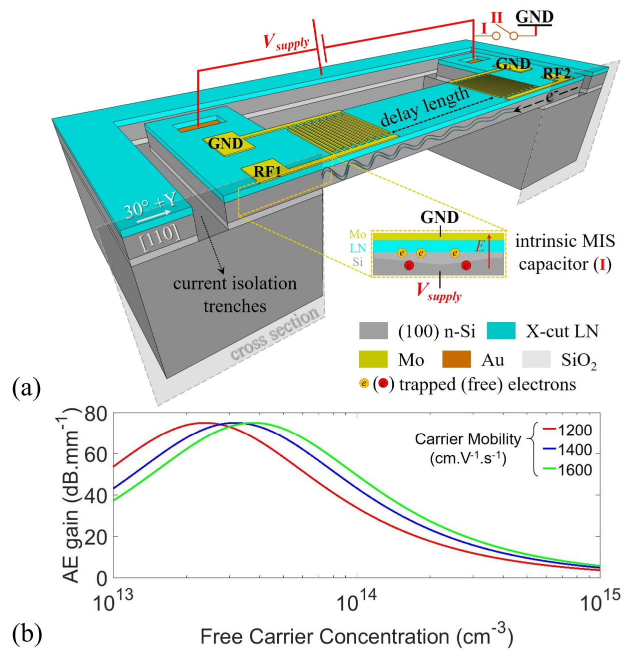

Fig. 1. (a) Schematic of AEDL showing the MIS capacitor used for adjusting the carrier density in the Si. This can be achieved by closing the switch to state (I), i.e. making the negative terminal of V_{supply} the same as ground. (b) Theoretical AE gain as a function of free carrier density for three values of carrier mobility, highlighting the importance of adjusting carrier density through the MIS capacitor for improving the AEDL efficiency.

II. DESIGN AND FABRICATION OF THE AEDL

The AEDLs of this work are fabricated on a substrate that is comprised of a 1-µm X-cut LN film which is bonded to a 3-µm (100) silicon-on-insulator (SOI) wafer by NGK Insulators LTD. The Si layer is n-type doped (n~8E14 cm^{-3}). The LN film is oriented in a way that the propagation axis of the AWs in the AEDLs is aligned to both the [110] Si plane and the 30° off +y-axis direction of LN, which yields the highest electromechanical coupling for excitation of the fundamental symmetric Lamb waves (S0) [6]. The top interdigital transducers (IDT) are made of sputtered molybdenum (Mo) and

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gold (Au) contacts to Si are made by ion milling the LN film using a combination of argon and fluorine plasma. The device-cavity is defined by dry-etched trenches in the LN-silicon stack and the devices are released by backside DRIE followed by buffered oxide etching of the buried oxide layer. The fabrication steps are summarized in Fig. 2 (a)-(f) and the optical micrograph of an AEDL is shown in Fig. 2 (g). The delay length, determined by the separation between the two IDTs, is 400 µm for the device studied here, the width of the AEDL is 200 µm, and the IDT finger pitch is 5 µm which defines the center frequency to be ~645 MHz. By applying a DC voltage (V_{supply}) to the Si layer a current will be injected in Si while the AW is launched in the composite structure by IDTs on LN.

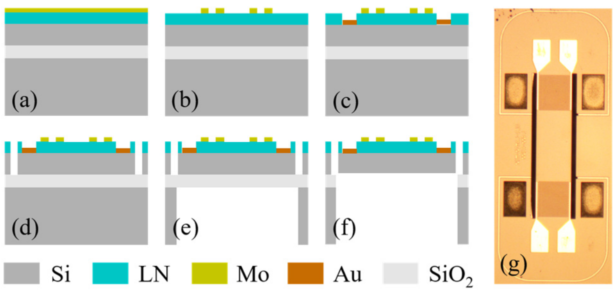

Fig. 2. (a) - (f) Schematic depiction of the fabrication process steps; (g) micrograph of the AEDL studied herein.

III. Characterization of the AEDL

The device under test is characterized in two configurations: one with the negative terminal of V_{supply} connected to the RF signal ground (state I) and second when V_{supply} is isolated from signal (state II). The transmission response $|S_{21}|$ of the AEDL for the two configurations while increasing the V_{supply} from 0 V to 100 V in 25 V increments along with the measured currents in each case are presented in Fig. 3. The value of V_{supply} is measured to be much larger than the voltage across the AEDL length as a result of the poor contact between the DC probe and Au-overlaid Si windows. It is evident that the currents in case (I) are lower than those of the case (II) due to the carrier depletion as the DC electric field will be induced in Si across the MIS capacitor in the first configuration. The measured AE gain and NTR as a function of V_{supply} is plotted in Fig. 4 (a); case (I) is plotted in red and case (II) in blue. It is evident that at V_{supply}=25 V the AE gain in the depleted case (I) is ~1.5 times that of (II) while consuming slightly less current (~60% efficiency improvement). Further depletion, however, reduces the gain relative to (II). To further evaluate such hypothesis, a bias is applied to the top electrodes to confirm the effect of carrier depletion and accumulation. Consistent improvement and degradation of the AE, respectively, are observed for such cases. Fig. 4 (b) compares the insertion loss, reverse isolation, and return loss of the device in the two configurations at V_{supply}=100 V which shows degradation of AE gain upon deep depletion.

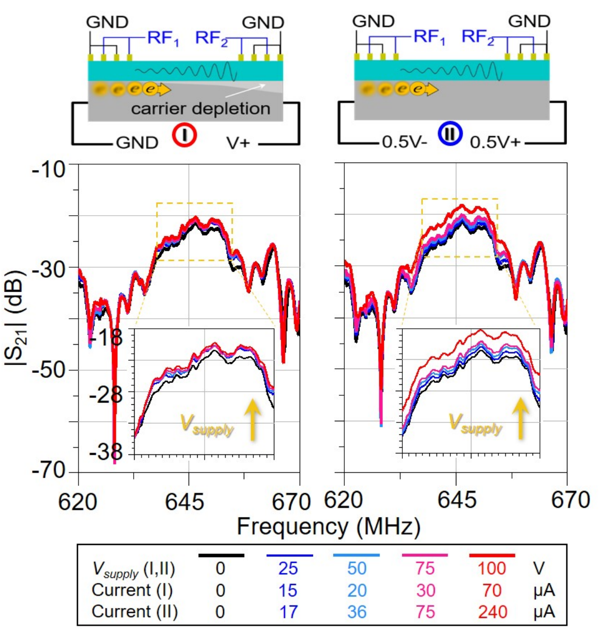

Fig. 3. Transmission of AEDL tested in the two configurations of applying V_{supply} with the corresponding measured currents. As schematically displayed at the top, in (I) the vertical electric field component results in depletion of Si.

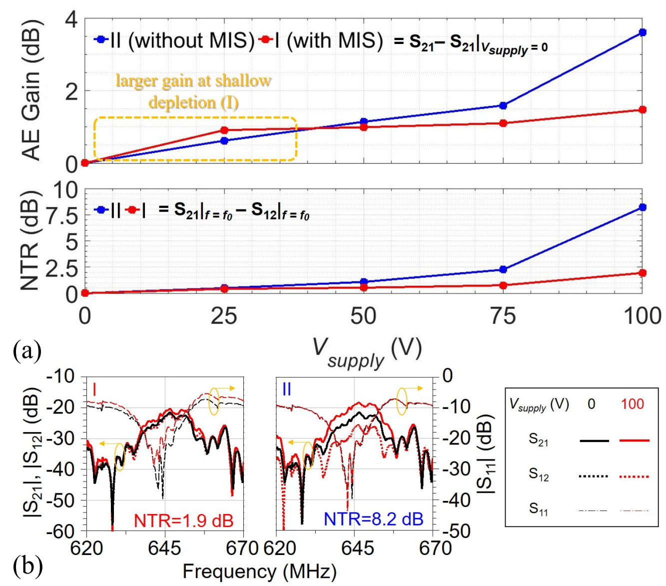

Fig. 4. (a) Measured AE gain and NTR at different values of V_{supply} for the two cases: red line for (I) and blue line for (II); A higher efficiency is observed for shallow depletion. (b) Scattering parameters of the device at V_{supply}=100 V for the two cases showing the loss of efficiency at deep depletion.

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