Cadmium Telluride Cells on Silicon as Precursors for Two-Junction Tandem Cells

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***Abstract*—Cadmium telluride and silicon are among the widely used absorber materials in photovoltaic industry. A tandem solar cell of these two can absorb significant portion of solar spectrum to yield high efficiency due to the added voltage of the two solar cells. On basis of low-cost production, a CdTe/Si cell has the potential to produce low-cost and high efficiency tandem PV. The CdTe top cell in a substrate configuration is essential to achieve a tandem between CdTe and Si. A functional CdS/CdTe solar cell in the substrate configuration was fabricated on a Si wafer. Current -Voltage measurements show a diode-like curve with lower J-V parameters compared to standard CdS/CdTe cells. SCAPS simulations were performed to identify possible reasons for poor performance and help improve the device performance.**

***Index Terms*—tandem, substrate, Two-Junction, CdTe, Silicon**

I. Introduction

Cadmium telluride (CdTe) is a direct band gap (1.5 eV) semiconductor with a large absorption coefficient ($\sim 10^5$ cm^{-1}). A few microns of CdTe is enough to absorb significant amount of photons of wavelength below 840 nm making it an attractive solar absorber. Devices with efficiency greater than 20 % have been fabricated at Colroado State Univeristy (CSU) [1]. Si solar cells with efficiency greater than 25 % have been fabricated [2] with thickness $\sim$ 200 μm with band gap of 1.1 eV and cutoff wavelength of 1130 nm, close to their theoretical limits [3]. This makes a CdTe top cell with Si bottom cell an attractive prospect for tandem device. Along with providing mechanical support to the thin CdTe top cell, a Si bottom cell should assist in the voltage addition in tandem with CdTe top cell with incorporation of a suitable intermediate tunnel junction. The sub-band-gap photons for CdTe top cell will be absorbed by the Si bottom cell. With assistance of proper interconnect tunneling layers, a current across a two terminal CdTe/Si tandem device can be extracted. The overall efficiency should be enhanced primarily due to the addition of voltage from the two cells. The following points are key to the realization of the CdTe/Si tandem device:

- Fabrication of the substrate configuration of the CdTe on a Si substrate.
- Study of the intermediate conduction layers for the current transport and voltage addition between the two cells.
- Impact and mitigation of degradation of Si bottom cell due to fabrication of CdTe top cell.

Here, we present the results of fabrication of substrate CdTe top cell on Si wafers.

II. Experiment :CdTe top cell in substrate configuration

CdTe solar cells at CSU is traditionally grown in a superstrate configuration on soda lime glass via closed space sublimation (CSS) close to 480 °C using an inline single vacuum system with multiple CSS stations [4]. For the purpose of a CdTe/Si tandem, however, the CdTe top cell needs to be fabricated in a substrate configuration. Deposition of CdTe on a Si wafer of thickness 150 μm was performed for these experiments. A thin layer of intermediate conductive oxide was sputtered on Si wafers and CdTe of thickness 2.5 μm was deposited with CSS. Subsequent $CdCl_2$ passivation was performed and devices were finished by chemical bath deposition (CBD) of 100 nm of CdS. A 200-nm transparent conductive oxide of ZnO:Al was deposited by RF sputter for the front contact. After a grid of evaporated Al to make ohmic contact, small area devices of 0.5 cm^2 were isolated. A schematic of the device structure is presented as in Fig 1(a) whereas the proposed tandem device with the CdTe top cell and a bilayer of p^+-ZnTe:N/ n^--ZnO:Al intermediate tunnel junction is shown in Fig. 1(b) [5].

III. Results

Initial attempts to deposit CdTe on a bare Si at the standard deposition temperature suffered due to adhesion problems.

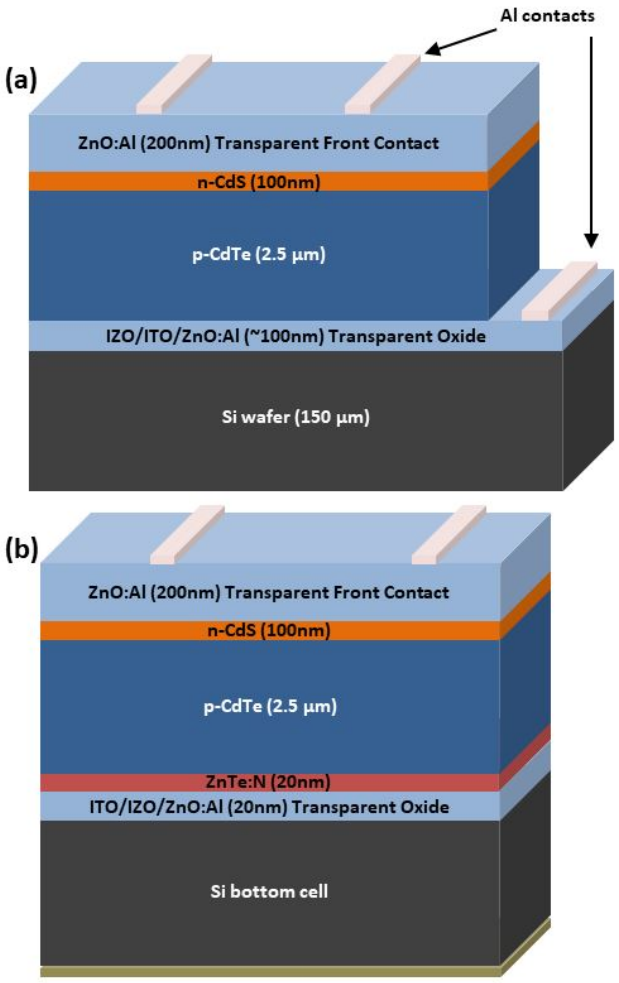

Fig. 1. (a) Schematic of the substrate CdTe top cell (b) Proposed tandem cell with ZnTe:N/TCO intermediate connecting layer

Lowering the growth temperature to 430°C allowed the deposition of CdTe. However, the CdTe films delaminated after subsequent $CdCl_2$ treatment. The introduction of a thin intermediate transparent oxide layer of indium-doped zinc oxide (IZO) helped with adhesion and conformal growth of the CdTe fims. The intermediate oxide layers have high conductivity which can act as terminals for the electrical measurements of the finished CdTe top cells. Such a conductive oxide layer is vital for the formation of the interconnecting layers for the current transport and voltage addition by formation of tunnel junction between the two cells.

Deposition of CdTe and subsequent $CdCl_2$ passivation at two different temperatures of 430 °C and 480 °C was performed as temperature play a vital role in the device perormance. While smaller grain sizes were observed at lower growth teperature of 430 °C, SEM imaging in Fig. 2 clearly shows that the typical depostion temperature of 480 °C yields in larger grains which are vital for better devices. Subsequent $CdCl_2$ passivation which results in recrystallization of the

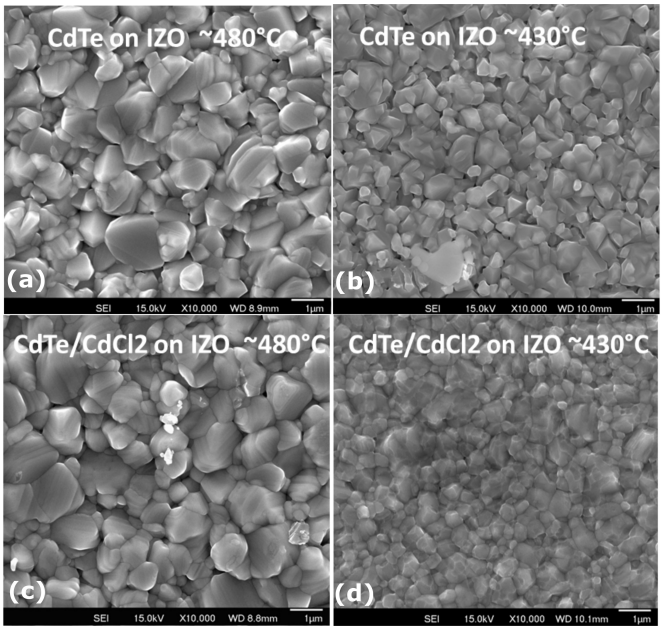

Fig. 2. SEM of as deposited CdTe on a Si wafer with an intermediate oxide layer of IZO at two temperatures of 480 °C and 430 °C. Top row is as deposited CdTe and bottom row is after $CdCl_2$ treatment.

as-deposited polycrystalline CdTe was observed. A separate experiment where variation in deposition temperature of CdTe and subsequent $CdCl_2$ on Si wafers was conducted, which showed minimal degradation of the Si wafer [6], [7] which is essential in fabrication of CdTe/Si tandem solar cell.

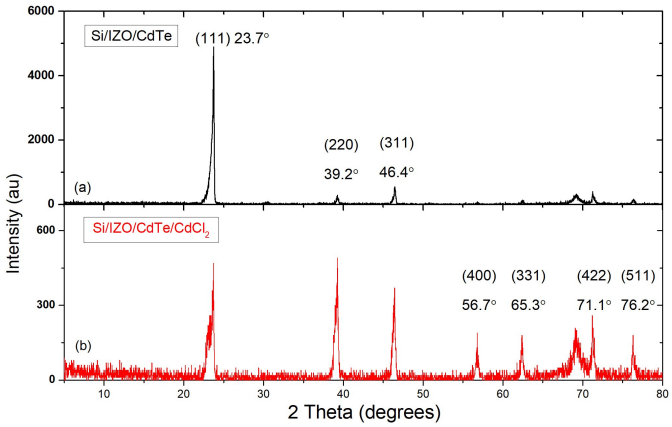

Fig. 3. (a)XRD peak analysis of as deposited CdTe on a Si with thin intermediate oxide of IZO at 480 °C (b) XRD peaks after subsequent $CdCl_2$ treatment shows recrystallization and appearance of new CdTe grain orientations.

$CdCl_2$ treatment is a vital process in CdTe device fabrication. The process passivates the CdTe grain boundaries by decorating them with Cl atoms. It also recrystallizes the grains structures to a more preferred orientations. Here we found that for a substrate CdTe configuration, the $CdCl_2$ treatment has a similar effect to the grain structures as that of superstrate configuration of CdTe. The as deposited CdTe is dominated by

the (111) CdTe grain orientation but after the $CdCl_2$ treatment the other orientations also have a significant presence as shown in Fig. 3.

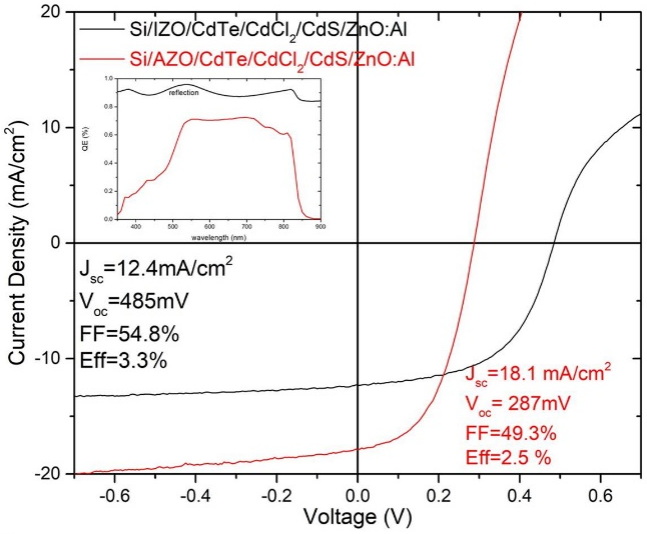

Fig. 4. Current Voltage (J-V) measurement of devices with two different intermediate oxide layer IZO and AZO. The inset shows the QE of substrate CdTe.

CdTe top cells in the substrate configuration were fabricated using two different oxides, alumunium-doped zinc oxide (AZO) and indium-doped zinc oxide (IZO) to study the impact of the intermediate oxide layer. A basic diode-like curve of a good solar cell was measured for both devices as shown in Fig. 4. The device with AZO has larger short circuit current but a lower open circuit voltage compared to the the device with IZO. The low current is likely due to the cell not making electrical contact over its full areas. The low fill factor can be attributed to the excessive recombination of the photo-generated electrons and holes. Despite these low efficiencies these cell structure are valuable for the aspect of growing a functional CdS/cdTe solar cell on a Si bottom cell. The QE in the inset of Fig.4 has a clean cutoff at around 830 nm, the wavelength corresponds to that of CdTe bandgap. The curve has a reduced QE at around 510 nm typical of CdS parasitic absorption. The gap between the reflection curve QE curve is an indication of full area of cell not contributing to the current.

J-V parameters obtained to date have been inferior to the typical CdS/CdTe solar cells, indicating need for optimization. To identify the potential reasons for the lower performance, a SCAPS simulation was performed in the device stack as shown in Fig. 1(a) [8]. The band diagrams obtained in Fig. 5(a) shows a comparison between energy band diagrams for standard CdS/CdTe device and the device structure as shown in Fig. 1(a). The intermediate conductive oxides are n-type meaning that the band will bend downwards significantly at the back in comparison to the standard CdS/CdTe devices. This unfavorable band bending leads to an increased recombination at the back of CdTe top cell and thus reduced device performance as seen in the J-V curves in Fig. 4. Such a band bending at the back can be mitigated by use of a back surface field with a highly doped p-type semiconductor. Highly doped p-type semiconductor will pin the Fermi of CdTe top cell at the intermediate connection and help reduce recombination at the back junction. Wider band gap p-type semiconductor at the back of CdTe adjacent to the intermediate oxide layer will also help form the tunnel junction which is vital for optical transmission of sub-band-gap photons, current transport and voltage addition across the two cells, as was shown in Fig. 1(b). The band diagram for a functional CdTe/Si tandem where the holes in valence band of CdTe will recombine with electrons in conduction band of Si via a recombination center of p_{++} ZnTe:N back surface field and a n_{++} TCO is as shown in Fig. 5(b).

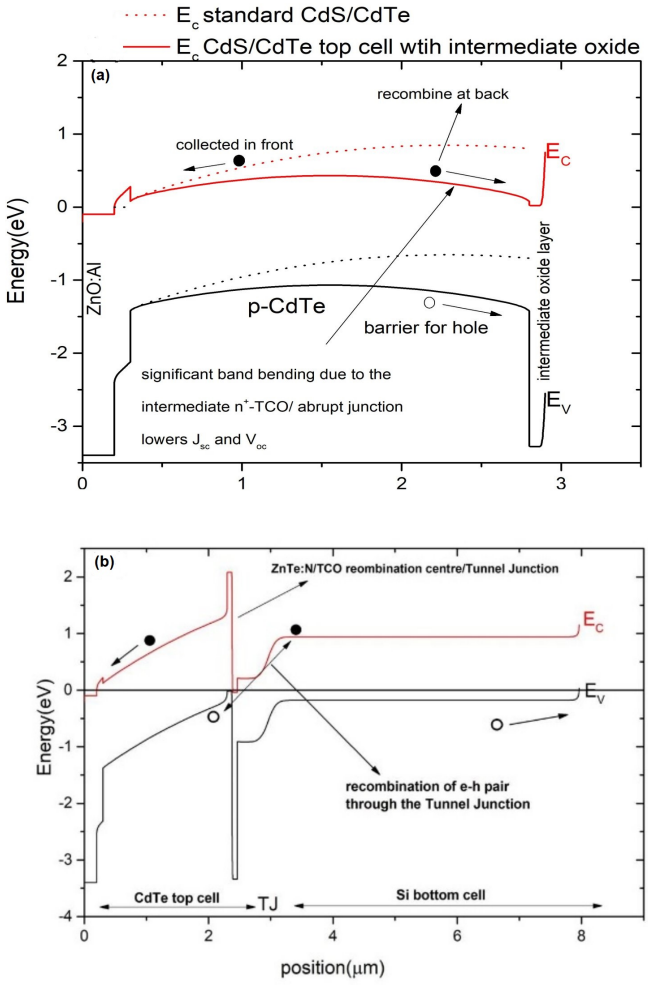

Fig. 5. (a) Band diagram of top CdS/CdTe with intermediate oxide layers. Dotted lines represent the energy band diagram for the typical CdS/CdTe while the solid lines represent the semiconductor stack presented in Fig. 1(a) with intermediate oxide layer of IZO or AZO. (b) Band diagram for a fully functional CdTe/Si tandem cell with intermediate tunnel junction representative of Fig. 1(b)

IV. CONCLUSION

A functional CdS/CdTe solar cell in a substrate configuration was fabricated on silicon as a first step towards CdTe/Si

tandem solar cell. Lower performance of the fabricated CdTe top cell was due to the unfavorable band bending at the back of the CdTe top cell. A proper back surface field, however, should enable the formation of tunnel junction and a better performing CdTe top cell that can be fabricated on a working Si bottom cell to make a CdTe/Si tandem device. For a two junction tandem solar cell, favorable current matching for a 1.1 eV bottom cell is possible with a top cell of band-gap 1.7 eV. Alloying of CdTe with Mg or Zn to form a ternary alloy can widen the band gap of CdTe to a suitable 1.7 eV [9], [10].

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