Accelerating Electromigration Aging: Fast Failure Detection for Nanometer ICs

Sheriff Sadiqbatcha, *Student Member, IEEE*, Zeyu Sun, *Student Member, IEEE*, and Sheldon X.-D. Tan, *Senior Member, IEEE*

***Abstract*—For practical testing and detection of electromigration (EM) induced failures in dual damascene copper interconnects, one critical issue is creating stressing conditions to induce the chip to fail exclusively under EM in a very short period of time so that EM sign-off and validation can be carried out efficiently. Existing acceleration techniques, which rely on increasing temperature and current densities beyond the known limits, also accelerate other reliability effects making it very difficult, if not impossible, to test EM in isolation. In this paper, we propose novel EM wear-out acceleration techniques to address the aforementioned issue. First, we show that multisegment interconnects with reservoir and sink structures can be exploited to significantly speedup the EM wear-out process. Based on this observation, we propose three strategies to accelerate EM induced failure: 1) reservoir-enhanced acceleration; 2) sink-enhanced acceleration; and 3) a hybrid method that combines both reservoir and sink structures. We then propose several configurable interconnect structures that exploit atomic reservoirs and sinks for accelerated EM testing. Such configurable interconnect structures are very flexible and can be used to achieve significant lifetime reductions at the cost of some routing resources. Using the proposed technique, EM testing can be carried out at nominal current densities, and at a much lower temperature compared to traditional testing methods. This is the most significant contribution of this paper since, to our knowledge, this is the only method that allows EM testing to be performed in a controlled environment without the risk of invoking other reliability effects that are also accelerated by elevated temperature and current density. The simulation results show that using the proposed method, we can reduce the EM lifetime of a chip from ten years down to a few hours (about $10^5\times$ acceleration) under the 150 °C temperature limit, which is sufficient for practical EM testing of typical nanometer CMOS ICs.**

***Index Terms*—Accelerated testing, atomic reservoirs, atomic sinks, back-end reliability, electromigration, failure analysis, integrated circuits, interconnects, stressing conditions.**

I. Introduction

ELECTROMIGRATION (EM) is the top reliability concern for copper-based back-end-of-the-line (BEOL) interconnects, both for current and future ICs in the sub-10-nm realm. 2015 ITRS-interconnect predicted that EM lifetime of interconnects in VLSI chips will be reduced by half for each generation of nodes [1]. This is primarily due to increasing current densities and shrinking wire cross-sections, which determine the critical sizes for EM effects. On the other hand, many applications, ranging from automotive to medical devices and aerospace equipment, require a very long lifetime and have very demanding reliability requirements. As a result, testing and verification of reliability, especially EM-reliability, of VLSI chips used in those applications becomes critical.

For many practical applications, reliability of ten years or more is typically expected [2]. However, testing a chip for the duration of its projected lifetime is not practical. Hence, accelerated testing and stressing-conditions are needed to shorten the validation process. The main motivation of this paper is to independently accelerate EM specific failures in practical VLSI chips under allowed chip working conditions so that EM failure effects can be fully verified and validated. If an acceleration from ten years to a few hours is expected, one needs a time-to-failure (TTF) reduction in the order of $10^5\times$. However, this is quite challenging to achieve in reality, especially when we want the chip to fail exclusively under EM wear-out. The reason is that the traditional acceleration methods, using high temperature and high voltage, also accelerate other reliability effects, such as time dependent dielectric breakdown (TDDB) for dielectrics, biased temperature instability (BTI), and hot carrier injection (HCI) for CMOS devices. As a result, we would like to limit the testing temperature to be within the typical working temperature range of CMOS devices, which is from −55 °C to 125 °C with 150 °C being the maximum temperature limit [3], [4].

There are two main challenges. First, we need scalable EM models which are accurate both across the high stress conditions used during testing, as well as the normal use conditions. The model data from these acceleration tests can then be used to predict the actual TTF when the chip is subjected to a normal workload. Existing Black and Blech-based empirical EM models [5], [6] are considered too conservative. Moreover, they do not fit well over a wide range of stressing conditions as the activation energy and current exponents are stress-condition dependent [7]. This will make it difficult to apply the results obtained from the high stressing conditions to the normal operating conditions. Second, once we have an accurate EM model, we need to find realistic EM stressing conditions and other accelerating techniques to achieve the

Manuscript received October 1, 2018; revised December 31, 2018; accepted March 4, 2019. Date of publication March 26, 2019; date of current version March 18, 2020. This work was supported in part by NSF under Grant CCF-1527324 and Grant CCF-1816361, and in part by The Defense Advanced Research Projects Agency (DARPA) under Grant HR0011-16-2-0009. This paper was recommended by Associate Editor N. Wong. *(Corresponding author: Sheldon X.-D. Tan.)*

The authors are with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA 92521 USA (e-mail: sheldon.tan@ucr.edu).

Digital Object Identifier 10.1109/TCAD.2019.2907908

desired reduction in TTF. This has to be done while ensuring that the chip only fails under EM, not other reliability effects. Hence, the stressing condition should only accelerate EM, which is not the case for existing methods that use high temperature and voltage-based stressing conditions.

Recently, a number of physics-based EM models and assessment techniques have been proposed [8]–[20]. Huang *et al.* [9], [12] proposed a compact EM TTF model based on the approximate closed form solution of Korhonen's equation for a single wire and studied the impact that wire redundancy has on EM failure in the power grid networks [9], [12], [21]. This paper has been extended to multisegment wires [11] and time-varying current cases [15], [16]. Additionally, a numerical solution-based finite difference method [17] and Krylov subspace method [17] have been explored. These EM models are primarily based on the hydrostatic stress diffusion kinetics in confined metal wires and hence can consider stress evolution and distribution in entire interconnect structures consisting of many wire segments. This is in stark contrast with the traditional Black–Blech EM models, which can only consider isolated single segment wires. As a result, these open new ways to manipulate multisegment interconnect structures in order to achieve the desired stress and aging effects. Recently a very accurate three-phase EM model was proposed [8], [18], which better described the post-voiding wire resistance change behavior of copper dual damascene interconnects. We will utilize this EM model for the analysis performed in this paper.

Traditionally, for accelerating the EM failure process, raising temperature has been the most effective method as the EM effects are exponentially dependent on temperature. However, elevated temperature will lead to other failures, such as TDDB, very quickly. Moreover breaching the well-known thermal limits of semiconductor devices is not a reliable approach [3]. Increasing the current density is another way to accelerate EM wear-out. However, it is well-known that the impacts of current density is reversely proportional to the TTF under EM with current exponent between 1 and 2 [22]. This limits the impact of current density on acceleration. Furthermore, high current densities can lead to thermal runaway effects due to excessive Joule heating [23]. Hence, in order to ensure failure exclusively under EM, a new acceleration method is urgently needed, which can achieve the same reduction in TTF but at a much lower current density and temperature.

In this paper, we propose novel EM acceleration techniques based on stress engineering in the multisegment interconnect wires, by utilizing a recently proposed physics-based EM model [8], [18]. The significance of the proposed work is that it allows accelerated EM testing to be carried out at nominal current densities, and at a much lower temperature compared to traditional testing methods. Our specific contributions are as follows.

1) We show how reservoirs can be exploited to significantly increase hydrostatic stress on a wire leading to an accelerated EM wear-out process. To leverage this effect for accelerated EM testing, we propose a novel interconnect structure with one and two reservoir segments. We show how the desired reduction in TTF can be achieved by simply configuring the geometry of the proposed structure.
2) We demonstrate how a similar EM acceleration effect can be achieved using sink-based multisegment structures. We then propose our second EM acceleration technique that leverages these atomic sinks. The sink-based structures are more challenging to design since they require several parameters to be tuned to achieve the desired reduction in TTF. This will be discussed in detail in the latter part of this paper.
3) We then propose a third EM acceleration technique based on combining both reservoir and sink segments in one hybrid structure. We show that this structure significantly outperforms the previous two.
4) We show that, in general, 10% increase in temperature can achieve about $10\times$ reduction in TTF. However, on-chip temperature has an upper limit for the working operations of CMOS circuits. Hence, in this paper all the tests will be performed below 150 °C.
5) For practicality, all the structures proposed in this paper will be designed to operate under two modes: a) normal-use and b) acceleration. Under normal-use, the structures will meet the lifetime requirement of at least ten years. Under acceleration mode, the structures will fail quickly, within days or hours, while maintaining nominal current densities and stressing temperatures below 150 °C.

The simulation results show that by combining temperature and the aforementioned structure-based acceleration techniques, we can reduce the EM lifetime of a wire from ten years down to a few hours (about $10^5\times$ acceleration in TTF) under the 150 °C temperature limit. This, for the very first time, will afford us the ability to test EM under a controlled environment without the risk of invoking other reliability effects that are also accelerated by the traditional methods.

The rest of this paper is organized as follows. Section II reviews the recently proposed physics-based EM models and three-phase EM models used for multisegment copper interconnects. Section III presents our new atomic reservoir and sink enhanced EM acceleration techniques. Section IV presents the impact of temperature on EM wear-out. Section V presents the EM acceleration results from subjecting the proposed structures to the temperate-based stressing conditions. Section VI concludes this paper.

II. Review of EM Physics and Three-Phase EM Model

A. Review of EM Physics and Stress Modeling

EM is a physical phenomenon of the migration of metal atoms along the direction of the applied electrical field. Atoms (either lattice atoms or defects/impurities) migrate along the trajectory of conducting electrons. During the migration process, hydrostatic stress is generated inside the embedded metal wire due to momentum exchange between the electrons and lattice atoms. Over time, EM causes an accumulation of atoms at the anode and depletion at the cathode, resulting in compressive and tensile hydrostatic stress in the respective ends of the wire. When the stress exceeds the so-called critical stress

value, voids and hillocks will form at the cathode and anode nodes, respectively.

The traditional method of predicting TTF is based on approximations and statistical methods, such as Black's equation [5] and Blech's limit [6]. However, they are subject to growing criticism due to their over conservativeness and lack of consideration of multisegment interconnect wires [12]. To mitigate this problem, a number of new physics-based EM modeling techniques have been proposed [11]–[13], [17], [19], [21], [24]–[26] based on solving the Korhonen *et al.*'s hydrostatic stress diffusion equation [27]. Recently a three-phase EM model [18], [28], which better represents the wire resistance change over time, was proposed. This model will be discussed in the following section.

B. Three-Phase Physics-Based Compact EM Model for Multisegment Wires

In the existing physics-based EM models, the EM failure process in general can be viewed as two phases: 1) the nucleation phase, in which the void is generated after the critical stress is reached and 2) the growth phase, in which the void starts to grow. Existing compact EM models are also versed in terms of the two phases, where each phase is described by TTF as a function of current density and other parameters [12], [29]. However, such a simple EM model ignores the fact that when the void is nucleated or formed, it will not change the wire's resistance immediately. It has been experimentally observed that there exists a so-called *critical void size* [30], [31], which is typically the via-diameter or cross section area of the interconnect wire. Since the conductivity of Cu is much higher than the barrier layers, resistance of the wire does not change until the void grows to a point where its volume equals or becomes larger than the cross section of the via or wire. Only then will all the current start to flow over the thin barrier layer, which will lead to a very high current density and consequent Joule heating. The Joule heating in turn will lead to a small resistance jump, indicating the end of this phase [see Fig. 1(a)]. Fig. 1(b) shows the experimentally measured resistance change over time where the small resistance jumps are clearly visible. Also, sometimes the barrier layers are not very stable, due to manufacturing process variations, causing the barrier layer to quickly burn out resulting in an open circuit as is shown in Fig. 1(b) [31].

Based on these observations, a three-phase EM model has been proposed for a single segment wire [18], [28]. The new model has three phases as shown in Fig. 1(a): 1) the *nucleation phase* from $t = 0$ to t_{nuc}; 2) the *incubation phase* from t_{nuc} to t_{inc}; and 3) the *growth phase* from t_{inc} to t_{50} (or t_{gro}), together indicate the TTF in statistical terms (50% of the samples fail). This model was later extended to consider more general multisegment interconnect structures [32] (i.e., Fig. 2). We remark that the three-phase EM model is more consistent with the measured wire resistance change over time than existing physics-based EM models, such as [12], [17], and [24], which do not consider the incubation time. The incubation time, which is the time between nucleation time and the time when the wire resistance changes, can be significant for the

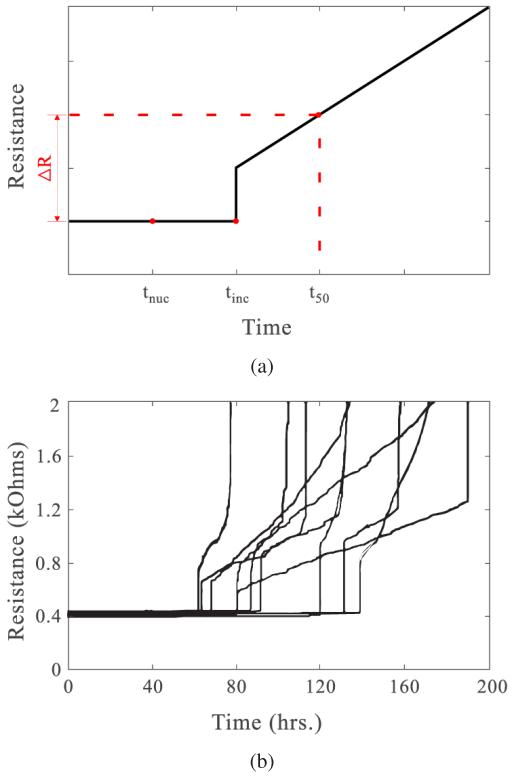


Fig. 1. (a) Illustration of resistance change over time, courtesy of [18]. (b) Experimentally measured resistance change over time, courtesy of [31].

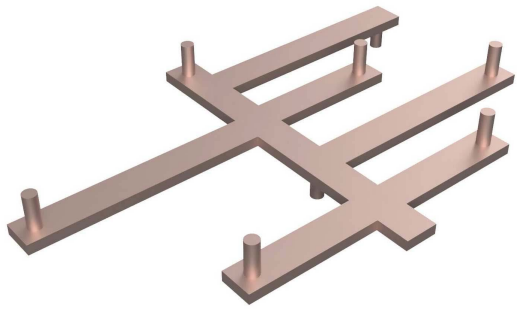


Fig. 2. Illustration of a multisegment interconnect wire structure.

overall TTF analysis and is dependent on the wire structure as well. As a result, the three-phase EM model is more accurate than other physics-based models and will be used for the proposed EM acceleration work in this paper.

C. Multimode Failure Scheme

The three-phase EM model, discussed in the previous section, allows us to consider a robust multimode failure scheme. Typically, only parametric failures, or late-failures (LFs), are considered for EM wear-out where, as the void grows, resistance of the wire slowly increases and reaches a point where the circuit can no longer function as intended. This type of failure occurs in the so called via-below structures as shown in Fig. 3(a), where the flow of electrons is from a lower metal layer to a higher one (hence this structure is also called an upstream structure). In this case, even when the void grows to

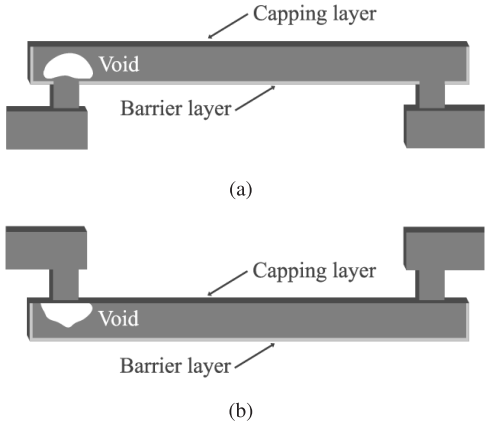


Fig. 3. (a) Via-below or upstream and (b) via-above or downstream wire structures showing void formations.

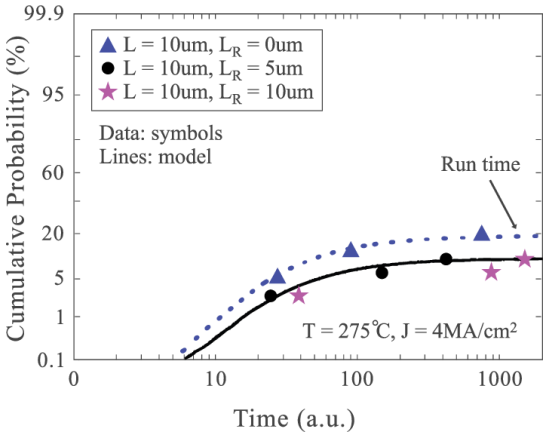


Fig. 4. Experimentally obtained failure distribution for a two segment wire with a reservoir. L_r is the length of the reservoir segment. Courtesy of [33].

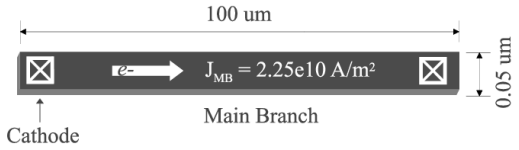


Fig. 5. Active interconnect wire segment.

its critical size (cross sectional area or via diameter), current can still flow through the barrier layer, but, at a much higher resistance. Here the wire can be considered as failed at the end of the growth phase, which, typically, is the point where the wire's resistance increases by 10% (or other user defined criteria). However, there exists another type of failure, called early failure (EF), which is observed in the so called via-above structures like the one shown in Fig. 3(b). Here the electron flow is from a higher metal layer to a lower one (hence it is also called a downstream structure). Since a nonconductive capping layer is applied between the layers of metallization in the dual damascene process, once the void reaches the critical size, we instantly see an open circuit because current cannot flow though the dielectric capping layer. Therefore, in such structures the wire fails at the end of the incubation phase. This critical distinction can only be accounted for accurately using the new three-phase EM model. More detailed study on these failure schemes can be found in [30] and [31]. In this paper, we present TTF results for both the via-above (TTF_{EF}) and via-below (TTF_{LF}) topologies.

III. Atomic Reservoir and Sink Enhanced EM Acceleration

The new EM acceleration techniques are inspired by the observation that atomic reservoir and sink segments in a multi-segment interconnect wire can have a significant impact on the hydrostatic stress evolution in the wire [33], [34]. These structures are good candidates for accelerating EM failure effects as they offer a great deal of flexibility and configurability on the EM lifetime of active interconnects without affecting their normal functionality. EM induced hydrostatic stress on the main conductive wire segments that share a terminal with the reservoir and sink structures can be drastically altered using several design parameters.

The impact of these structures is analyzed in the following sections. The unique properties of reservoirs and sinks are then exploited in designing structures for accelerated EM testing. The proposed structures are designed to operate under two modes: 1) normal use and 2) acceleration. The configurable nature of these structures allow them to be designed for a lifetime of 10+ years (typical lifetime requirement for ICs) under normal use, and just a few days or hours under acceleration mode (or as desired for the application at hand). Note, temperature of 353 K (∼80 °C) is assumed for all the analysis in this section. Temperature configuration for actual EM acceleration tests will be discussed in Section IV.

A. Configurable Reservoir-Based EM Failure Acceleration

Reservoir structures (passive interconnect segments) are typically added to the cathode terminal of active interconnect wires that are vulnerable to EM wear-out. These structures decrease the rate of hydrostatic stress evolution on the active wires, consequently prolonging nucleation time. Fig. 4 shows the measured failure distribution of a two segment wire with reservoir segments of different lengths [33]. As the results show, the lifetime of the wire increases when the reservoir is present ($L_r > 0$). The more reservoir area (longer length in this case), more the lifetime is prolonged.

To further demonstrate the impact of reservoir segments, let us consider an active interconnect segment (main-branch), with no reservoir structure, shown in Fig. 5. With the previously discussed three-phase EM model, transient stress across this wire segment can be computed using a numerical approach, such as finite element or finite difference. Fig. 8(a) shows the hydrostatic stress evolution over time at the cathode terminal computed using finite element analysis. Only the cathode node is shown since, in most cases, void is nucleated here as the cathode end of the wire experiences the maximum tensile stress. The results for this structure show void nucleation, t_{nuc}, at 1.68×10^3 h. Post nucleation, the incubation, t_{inc}, and growth, t_{gro}, times can be calculated using the closed form equations discussed previously. For this structure the

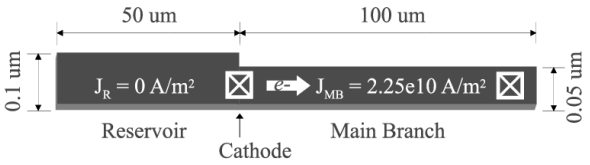


Fig. 6. Reservoir at the cathode of an active interconnect wire.

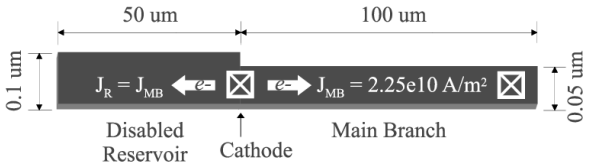


Fig. 7. Disabled reservoir at the cathode of an active interconnect wire.

results are: $t_{\text{inc}} = 1.68 \times 10^4$ h and $t_{\text{gro}} = 1.56 \times 10^4$ h. Therefore the effective TTF for early and late failure cases are: $\text{TTF}_{\text{EF}} = 1.85 \times 10^4$ h and $\text{TTF}_{\text{LF}} = 3.41 \times 10^4$ h for the interconnect wire shown in Fig. 5.

Let us now consider the effect of adding a passive reservoir segment to the cathode terminal of this wire. For now, let us arbitrarily set the reservoir to be half the length and twice the width of the active wire ($W_R = 0.1$ um and $L_R = 50$ um) as shown in Fig. 6. Transient stress analysis at the cathode of this new structure shows nucleation delayed to $t_{\text{nuc}} = 1.29 \times 10^4$ h as shown in Fig. 8(b). Incubation and growth times stay the same since these depend on total atom flux at the cathode and at this point, only the main-branch is carrying current and therefore contributing to the effective flux. Nonetheless, delaying nucleation time prolongs the wire's lifetime: $\text{TTF}_{\text{EF}} = 1.72 \times 10^4$ h and $\text{TTF}_{\text{LF}} = 3.28 \times 10^4$ h. This is the typical application for reservoir segments.

Interestingly, if we design the structure shown in Fig. 6 such that current in the reservoir segment can be activated during runtime, we can exploit a very unique property. Let us consider the structure shown in Fig. 7, which is identical to the structure in Fig. 6 but with current flow enabled in the reservoir segment. Let us arbitrarily set the current density in the reservoir segment (disabled reservoir) to be the same as the main-branch, but in the opposite direction. We call this a disabled reservoir since this configuration effectively disables the benefits of the reservoir segment, shifting nucleation time back to what was originally observed from the structure in Fig. 5. This acceleration in nucleation time is shown in Fig. 8(c). Moreover, the additional atom flux generated by the electron flow in the reservoir segment also accelerates the incubation and growth times: $t_{\text{inc}} = 1.41 \times 10^3$ h and $t_{\text{gro}} = 5.19 \times 10^3$ h. The effective TTF now becomes: $\text{TTF}_{\text{EF}} = 3.08 \times 10^3$ h and $\text{TTF}_{\text{LF}} = 8.28 \times 10^3$ h. This is a significant reduction in lifetime achieved, at nominal current density and temperature, by merely switching on current flow in the reservoir segment. This critical observation is the basis for our reservoir-enhanced EM acceleration technique.

Based on this analysis, we propose a configurable two-segment interconnect structure shown in Fig. 9 [32]. The structure consists of a two segment wire (one reservoir and one main-branch), one MOSFET device (switch to disable the reservoir) and two resistors R_1 and R_2 to configure the currents in the two wire segments. The bottom half of Fig. 9 shows the 3-D view of this design. During normal use, the reservoir will remain passive (zero current density). Once acceleration (Acc.Signal) is activated, the current density in the reservoir will become nonzero, thus disabling the reservoir and accelerating EM wear-out.

In addition to the simple two-segment interconnect structure, we further propose the three-segment configurable interconnect structure shown in Fig. 10, with two reservoir segments. Here, the configurable circuity is omitted for the sake of better presentation. This multisegment design is meant to show both the robustness of the EM model used in this paper,

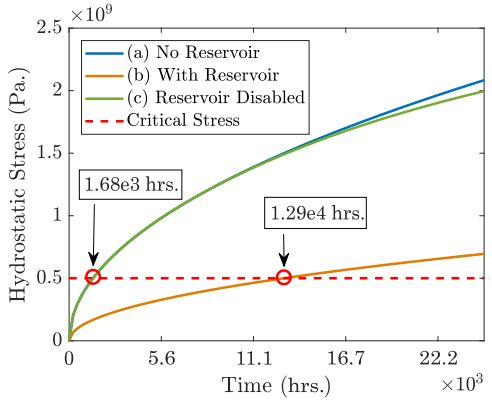


Fig. 8. Impact of reservoir on nucleation time.

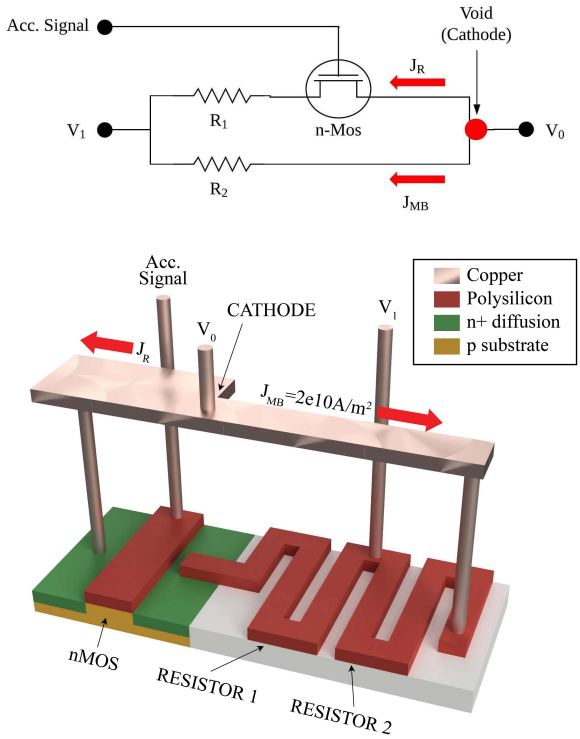


Fig. 9. Proposed configurable reservoir-based EM wear-out acceleration circuit (for illustration only; components not drawn to scale with respect to each-other).

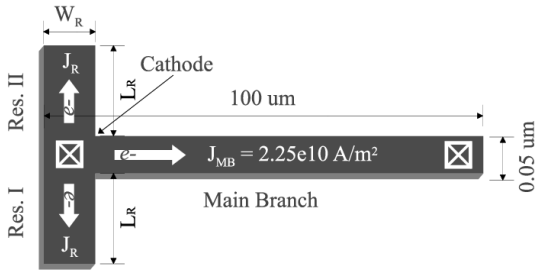


Fig. 10. Proposed EM acceleration structure with two reservoir segments.

as well as the flexibility the circuit designers have to design such reservoir structures for EM acceleration. Typically, circuit designers work under several constraints where optimization between critical parameters is crucial. The configurable nature of the proposed structure naturally allows for optimization between geometry, current density, and desired lifetime under normal use and acceleration modes.

As mentioned previously, the proposed structure will be designed to operate under two modes: 1) normal use and 2) acceleration. Under normal use (no current in reservoir), it is critical to ensure that the structure will have a lifetime of at least ten years (or as needed for the given application). Under acceleration (current enabled in reservoir), we want the structure to fail quickly (typically within days or hours). Hence, the goal is to find a configuration (W_R, L_R) that will meet these requirements.

Traditionally, current density of the main branch, J_{MB}, is significantly increased to achieve EM acceleration. However, this method also accelerates other reliability effects and, above a certain threshold, leads to Joule heating causing additional problems. Hence, we will fix J_{MB} to be the same under both normal use and acceleration modes. For acceleration mode we will simply activate current in the reservoir such that $J_R = 0$ becomes $J_R = J_{\text{MB}}$. Indeed, J_R can be set higher than J_{MB} as long as it abides by the design rules (i.e., Synopsys 32-nm PDK [35]).

As shown in Fig. 11, the proposed structure gives the circuit designer a great deal of flexibility in achieving the desired TTF for the application at hand. For instance the configuration $W_R = 0.3$ um and $L_R = 18$ um results in $T_{\text{nuc}} = 8.31 \times 10^4$ h, $T_{\text{inc}} = 4.17 \times 10^3$ h, and $T_{\text{gro}} = 1.56 \times 10^4$ h ($\text{TTF}_{\text{EF}} \approx 10$ years, $\text{TTF}_{\text{LF}} \approx 11.7$ years) under normal use, and $T_{\text{nuc}} = 1440$ h, $T_{\text{inc}} = 325$ h, $T_{\text{gro}} = 1197$ h ($\text{TTF}_{\text{EF}} \approx 73.6$ days, $\text{TTF}_{\text{LF}} \approx 123.5$ days) under acceleration mode. TTF can be reduced a little further with larger reservoirs, for instance the configuration $W_R = 1$ um and $L_R = 18$ um results in $T_{\text{nuc}} = 1427$ h, $T_{\text{inc}} = 103$ h, $T_{\text{gro}} = 381$ h ($\text{TTF}_{\text{EF}} \approx 63.8$ days, $\text{TTF}_{\text{LF}} \approx 79.6$ days). However, bear in mind, this was achieved at a working temperature of 353 K (~80 °C), this structure under burn-in conditions will yield a failure time that is much lower. These testing conditions will be discussed in detail in the next section.

Note, we can make a critical observation from the results shown in Fig. 11. For the proposed structure operating under normal mode [Fig. 11(a)], the results show that the TTF is a

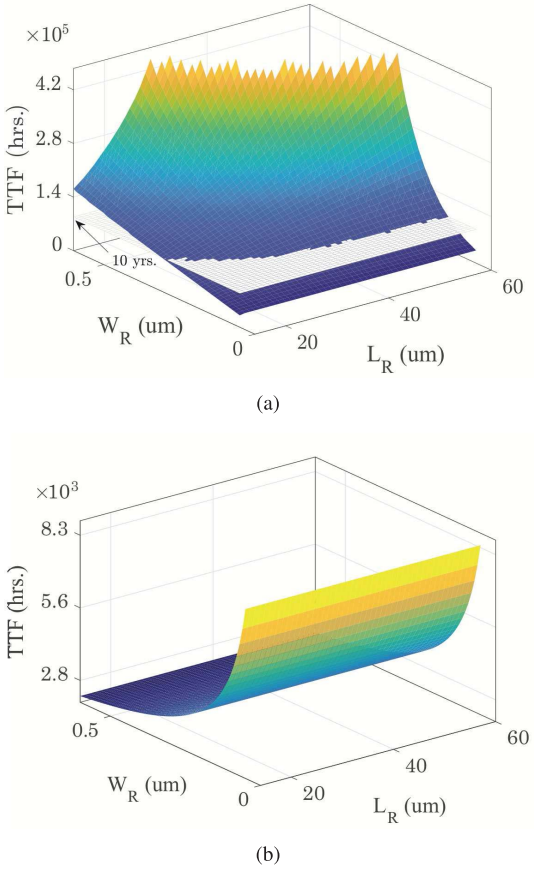


Fig. 11. TTF_{LF}. (a) Normal use. (b) Acceleration mode.

function of reservoir area. However, under acceleration mode [Fig. 11(b)], it is clear that TTF is a function of just the reservoir width, not its length. This is because the acceleration in nucleation time is caused by the additional atom flux through the reservoir's cross section at the cathode boundary of the active wire. The additional length of the reservoir is merely there to ensure that the structure meets the lifetime requirement for normal use (10+ years or immortality); it has no impact on acceleration. This observation will be exploited later with the hybrid structure that combines both reservoir and sink segments.

B. Configurable Sink-Based EM Failure Acceleration

Atomic sinks can be passive or active interconnect structures that, when added to the anode terminal of an active interconnect wire, can significantly increase the steady state tensile stress at the cathode. Additionally, adding a sink segment can reduce the compressive stress at the anode node, hence reducing the chance of hillock formations or extrusions.

Let us consider the structure shown in Fig. 12(a), where $L_{\text{MB}} = 5$ um, $W_{\text{MB}} = W_S = 0.05$ um, $L_S = 95$ um, and $J_{\text{MB}} = J_S = 2.25 \times 10^{10}$ A/m^2. This structure is indeed identical to the single main-branch that was shown in Fig. 5, but this time split into two segments. We will now refer to the first segment as the main-branch and the second segment as the active sink. As expected, hydrostatic stress evolution over time at the cathode

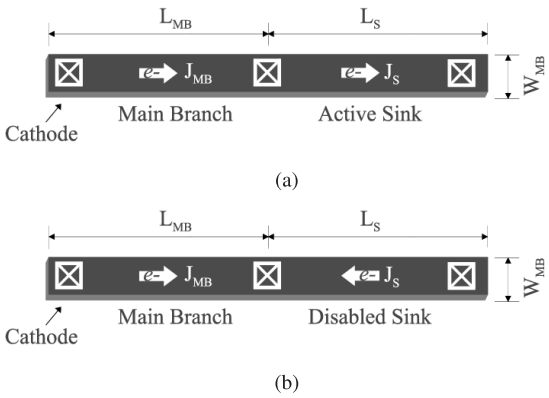


Fig. 12. Active interconnect wire with: (a) active sink at the anode and (b) disabled sink at the anode.

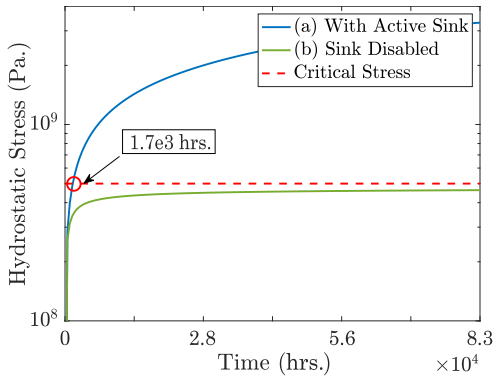


Fig. 13. Hydrostatic stress progression at the cathode with: (a) active sink at the anode and (b) disabled sink at the anode.

terminal [Fig. 13(a)] of the structure in Fig. 12(a) is identical to what was previously observed for the structure in Fig. 5.

However, if we can design this structure such that the direction of current in the sink segment can be reversed during runtime, then we can effectively disable the impact of the sink segment, hence significantly reducing the tensile stress at the cathode [Fig. 13(b)]. Note, sink structures behave very differently than reservoir structures. While reservoirs affect both steady-state and transient stress, sink structures only affect the steady-state. This is a critical distinction that should be noted.

Previously in [36], we proposed two methods to trigger the wire to fail. In the first method, an active wire segment is converted to a passive sink, where as in the second method, a passive sink is converted to an active sink. We have revised this approach in this paper, effectively combining the two methods, turning an active wire segment into an active sink directly. This technique allows us to easily control the mortality of the interconnect structure during runtime simply by controlling the direction of current flow in the sink segment.

To take advantage of this behavior, we have to carefully design the structure such that the tensile stress at the cathode saturates above critical stress for acceleration (active sink), and below critical stress for normal use (disabled sink). When steady-state stress is below critical stress, the structure is considered immortal under EM (will never fail). Hence, unlike the reservoir-based method, the sink-based method requires careful tuning of three variables (main-branch length, sink length, and current density) to achieve the desired TTF under normal-use and acceleration modes. The TTF results for various configurations are shown in Table I. Note, all these configurations are carefully designed so that the structure is immortal under normal use; the results presented in the table are from when the structure is operated under acceleration mode.

TABLE I
TTF ACCELERATION WITH VARIOUS SINK AND MAIN-BRANCH CONFIGURATIONS

$L_{MB}(um)$	$L_S(um)$	$J(A/m^2)$	$TTF_{EF}(hr)$	$TTF_{LF}(hr)$
100	60	2.90×10^9	1.15×10^5	2.36×10^5
50	30	4.10×10^9	6.75×10^4	1.1×10^5
30	20	6.80×10^9	2.92×10^4	4.47×10^4
20	15	1.20×10^{10}	1.25×10^4	1.84×10^4
15	10	1.60×10^{10}	8×10^3	1.13×10^4
10	7	3.10×10^{10}	3.42×10^3	4.53×10^3
8	6	3.80×10^{10}	2.62×10^3	3.36×10^3
7	4	5.30×10^{10}	1.79×10^3	2.25×10^3

C. Hybrid EM Acceleration Technique Combining Both Reservoir and Sink Segments

In this section, we leverage the effects of both the reservoir and sink structures to propose a hybrid structure that achieves even better TTF acceleration. The new design, shown in Fig. 14, is a four-segment interconnect structure consisting of two configurable reservoirs, one configurable main-branch, and one configurable sink. We will fix the reservoir length, L_R to be 20 um and only adjust its width, W_R, to achieve the desired TTF. Likewise, the width of the main branch and the sink segment will be fixed at 0.05 um. In order to design the structure for the desired TTF, we will configure the length of the sink, L_S, width of the reservoir, W_R, length of the main branch, L_{MB}, and current density in the main-branch, J_{MB}. The current density in the sink (or disabled sink for normal use) will be set equal to the main-branch, $J_S = J_{\text{MB}}$.

To trigger acceleration mode, the direction of current in the disabled sink segment will be reversed, turning it into an active sink. However, the current density will be kept the same. At the same time, the current flow will be activated in the reservoir segments. Again, the current density in these segments will also be the same as the main branch, $J_R = J_{\text{MB}}$. The direction of current flow during normal use and acceleration mode is illustrated in Fig. 14(a) and (b), respectively.

The simulation results for the proposed structure with varying configurations is shown in Table II. As the results show, this hybrid structure allows us to achieve significant TTF acceleration and meet the lifetime requirement for normal use while keeping the reservoir length at 20 um. This was possible since, unlike the reservoir-based acceleration structure where the additional length of the reservoir was needed to guarantee 10+ years of lifetime during normal use, in this hybrid structure the sink segment is designed to guarantee immortality during normal use. Hence, here the reservoir can be designed solely for enhancing the EM effects during acceleration mode.

TABLE II
TTF ACCELERATION WITH VARIOUS SINK, MAIN SEGMENT, AND RESERVOIR CONFIGURATIONS

L_{MB} (um)	L_S (um)	W_R (um)	J (A/m^2)	TTF_{EF} (hr)	TTF_{LF} (hr)
100	60	0.3	5×10^9	3.44×10^5	3.53×10^5
50	30	0.4	1.25×10^{10}	7.33×10^3	8.67×10^3
30	20	0.5	2×10^{10}	2.1×10^3	2.52×10^3
20	15	0.6	2.75×10^{10}	1.12×10^3	1.29×10^3
15	10	0.7	3.5×10^{10}	694.44	780.56
10	7	0.8	4.25×10^{10}	472.22	513.89
8	6	0.9	5×10^{10}	344.44	372.22
7	4	1	5.75×10^{10}	261.67	277.78

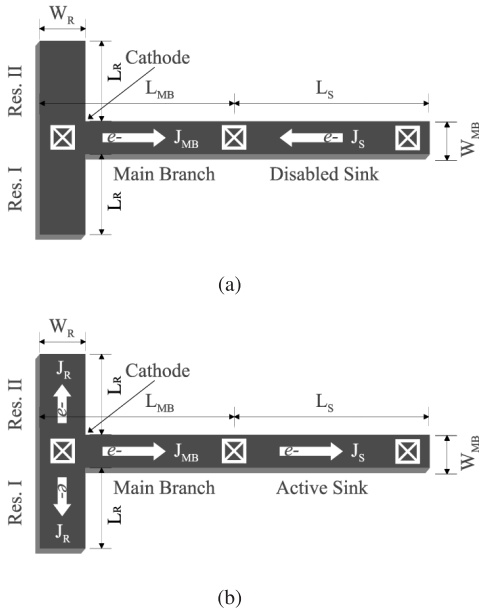


Fig. 14. Proposed hybrid EM acceleration structure with one sink and two reservoir segments under: (a) normal use and (b) acceleration mode.

With this hybrid structure, we were able to achieve a TTF of 10.9 days for the early failure case, and 11.6 days for the late failure case. However, as previously stated, this is achieved at a working temperature of ∼80 °C, with no increase in current density, simply by triggering acceleration mode where current flow is activated in the reservoir segments, and the direction of current is reversed in the sink segment. During testing, the operating temperature will be increased to accelerate EM effects, consequently reducing TTF even further. Our goal in this paper is to leverage the unique properties of the proposed structures so the desired TTF can be achieved with minimal increase in operating temperature. In the next section, we will discuss these testing conditions.

IV. TEMPERATURE-BASED EM FAILURE ACCELERATION

In this section, we study the impact of temperature in accelerating the EM aging process. If the wire is immortal (tensile stress at the cathode saturates below critical stress), then temperature will not have any impact on EM wear-out. However, if the wire is mortal, then increasing temperature will have a significant impact in accelerating TTF under EM. This is due to the fact that EM is fundamentally an atom diffusion process

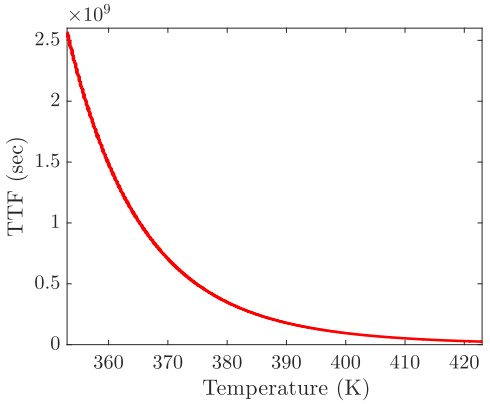


Fig. 15. Impact of temperature on the structure shown in Fig. 10 operating under normal mode.

TABLE III
RESULTS FROM TEMPERATURE-BASED ACCELERATED TECHNIQUE ON THE STRUCTURE SHOWN IN FIG. 10 OPERATING UNDER NORMAL MODE

Temp.(°C)	$TTF_{EF}(hr)$	$TTF_{LF}(hr)$
79.85	7×10^5	7.17×10^5
89.85	3.58×10^5	3.64×10^5
99.85	1.7×10^5	1.73×10^5
109.85	8.08×10^4	8.25×10^4
119.85	4.39×10^4	4.47×10^4
129.85	2.24×10^4	2.29×10^4
139.85	1.29×10^4	1.32×10^4
149.85	7.03×10^3	7.19×10^3

which is activated only if steady-state tensile stress is above 500 MPa (critical stress).

However, as previously mentioned, temperature also accelerates other reliability effects, which is not desirable when the goal is to study EM in isolation. Hence, we will leverage temperature along with the aforementioned reservoir and sink-based methods to achieve significant TTF acceleration while staying below the 150 °C temperature limit.

Before we discuss the impact that increasing temperature has on the proposed structures operating in acceleration mode, we will first show the results for normal use mode. Specifically, we use the multisegment structure shown in Fig. 10, where $L_R = 20$ um and $W_R = 1$ um. This configuration is mortal in its default state and therefore is a good candidate to illustrate the effects of increasing temperature. The simulation results in Fig. 15 shows the impact on TTF as temperature is gradually increased. Few of the data points from this figure is shown in Table III.

As the results show, temperature has an exponential impact on the EM lifetime of mortal interconnect wires. In general, a design rule-of-thumb is 10% increase in temperature will lead to 10× reduction in TTF.

V. NUMERICAL RESULTS AND DISCUSSION

In this section, we present the results from subjecting the proposed structures to the temperature-based testing conditions under acceleration mode. We will show that the proposed methods lead to the targeted $10^5\times$ acceleration in TTF while staying below the 150 °C temperature limit

TABLE IV
TOTAL ACCELERATION RESULTS: COMBINING THE PROPOSED STRUCTURE-BASED EM ACCELERATION METHODS AND TEMPERATURE-BASED STRESSING CONDITIONS

Temp.(°C)	Reservoir-based Structure		Sink-based Structure		Hybrid Structure	
	$TTF_{EF}(hr)$	$TTF_{LF}(hr)$	$TTF_{EF}(hr)$	$TTF_{LF}(hr)$	$TTF_{EF}(hr)$	$TTF_{LF}(hr)$
79.85	1.49×10^3	1.69×10^3	1.98×10^3	2.45×10^3	263.33	271.94
89.85	747.22	836.11	861.11	1.13×10^3	121.94	125.83
99.85	336.11	380.56	438.89	541.67	58.89	60.83
109.85	168.33	189.72	216.94	266.94	29.44	30.28
119.85	92.5	103.33	110.03	136.67	15.17	15.67
129.85	46.39	52.22	57.5	71.67	8.08	8.36
139.85	25.47	28.61	30.83	94.17	4.47	4.61
149.85	15.25	17.11	19.5	23.97	2.56	2.64

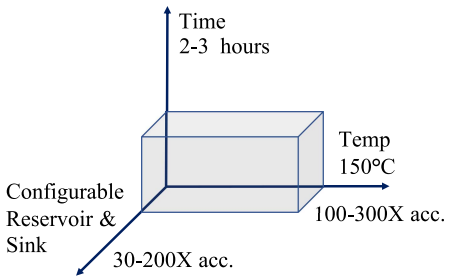


Fig. 16. Leveraging both structure-based and temperature-based acceleration methods.

A. Configurable Reservoir-Based Structure Subjected to Temperature-Based Stressing Conditions

First, we use the reservoir-based structure shown in Fig. 10, where $L_{\text{MB}} = 100$ um, $W_{\text{MB}} = 0.05$ um, $J_{\text{MB}} = 2 \times 10^{10}$ A/m^2, $L_R = 20$ um, and $W_R = 2$ um. Table IV summarizes the acceleration results as temperature is gradually increased from ∼80 °C to ∼150 °C. In this configuration, at ∼150 °C, lifetime is reduced from 10+ years down to about 15.26 h for the early failure case and 17.12 h for the late failure case. This constitutes to an acceleration in the order of $10^4\times$.

B. Configurable Sink-Based Structure Subjected to Temperature-Based Stressing Conditions

Second, we use the sink-based structure shown in Fig. 12, where $L_{\text{MB}} = 7$ um, $L_S = 4$ um, and $J_{\text{MB}} = J_S = 5.3 \times 10^{10}$ A/m^2. The resulting TTF for both EF and LF cases as the temperature is increased from ∼80 °C to ∼150 °C is shown in Table IV. This configuration yields a TTF of 19.5 h for the early failure case and 23.97 h for the late failure case. The acceleration is still in the order of $10^4\times$. Our results show that the reservoir-based method typically achieves slightly better acceleration but at the cost of a higher area-overhead.

C. Hybrid Structure (Reservoir + Sink) Subjected to Temperature-Based Stressing Conditions

Lastly, we repeat the same test on the hybrid structure shown in Fig. 14. By leveraging both the reservoir-based and sink-based acceleration methods together, we can achieve an even more impressive TTF reduction without needing to exceed the 150 °C temperature limit as illustrated in Fig. 16. For the structure shown in Fig. 14, where $W_R = 2$ um, $L_R = 20$ um, $L_{\text{MB}} = 7$ um, $L_S = 4$ um, and $J_{\text{MB}} = J_R = J_S = 5.6 \times 10^{10}$ A/m^2. The TTF results for both EF and LF cases as the temperature is increased from ∼80 °C to ∼150 °C is shown in Table IV.

As the results show, we were able to achieve a TTF reduction from ten years down to 2.56 h for the EF case, and 2.65 h for the LF case. This structure gives us the $10^5\times$ acceleration that we aimed for. This is a significant reduction in EM lifetime achieved at nominal current density and temperature when compared to traditional burn-in testing.

VI. CONCLUSION

In this paper, we studied two structure-based EM acceleration techniques for fast failure testing. We showed that especially designed EM acceleration structures, based on the unique properties of atomic reservoir and sink segments, can be used to drastically alter the TTF of active interconnect wires. The proposed structures can be configured to achieve the desired TTF reduction during acceleration mode, while, at the same time, meet the 10+ year lifetime requirement during normal use. We demonstrated that these structures, when subjected to the traditional temperature-based testing conditions, can achieve a lifetime reduction from 10+ years down to a few hours, while staying below a 150 °C temperature limit. This satisfies the $10^5\times$ reduction in TTF that is typically desired for accelerated testing. The proposed method, for the first time, allows EM testing and validation to be carried out in a controlled manner without the risk of accelerating other reliability effects in the process.

REFERENCES

[1] (2015). *International Technology RoadMap for Semiconductors (ITRS)*. [Online]. Available: http://www.itrs2.net/itrs-reports.html
[2] H. Stork, "Keynote: Electrified driving experience—Expectations on automotive semiconductors," in *Proc. IEEE Int. Integr. Rel. Workshop (IIRW)*, 2017, p. 1.
[3] M. Ohring, *Reliability and Failure of Electronic Materials and Devices*. San Diego, CA, USA: Academic Press, 1998.
[4] D. Wolpert and P. Ampadu, *Temperature Effects in Semiconductors*. New York, NY, USA: Springer, 2012, pp. 15–33. [Online]. Available: https://link.springer.com/chapter/10.1007/978-1-4614-0748-5_2
[5] J. R. Black, "Electromigration—A brief survey and some recent results," *IEEE Trans. Electron Devices*, vol. ED-16, no. 4, pp. 338–347, Apr. 1969.
[6] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *J. Appl. Phys.*, vol. 47, no. 4, pp. 1203–1208, 1976.
[7] M. Hauschildt *et al.*, "Electromigration early failure void nucleation and growth phenomena in Cu and Cu(Mn) interconnects," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2013, pp. 2C.1.1–2C.1.6.

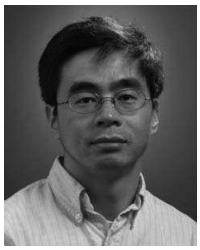
[8] S. X.-D. Tan *et al.*, *VLSI Systems Long-Term Reliability—Modeling, Simulation and Optimization*. Cham, Switzerland: Springer, 2019.
[9] X. Huang, T. Yu, V. Sukharev, and S. X.-D. Tan, "Physics-based electromigration assessment for power grid networks," in *Proc. Design Autom. Conf. (DAC)*, Jun. 2014, pp. 1–6.
[10] V. Sukharev, X. Huang, H. Chen, and S. X.-D. Tan, "IR-drop based electromigration assessment: Parametric failure chip-scale analysis," in *Proc. Int. Conf. Comput-Aided Design (ICCAD)*, Nov. 2014, pp. 428–433.
[11] H.-B. Chen, S. X.-D. Tan, X. Huang, T. Kim, and V. Sukharev, "Analytical modeling and characterization of electromigration effects for multibranch interconnect trees," *IEEE Trans. Comput-Aided Design Integr. Circuits Syst.*, vol. 35, no. 11, pp. 1811–1824, Nov. 2016.
[12] X. Huang, A. Kteyan, S. X.-D. Tan, and V. Sukharev, "Physics-based electromigration models and full-chip assessment for power grid networks," *IEEE Trans. Comput-Aided Design Integr. Circuits Syst.*, vol. 35, no. 11, pp. 1848–1861, Nov. 2016.
[13] V. Mishra and S. S. Sapatnekar, "Predicting electromigration mortality under temperature and product lifetime specifications," in *Proc. 53rd ACM/EDAC/IEEE Design Autom. Conf. (DAC)*, Jun. 2016, pp. 1–6.
[14] Z. Sun *et al.*, "Voltage-based electromigration immortality check for general multi-branch interconnects," in *Proc. Int. Conf. Comput-Aided Design (ICCAD)*, Nov 2016, pp. 1–7.
[15] X. Huang, V. Sukharev, T. Kim, H. Chen, and S. X.-D. Tan, "Electromigration recovery modeling and analysis under time-dependent current and temperature stressing," in *Proc. Asia–South Pac. Design Autom. Conf. (ASPDAC)*, 2016, pp. 244–249.
[16] X. Huang, V. Sukharev, T. Kim, and S. X.-D. Tan, "Dynamic electromigration modeling for transient stress evolution and recovery under time-dependent current and temperature stressing," *VLSI J. Integr.*, vol. 58, pp. 518–527, Jun. 2017.
[17] S. Chatterjee, V. Sukharev, and F. N. Najm, "Power grid electromigration checking using physics-based models," *IEEE Trans. Comput-Aided Design Integr. Circuits Syst.*, vol. 37, no. 7, pp. 1317–1330, Jul. 2018.
[18] S. X.-D. Tan *et al.*, "Recent advances in EM and BTI induced reliability modeling, analysis and optimization," *VLSI J. Integr.*, vol. 60, pp. 132–152, Jan. 2018.
[19] Z. Sun, E. Demircan, M. D. Shroff, C. Cook, and S. X.-D. Tan, "Fast electromigration immortality analysis for multisegment copper interconnect wires," *IEEE Trans. Comput-Aided Design Integr. Circuits Syst.*, vol. 37, no. 12, pp. 3137–3150, Dec. 2018.
[20] H. Zhao and S. X.-D. Tan, "Postvoiding fem analysis for electromigration failure characterization," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 11, pp. 2483–2493, Nov. 2018.
[21] C. Cook, Z. Sun, E. Demircan, M. D. Shroff, and S. X.-D. Tan, "Fast electromigration stress evolution analysis for interconnect trees using Krylov subspace method," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 5, pp. 969–980, May 2018.
[22] R. L. De Orio, H. Ceric, and S. Selberherr, "Physically based models of electromigration: From black's equation to modern TCAD models," *Microelectron. Rel.*, vol. 50, no. 6, pp. 775–789, 2010.
[23] W. K. Meyer, *Electromigration of Damascene Copper for IC Interconnect*. Ph.D. dissertations, Dept. Elect. Comput. Sci., Oregon Health Sci. Univ., Portland, OR, USA, Apr. 2004.
[24] V. Sukharev, A. Kteyan, and E. Zschech, "Physics-based models for EM and SM simulation in three-dimensional IC structures," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 2, pp. 272–284, Jun. 2012.
[25] V. Sukharev, A. Kteyan, and X. Huang, "Postvoiding stress evolution in confined metal lines," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 1, pp. 50–60, Mar. 2016.
[26] H.-B. Chen, S. X.-D. Tan, J. Peng, T. Kim, and J. Chen, "Analytical modeling of electromigration failure for VLSI interconnect tree considering temperature and segment length effects," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 4, pp. 653–666, Dec. 2017.
[27] M. A. Korhonen, P. Borgesen, K. N. Tu, and C.-Y. Li, "Stress evolution due to electromigration in confined metal lines," *J. Appl. Phys.*, vol. 73, no. 8, pp. 3790–3799, 1993.
[28] S. Wang, Z. Sun, Y. Cheng, S. X.-D. Tan, and M. B. Tahoori, "Leveraging recovery effect to reduce electromigration degradation in power/ground TSV," in *Proc. Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2017, pp. 811–818.
[29] J. R. Lloyd, "New models for interconnect failure in advanced IC technology," in *Proc. 15th Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA)*, 2008, pp. 1–7.
[30] C.-K. Hu *et al.*, "Effects of overlayers on electromigration reliability improvement for Cu/low K interconnects," in *Proc. 42nd Annu. IEEE Int. Rel. Phys. Symp.*, 2004, pp. 222–228.
[31] L. Zhang, *Effects of Scaling and Grain Structure on Electromigration Reliability of Cu Interconnects*, Ph.D. dissertations, Elect. Comput. Eng., Univ. Texas at Austin, Austin, TX, USA, 2010.
[32] Z. Sun, S. Sadiqbatcha, H. Zhao, and S. X.-D. Tan, "Accelerating electromigration aging for fast failure detection for nanometer ICs," in *Proc. Asia–South Pac. Design Autom. Conf. (ASPDAC)*, 2018, pp. 623–630.
[33] M. Lin and A. S. Oates, "An electromigration failure distribution model for short-length conductors incorporating passive sinks/reservoirs," *IEEE Trans. Device Mater. Rel.*, vol. 13, no. 1, pp. 322–326, Mar. 2013.
[34] M.-H. Lin and A. S. Oates, "Electromigration failure time model of general circuit-like interconnects," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 2, pp. 381–398, Jun. 2017.
[35] *Synopsys University Program and Resources*, Synopsys, Mountain View, CA, USA. [Online]. Available: https://www.synopsys.com/community/university-program/teaching-resources.html
[36] S. Sadiqbatcha, C. Cook, Z. Sun, and S. X.-D. Tan, "Accelerating electromigration wear-out effects based on configurable sink-structured wires," in *Proc. IEEE Synth. Model. Anal. Simulat. Methods Appl. Circuit Design (SMACD)*, 2018, pp. 21–24.

Sheriff Sadiqbatcha (S'14) received the B.S. degree in electrical engineering from California State University at Bakersfield, Bakersfield, CA, USA, in 2017. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA, USA.

His current research interests include very-large scale integration (VLSI) reliability and exploring applications of machine learning in the area of EDA and physical design, including thermal modeling and analysis of VLSI systems.

Zeyu Sun (S'16) received the B.S. degree in electronic and computer engineering from the Hong Kong University of Science and Technology, Hong Kong, in 2015. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA, USA.

His current research interests include electromigration modeling and assessment and reliability-aware performance optimization.



Sheldon X.-D. Tan (S'96–M'99–SM'06) received the B.S. and M.S. degrees in electrical engineering from Fudan University, Shanghai, China, in 1992 and 1995, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Iowa, Iowa City, IA, USA, in 1999.

He is a Professor with the Department of Electrical Engineering, University of California at Riverside, Riverside, CA, USA, where he is also a Cooperative Faculty Member with the Department of Computer Science and Engineering. He was a Visiting Professor with Kyoto University, Kyoto, Japan, and a JSPS Fellow from 2017 to 2018. His current research interests include very large-scale integration reliability modeling, optimization and management at circuit and system levels, hardware security, thermal modeling, optimization and dynamic thermal management for many-core processors, parallel computing, and adiabatic and Ising computing based on GPU and multicore systems. He has published over 290 technical papers and has coauthored 6 books in the above areas.

Dr. Tan was a recipient of the NSF CAREER Award in 2004, the three Best Paper Awards from ICSICT'18, ASICON'17, ICCD'07, and DAC'09, and the Honorable Mention Best Paper Award from SMACD'18. He is serving as the TPC Vice Chair for ASPDAC'19. He is serving or served as the Editor-in-Chief for *Integration, the VLSI Journal* (Elsevier), the Associate Editor for three journals: the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI), *ACM Transactions on Design Automation of Electronic Systems* (TODAE), and *Microelectronics Reliability* (Elsevier).