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Full-chip wire-oriented back-end-of-line TDDB hotspot detection and lifetime analysis☆

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ABSTRACT

Time-dependent dielectric breakdown (TDDB) has become an important cause of failure for inter-metal dielectrics (IMD) in integrated circuits as feature sizes continue to shrink and novel materials are introduced. Although many studies have been conducted to understand the underlying physics of this issue, not enough work has been focused on evaluating TDDB lifetime of practical chip designs in the physical design stage. This paper proposes a full-chip TDDB failure analysis methodology to evaluate lifetime and identify TDDB hotspots in VLSI layouts, which are essentially interconnect wires that have high failure risk due to TDDB. The proposed method features three new techniques compared to existing methods. First, we have developed a partitioning-based scheme to deal with scaling of full-chip analysis by partitioning the full chip layout into small tiles. Second, for each tile, the new method calculates a newly-introduced TDDB failure metric called *TDDB Damage* for vulnerable wires. Such a wire-oriented TDDB analysis is the first of its kind and is very amenable for physical design as the wires can be easily adjusted or re-routed for TDDB-aware optimization. Third, the new method considers the impact of the non-uniform electric field calculated using the finite element method (FEM), which significantly improves the accuracy of TDDB risk evaluation. Experimental results show that the proposed new TDDB analysis method is more accurate than a recently proposed full-chip TDDB analysis method in which electrical field is treated as a constant value. Additionally, the proposed method can analyze a practical VLSI layout in a few hours.

1. Introduction

As VLSI technology manufacturing nodes continue to evolve, geometries for both transistors and interconnect wires are being scaled down. For example, interconnect spacing can be smaller than 20 nm for 10 nm and 7 nm nodes. At the same time, more fragile materials are being used for the interconnect dielectric as they provide the benefit of a lower permittivity (referred to as low-*k*), which contributes to lowering the interconnect delay by reducing parasitic capacitance. Furthermore, manufacturing steps such as chemical-mechanical planarization (CMP) and plasma etch may damage the dielectric by causing sub-surface carrier traps that assist conduction, increasing the possibility of unwanted leakage and even failure. These are key factors that impact back-end-of-line (BEOL) Time-Dependent Dielectric Breakdown (TDDB), also called inter-metal dielectric (IMD) TDDB, an increasingly serious interconnect reliability challenge. BEOL TDDB occurs when the inter-metal dielectric breaks down after prolonged stress of an electric field. The failure is usually observed as an abrupt increase in leakage current [1].

Traditionally, TDDB has primarily been a concern for gate dielectrics of CMOS devices. With the advances of technology scaling, middle-of-line (MOL) TDDB and BEOL TDDB have also become important reliability mechanisms. MOL TDDB is breakdown between the gate and contact [2,6]. On the other hand, BEOL TDDB is breakdown between the interconnect wires, including both metal lines and vias. Significant research has also been done to understand the physics of BEOL TDDB [7]. Simple interconnect leakage test structures such as serpentine-comb or comb-comb have been typically used in these studies. In contrast, very little work has been done to develop a framework for assessing BEOL TDDB

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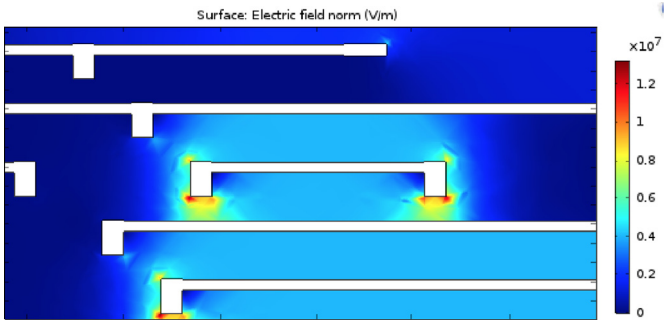

Fig. 1. FEM result showing higher electric field around tips.

risk in practical and actual circuit layout geometries, which this work focuses on.

Analysis results through FEM of electric field in a small piece of a synthesized layout shown in Fig. 1 reveals that with a voltage difference between neighboring wires, the electric field at 'corners' or 'tips' of wires can actually differ greatly from that along longer, straight-line segments, leading to the so called 'layout effects' [8]. The higher electric field at tips can substantially reduce the lifetime of such wires, making the results scaled from test data optimistic and inaccurate. Thus, more applicable methods considering such layout effects are required if experimental data is to be used in practical lifetime analysis.

To mitigate these problems, we propose a full-chip TDDB failure analysis method to identify the TDDB hotspots in the layout, which are essentially wires that have high failure risk due to TDDB. Based on solving electric field with the help of FEM, the proposed method can cover the layout effect and get more accurate results. Our novel contributions lie in the following new techniques compared to existing methods:

1. A partitioning-based scheme is developed to deal with the scalability for full-chip analysis. The layout of the entire chip is partitioned into smaller tiles to enable the use of FEM.
2. In each tile, the new method calculates a newly-introduced TDDB failure metric called *TDDB Damage* for the vulnerable wires. Such a wire-oriented TDDB analysis is the first of its kind and is very amenable for physical design as wires identified to be at risk for TDDB can be easily adjusted and re-routed for TDDB optimization.
3. The new method is applicable to all existing electric field-dependent TDDB models and can significantly improve accuracy as it is based on solving for electric field by FEM.

Because this method is based on solving electric field, unlike [3], it can consider the non-uniform electrical field and cover local field enhancement effects, which leads to more accurate TDDB lifetime estimation. Additionally, the proposed methods can be applied to all the existing electric field-dependent TDDB models such as E, 1/E, power-law, and $\sqrt{E}$ models. Numerical results show that our proposed method can identify the TDDB hotspots for a practical VLSI layout in a reasonable amount of time. Our study further shows that M1 (Metal1) typically has the shortest lifetime because of the highest metal density.

This paper is organized as follows: Section 2 briefly compares this work to related works, and Section 3 gives a review of various electric field-dependent TDDB models and introduces the equations we use to evaluate TDDB. Section 4 introduces our analysis flow in three steps. Some experimental results and insights are provided in Section 5. Finally, we conclude this paper in the last section.

2. Related work

There are three recent publications focusing on full-chip BEOL TDDB assessment. A chip-scale TDDB lifetime simulator is proposed in Ref. [3]. In this work, interconnect geometries are grouped by spacing between wires and the total run length of each group is extracted. Next, lifetime of each group is scaled by total length based on experimental data of dielectrics of the same spacing. Furthermore, practical considerations such as variation in spacing and different temperature across the chip are also done. Using data from tests with same line space makes the evaluation process straightforward, which however also means that the layout effect is not considered, making the results scaled from test data optimistic and inaccurate. Thus, it is not sufficient to evaluate lifetime purely by extracting spacings and scaling from test data assuming a uniform electrical field. Another limitation of [3] is that all horizontal wire segments and vertical ones are considered separately. In reality, one particular interconnect wire can have horizontal and vertical parts at the same time. Hence, they should not be analyzed separately.

The same problem of layout effect also applies to Ref. [9]. This paper is based on different TDDB equations, so accuracy is compromised when the assessment is simplified to focus on spacing between wires alone.

The simulator introduced by Ref. [4] is built on a look-up table of high-risk interconnect shape patterns. Although local field enhancement is considered in preparation of the look-up table, the effect of length scaling of wires is not covered.

3. New length-aware TDDB model

In this section, we first briefly review several TDDB models, especially the $\sqrt{E}$ model that is used in this work, then we derive the equations that we use to evaluate TDDB lifetime and failure rate based on the $\sqrt{E}$ model. Note that although $\sqrt{E}$ model is used throughout this study, any other electric field dependent model can be used in the same way with the proposed analysis flow.

3.1. Review of $\sqrt{E}$ and other TDDB models

Various models have been proposed based on different assumptions of the physics of BEOL TDDB. Some commonly discussed models are $\sqrt{E}$, power-law, E, $1/E$, and impact damage model [9]. All of them can fit the measured data obtained at high-E field stressing conditions well. However, they differ substantially when extrapolated to the practical low-E use conditions. As some further experimental results have shown [10], $\sqrt{E}$ model performs relatively better in fitting measured results under both high-E field and low-E field stressing conditions in conventional dielectrics. Thus, $\sqrt{E}$ model is used in this work. However, the specific choice of model does not limit the applicability of our approach, as all models are based on the electric field, and electric field is solved in our analysis flow.

The $\sqrt{E}$ model indicates that TDDB lifetime can be described in the following general form [11,12]:

$$TTF = K \exp(-\gamma \sqrt{E}) \exp(\frac{E_a}{kT}) \quad (1)$$

where TTF is the time to failure or lifetime, K is a fitting constant, γ is the electric field acceleration factor, E represents the electric field, E_a is the Arrhenius activation energy, k is the Boltzmann constant, and T is the absolute temperature. The $\sqrt{E}$ dependence comes from the assumption that Poole-Frenkel [13] or Schottky Emission injection [12] plays the primary role in electron conduction, and they both have a $\sqrt{E}$ dependence.

3.2. TDDB damage model of interconnect wires

In studies validating the $\sqrt{E}$ model [1], coefficients in (1) were fitted based on measurements carried out on a large set of identical interconnect test structures and geometries, under different stressing conditions.

However, for practical VLSI layouts, the study shows that the TDDB failure is also wire length-dependent [3]. Besides length, there exist significant differences in the shape of interconnect wires in VLSI layouts,

and thus the wire length and shape should be accounted for when the equation is used to estimate TDDB lifetime of wires in practical VLSI layouts. In Ref. [5], the reciprocal of the Weibull shape factor β is used as the area scaling factor for gate oxides. Thus, time to failure is proportional to $A^{-\frac{1}{\beta}}$ for the same stressing conditions, where A is the area of the dielectric. Based on this observation, in our model we propose using β as the *length* scaling factor for interconnect wires. This scaling approach has also been used in other BEOL TDDB lifetime analysis publications [3]. We note here that scaling is applied to perimeter length instead of area because it is safe to assume that the interconnect thickness is relatively constant, and thus the area scaling term reduces to a length scaling term with an appropriate adjustment to the fitting constant. As a result, in this work, we propose the following TDDB lifetime formula considering the length effect or scaling, which is shown below [5]:

$$TTF = K' \exp(-\gamma\sqrt{E}) \exp(\frac{E_a}{kT}) L^{-\frac{1}{\beta}} \tag{2}$$

where K' is a new fitting constant.

We further define a new metric called *TDDB Damage* (D) of wires on top of (2) by multiplying the reciprocal of *TTF*, which is used as a reference of what ratio we are at towards *TTF*. We define it as an accumulative factor with a derivative:

$$dD = \frac{dt}{TTF} = \frac{1}{K'} \exp(\gamma\sqrt{E}) \exp(\frac{-E_a}{kT}) L^{\frac{1}{\beta}} dt \tag{3}$$

It is obvious that by comparing (2) and (3), the maximum TDDB damage D an interconnect wire accumulates before failure is $D_{\max} = D(t = TTF) = 1$ under this definition.

Note that E is usually non-uniform along the perimeter of interconnect wires due to layout effects and IR drops, and E can even be time-variant. Furthermore, the same applies to T as well. So the layout-dependent TDDB damage for an interconnect wire in such complicated cases should be calculated through an integral on the perimeter (L) of the wire over time:

$$D_{wire} = \frac{1}{K'} L^{\frac{1}{\beta}-1} \int_0^t \oint_L \exp(\gamma\sqrt{E(l,t)}) \exp(\frac{-E_a}{kT(l,t)}) dl dt \tag{4}$$

In order to locate TDDB hotspots, which are interconnect wires with high failure risk, it is sufficient to assess the TDDB damage accumulated over a set of all interconnect wires. To simplify the problem further, we assume static E as the more complicated time-variant E-induced failure can be mapped to static E through measurements as done in Refs. [3,4].

Similarly, we consider steady-state or worst-case temperature as TDDB is a long-term failure effect. We also assume uniform temperature across the layout for simpler calculation. For non-uniform temperature, we will introduce a partitioning-based approach to mitigate this assumption later, in which constant temperature is assumed in one partition. As a result, we can remove the constant terms in (4) for a simplified metric *Damage rate* (R):

$$R = L^{\frac{1}{\beta}-1} \oint_L \exp(\gamma\sqrt{E(l)}) \exp(\frac{-E_a}{kT(l)}) dl \tag{5}$$

To further simplify, if we assume uniform temperature in a region (or partition), R can be reduced to:

$$R = L^{\frac{1}{\beta}-1} \oint_L \exp(\gamma\sqrt{E(l)}) dl \tag{6}$$

The most vulnerable wires would therefore be identified by calculating and comparing this metric for each wire.

3.3. Chip lifetime

As lifetime of each wire has a Weibull distribution with shape parameter β. The survival rate S (chance of not failing) and lifetime *TTF* of a wire are [14]:

$$S(t)_{wire} = \exp[-(t/\gamma)^{\beta}]$$

$$TTF_{wire} = \gamma \cdot \Gamma(\frac{1}{\beta} + 1)$$

Given the lifetimes of individual interconnect wires, the lifetime of the full chip can be derived by multiplying the reliability of each wire based on the assumption that failure of any single wire results in a short circuit and thus failure of the entire chip. Therefore, the reliability of the chip is:

$$S(t)_{chip} = \prod_i S(t)_{wire\_i} = \exp[-\sum_i (\frac{t}{\gamma_i})^{\beta}]$$

By comparing the relationship between S and *TTF*, lifetime of the chip in terms of BEOL TDDB is derived [3]:

$$TTF_{chip} = (\sum_n \frac{1}{TTF_n^{\beta}})^{-\frac{1}{\beta}} \tag{7}$$

Note that the assumption that one failed wire fails the chip is made for simplicity. If redundancy is used in design, the calculation of S can be adjusted accordingly to incorporate the redundancy.

4. Layout partition-based TDDB wire damage analysis

This section introduces in detail our approach to solving electric field across the layout, calculating the TDDB damage accumulation rate of interconnect wires, and locating the TDDB hotspots. An overview of the three key steps of the analysis flow is given in the flowchart in Fig. 2.

Basically, our new full-chip TDDB analysis flow first partitions the layout into many smaller tiles and records which tile each interconnect wire belongs to. After this, FEM problems for each tile are set up with the appropriate boundary conditions and solved for the electrical field distributions. Then, the TDDB damage accumulation rate described by (6) can be calculated. Finally we find the wires with maximum TDDB damage accumulation rate and mark them as the *hotspot* wires. Furthermore, lifetime of the chip can be calculated using (7).

In the following paragraphs, additional details of each step are given.

4.1. Layout partition

As (6) shows, electric field is required across the full layout in order to evaluate the damage accumulation rate for each interconnect wire. As discussed previously, 3D geometries are simplified to 2D for this work, and thus different layers are analyzed separately. However, it is still too computationally expensive to conduct FEM analysis of a full interconnect layer. Therefore, it is impractical to solve electric field over an entire interconnect metal layer in one FEM problem. One important

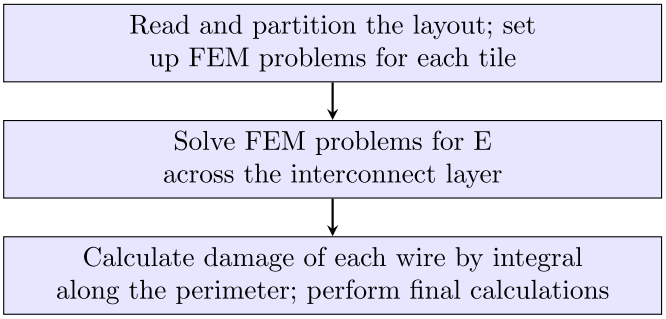

Fig. 2. The three key steps of the analysis flow.

point that is helpful for simplifying the problem is that in each metal layer, most interconnect wires are mainly routed in the same direction. For example it is horizontal for Metal3 (M3), and vertical for Metal4 (M4). As a result, the voltage applied on one wire is unlikely to contribute to the electric field several channels away as there will be a high likelihood of other interconnect wires in between, 'blocking' the electric field lines. This makes it reasonable to partition a big layout into smaller tiles, solve FEM problems in these tiles of much smaller size, and combine the results at the end. Fig. 3 is an example showing this idea. All the blue lines are interconnect wires of Metal3 in the layout. Details about this layout will be further discussed in Section 5. The dashed yellow lines in the figure show the partition of the layout into much smaller tiles. Electric field in each tile would be solved as if there is no other wire outside the tile.

Through experimentation (explained further in Section 5), we find that the electric field solved in the center area of the tile is accurate. This is reasonable as all surrounding wires which influence the electric field at the point of interest are included in the tile and thus the results are expected to be correct. However, in some cases, electric field around the boundaries of the tile is inaccurate as the adjacent wires in neighboring tiles are not included in the tile. We propose to solve this issue by enlarging the tiles. This idea is also shown in Fig. 3, where the yellow solid rectangle at the lower left corner represents the first tile after enlargement. Basically, the area analyzed for each tile is enlarged and the original tile is now the region where results are deemed as valid (the 'effective area'). The tile perimeter expansion ratio can be small since only close-range adjacent wires are required to be included in the extended area. Wires that are farther than, for example, 10 times the feature size or pitch can be safely ignored as they are unlikely to contribute to the electric field inside the tile. In comparison, the size of the effective area would be much larger than that of the feature size. Thus, enlarging the tiles is not expected to significantly affect the analysis runtime.

A library called python-gdsii [15] is used to collect geometry information of all wires on each layer. Once the size of each tile is defined, geometry of wires in each tile is extracted for the next step. At the same time, we are able to record which tile each wire is located in to assist step 3. One challenge is that the wires are broken into segments in the gdsii file, and there is no information indicating which segments each wire should be composed of. In other words, wires in complicated shapes need to be built back by locating and concatenating segments in simpler shapes such as rectangles. To accomplish this, an algorithm determining segments overlaps and union find [16] are used. Note that LVS (Layout versus Schematic) could also be used to analyze the connectivity for all wire segments initially, thus saving the time for running the union find algorithm.

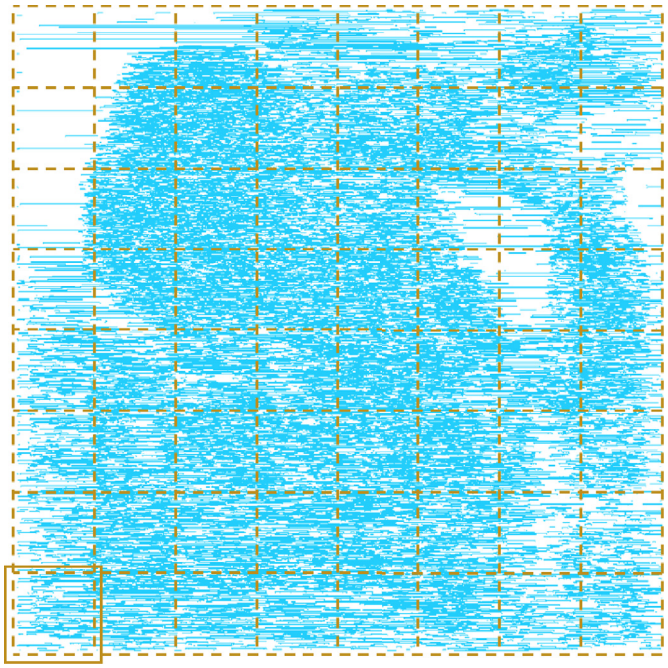

Fig. 3. Full layout of Metal3 and the partition scheme. Dashed lines show tiles after partition and solid line shows enlargement of the first tile.

4.2. Solving E and TDDB damage in each tile

In this step, we need both geometry information for the wires inside each tile and the voltages on each wire to set up the FEM problem. The geometry information is available after the first step. The voltages are set arbitrarily in order to simulate the worst case: all wires in horizontally-routed layers are sorted by their y-coordinates, while those in vertically routed layers are sorted by their x-coordinates. The wires are then alternately set to *VDD* and *GND*. Although the electric field computed in this manner would be higher than would be expected in real applications, this approach is sufficient to identify vulnerable wires. Essentially, a wire is vulnerable to TDDB failure due to sustained high electric fields produced by higher voltage, higher temperature, narrower space, longer length, or over time. Hence, the worst-case electric field can be used to find the wires at risk. We note that if this evaluation flow can be implemented in standard sign-off flow, where signal pattern for each network is available, more realistic boundary conditions of voltage can be applied, resulting in more trustworthy results and a more accurate determination of time to failure. In Ref. [4], similar work has been done and it shows that the worst case time to failure is about half of the realistic one for wire pairs with 50% duty cycle. Thus, if given more voltage information, simply adding a coefficient like 2 to lifetimes of wires of different groups can result in a more accurate estimate of time to failure.

In this work, all wire segments are treated as straight lines, so the line roughness effect (or equivalently, the variation of spacing) has been ignored. We note that this problem can be solved by adding a coefficient to the final result of time to failure as is done in Ref. [17].

COMSOL [18] is used to set up and solve the FEM problems. TDDB damage accumulation rate of each wire as described in (6) is calculated through an integral in COMSOL. At the same time, the length of each wire in the tiles is also recorded for the next step. Thus, the results obtained in this step for each tile are the damage accumulation rate R and length L of each wire in the tile.

Note that all these calculations are done within the scope of one tile, so calculations in different tiles can be carried out in parallel.

4.3. Integral of long wires for final results

As indicated previously, there may exist long wires that span more than one tile. In the previous step, the length and damage accumulation rate for these wires are available separately for each tile that they span. Another step of merging the integral results from different tiles is needed to get the final R values. Then the damage accumulation rates for all wires are available and thus, we can identify the most vulnerable ones. In Fig. 4, an example is given to show how long wires are dealt with in the simple case where there are only two tiles and three wires. Wire 1 lies completely within the left tile and wire 2 lies completely within the right tile. Wire 3 lies across both tiles. Note that the temperature is different in the two tiles so (5) shall be used to calculate R. Solving electric field distribution and calculating integral of damage accumulation rate R gives results of R_1, R_{31} in the left tile, and R_2, R_{32} in the right tile. R_1, R_2 are final results of the corresponding wire as

they lie in only one tile. However, there is an additional step needed to get R_3:

$$R_3 = \left(\frac{R_{31}}{L_1^{\frac{1}{\beta}-1}} + \frac{R_{32}}{L_2^{\frac{1}{\beta}-1}}\right) * (L_1 + L_2)^{\frac{1}{\beta}-1} \quad (8)$$

in which L_1, L_2 denotes the length of the part of wire 3 in each tile respectively, with $L_1 + L_2$ being the total length.

We want to remark that if there are errors due to electrical field accuracy, E, as we show later in Table 1, this error is not accumulative across partitions. The reason is that in (8), the damage rates computed from each partition R_x are added to together to compute the final damage rate. As a result, if each partition has 2% error (larger or smaller), then the total error in damage rate will be smaller than 2% as errors will not be amplified along different partitions.

To conclude, Algorithm 1 lists the details of the three steps discussed.

Algorithm 1 Full analysis flow.

Data: Layout file
Step 1 (Section 4.1):
Input: Size of tile, enlargement ratio
foreach *Tile* **do**
  Find wire segments in tile
  Merge segments back to wire
  Record long wires
  Set voltage on wires
end
Step 2 (Section 4.2):
forall *Tiles* **do**
  Initialize FEM problem
  Solve FEM problem for E
  Compute R and length of each wire with (6)
end
Step 3 (Section 4.3):
forall *Long wires* **do**
  Merge R from different tiles with (8)
end
Compare R of all wires for hotspot wire
Compute chip lifetime with (7)

5. Numerical results

We conducted three sets of simulations to validate the proposed analysis flow: the first analyzing a comb structure and a twisted line structure with (6) to show the layout effect, the second validating the accuracy of electric field and damage of wires calculated with the layout partition-based approach, and the last demonstrating the analysis flow on an example layout.

We synthesized a CPU test chip for the latter two sets of simulations using a 32 nm educational technology. The size of the layout is 193 μm by 193 μm. Further information about the layout is provided in the second part of the simulation in Table 3.

For numerical analysis, the electric field acceleration factor γ used in the equation is 20 if the unit of E is MV/cm, which is fitted based on published experimental data [11]. The Weibull shape factor β is 0.6, which is obtained from 30 nm half-pitch test vehicles [11]. Temperature is assumed to be constant. The additional constant $K' \exp(\frac{E_a}{kT})$ in (4) is required when evaluating lifetime. The value $1s/cm^{\frac{1}{0.6}}$ is used,

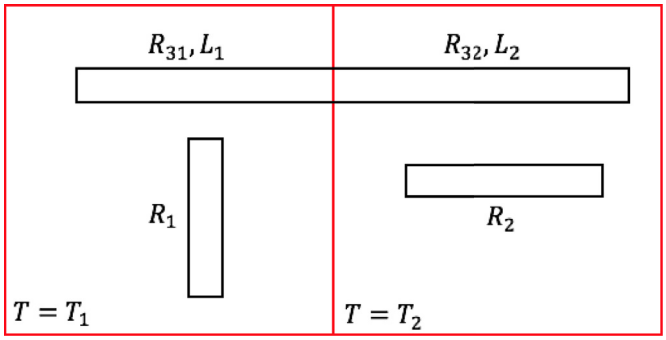

Fig. 4. An example of a wire crossing a tile boundary, with two tiles and three wires in total.

Table 1
Results of E at points marked "×" under different setups. Unit is V/m. Error is defined as $(E - E0)/E0$.

Point	$E0$	Error1(%)	Error2(%)
1	4.032E6	0.00%	0.00%
2	1.671E6	−0.24%	−0.33%
3	4.006E4	47.62%	−6.11%
4	3.261E6	0.30%	0.40%
5	3.815E6	5.70%	−0.03%
6	6.471E3	278.37%	−2.51%

which is an assumed number for the purpose of demonstrating the lifetime calculation.

5.1. Comparison on three structures

In this subsection, we compare our proposed method against two recently published full-chip TDDB methods on two wire structures and show that the electric field calculation is necessary for lifetime predic-

Table 2
Results of R of marked wires marked "∘" under different problem setups. Error is defined as $(R - R0)/R0$.

Wire	$R0$	Error1(%)	Error2(%)
A	1.552E-10	−0.24%	−0.11%
B	7.574E-11	0.33%	−0.05%
C	5.599E-11	−0.06%	−0.14%
D	4.538E-11	−63.06%	0.88%
E	1.038E-12	−39.60%	0.00%
F	1.973E-13	−37.72%	0.80%
G	1.198E-13	0.09%	−8.43%
H	2.679E-13	6.50%	−2.87%
I	3.931E-12	1.26%	1.51%

Table 3
Analysis results of all layers.

Layer	Number of wires	Max R	Lifetime (yr)	Runtime (h)
M1	53756	3.73E-7	118	11.8
M2	26576	3.47E-8	376	7.17
M3	15977	1.64E-8	1570	4.75
M4	5093	2.65E-8	4110	1.32
M5	2225	1.07E-8	1.49E4	0.87
M6	929	8.73E-9	1.08E5	0.38
M7	480	6.96E-9	1.32E5	0.30
M8	173	2.37E-9	3.42E6	0.12
M9	77	2.28E-9	1.85E6	0.10

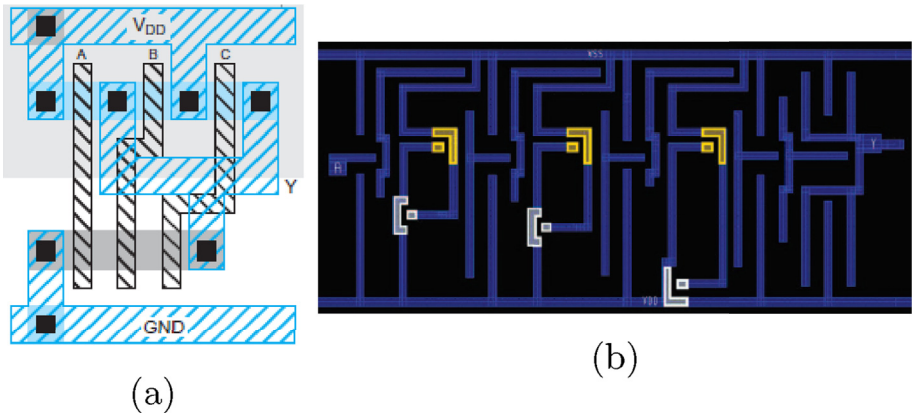

Fig. 5. Comb structures in designs. (a) A NAND gate, courtesy of [20]. (b) A delay cell, courtesy of [4].

tion. The simulated target is three different layout structures: a comb structure, a parallel line structure, and a twisted line structure. Comb structures usually appear in lower levels of interconnects for the purpose of saving area of logic gates. Two examples are shown in Fig. 5. Multiple comb structures exist between the VDD power rail and signal nets. The parallel line structure and twisted line structure usually appear at higher metal levels, as the router typically routes interconnect wires in one primary direction for each layer. Fig. 8, from our synthesized layout, contains many examples of parallel lines and a few twisted line structures. As shown in Fig. 6, the line widths and space between wires are both 60 nm, and the total dielectric channel length is 1000 nm for both (excluding the corner part in (a) and (c), consistent with the method in Ref. [3]). Specifically, the first two structures are simplified from the two commonly-used structures in studies of TDDB physics, namely serpentine-comb and comb-comb structures [19].

In Ref. [3], the time to failure (TTF) of a vulnerable wire with length L_v is scaled from the measured test wire structure under same stressing conditions with wire length L_t as follows:

$$TTF_v = TTF_t(\frac{L_t}{L_v})^{1/\beta} \tag{9}$$

where L_v is the only input of this method, which is 1000 nm for all three examples (shaded area), so the three structure will have the same lifetime as the wire length are same.

The method introduced by Ref. [4] can identify vulnerable spots, which does lead to the correct result that comb structure and twisted line structure fail faster than the parallel line structure. However, length effect is not considered in this method. If the length of stressed dielectric doubles, this method will still give the same result for *TTF*.

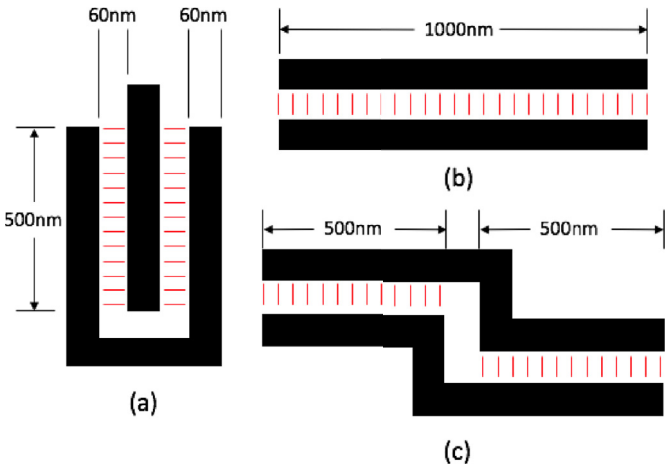

Fig. 6. Three structures analyzed: (a) comb (b) parallel line (c)twisted line.

Our proposed method takes both layout effect and length effect into consideration. In our method, we calculated the electric field in the three structures (shown in Fig. 7), R of three wires using (6), and obtained the lifetime, with the help of COMSOL. It turns out that the lifetimes of the comb structure and twisted line structure are only 0.89× and 0.7× that of the parallel line structure respectively. Furthermore, studies [8,19] show that comb structures are indeed more vulnerable to TDDB failures due to the increased electric field at the tips. Therefore, the proposed method is more accurate than the full chip TDDB method proposed in Ref. [3] and it is indeed necessary to base the analysis on electric field distributions for improved accuracy.

5.2. Validation of the partition-based method

As discussed in Section 4.1, partitioning the layout might lead to some inaccuracy around boundaries as information in neighboring tiles is missing. To reduce loss of accuracy in the electric field analysis, it is proposed to enlarge the tile. The second set of simulations is conducted to verify the effectiveness of this approach.

The simulations are conducted on an extracted small tile from our synthesized layout, as shown in Fig. 8. Wires in M3 layer of this region are represented by lines in the figure. The size of the entire tile is 1.6 μm by 1.6 μm. The green square is the enlarged tile to be analyzed, with an edge length of 1.2 μm, and the red square is the effective area of the tile, with an edge length of 1 μm.

Three simulations with different setups are done. All results are collected within the red square in the figure, which is the effective tile. At first, electric field is solved across the entire extracted tile (the complete Fig. 8) and damage accumulation rate of wires is calculated within the scope of the red square. We denote the electric field and damage accumulation rate results obtained in this phase by $E0$ and $R0$ respectively. These are the reference results that we compare results from the other two simulations. Secondly, with the same voltage settings on the wires, we reduce the scope of the FEM problem to the red square. Results from this step are compared with $E0$ or $R0$ and errors are calculated and denoted by $Error1$. As there is no enlargement of the tile being analyzed, the results in this step are expected to show significant discrepancies. Finally, a third analysis is done with FEM problem set to the green square, enlarging the red tile. Similarly, errors of results in comparison with $E0$ or $R0$ are calculated and denoted by $Error2$.

To compare the results precisely, six locations are chosen to evaluate the electric field. They have been marked by red "×" symbols with indices in Fig. 8 along the wires of interest. Points 1 and 2 are in the center of the tile, while points 3 through 6 are near the boundary of the effective tile area. They are chosen arbitrarily in order to cover as many variations as possible. Table 1 lists E, $Error1$ and $Error2$ at these

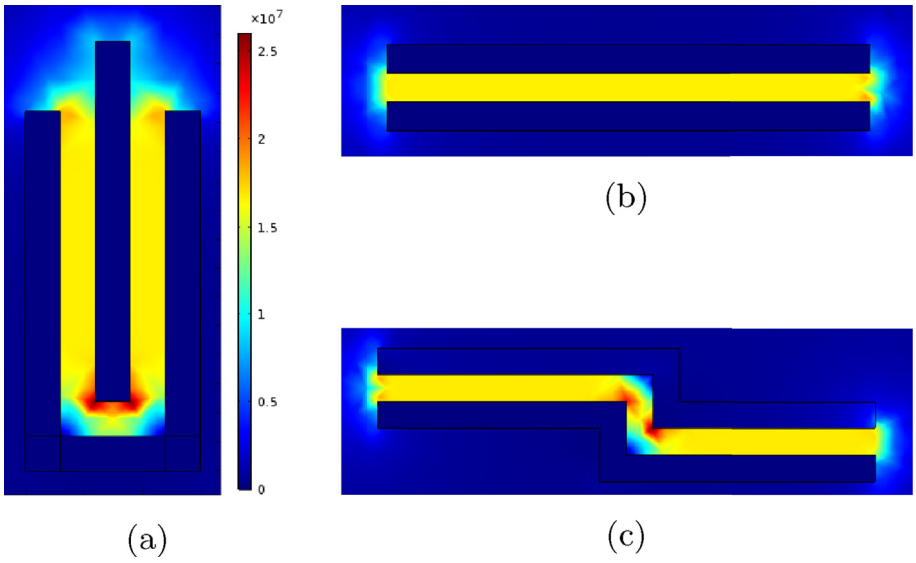

Fig. 7. Electric field distribution of the three structures analyzed.

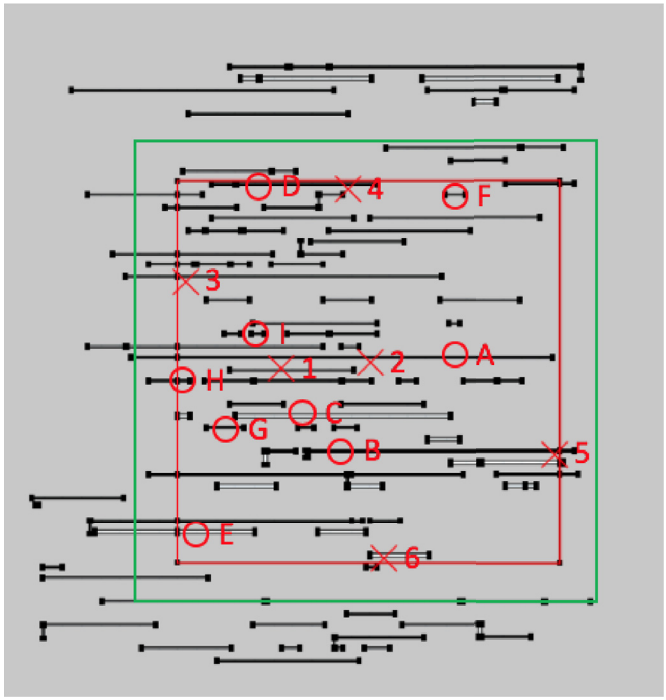

Fig. 8. The layout tile used to validate the partition-based approach.

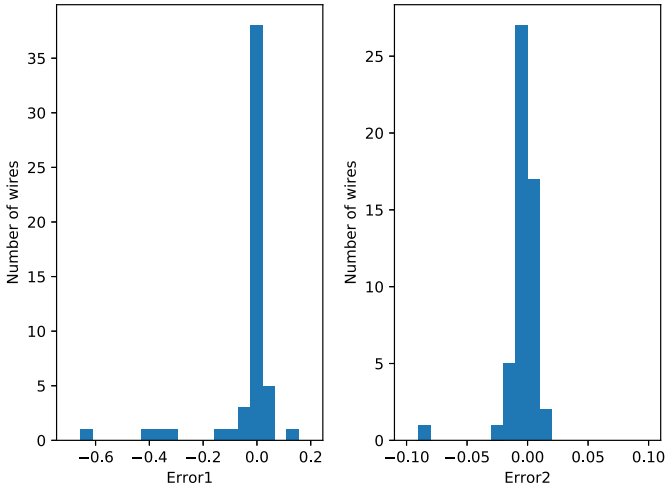

Fig. 9. Distribution of *Error*1 and *Error*2 of *R* among all wires.

points. As can be seen from the table, only points 3 and 6 show significant errors. However, the electric fields at these two points are much lower than the other four points. According to (6), the damage accumulation rate of a wire is mainly determined by high *E* locations along its perimeter. Therefore, the errors at low *E* points are not expected to influence the final results of the damage accumulation rate. The reason for the large *Error*1 values of points 3 and 6 is that the default boundary condition in FEM makes the results around the boundary less accurate. Fortunately, enlarging the tile leads to a significant improvement in the accuracy for these cases, as *Error*2 turns out to be much smaller than *Error*1.

Doing comparisons on *E* on several points is not enough, as there are a very large number of points. The accuracy of *R* of wires is more important for getting the right evaluation of lifetime. As a result, another comparison is done for the *R* computed in the two cases. The nine evaluated wires are marked by red "∘" along with indices in Fig. 8. First, histograms of errors in *R* of all wires are plotted in Fig. 9. The definition of *Error*1 and *Error*2 is same as that in the previous comparison of *E*. It can be seen that enlarging the tile has greatly decreased the overall errors. Second, we list several extreme examples in Table 2 as we did with the comparisons of *E*. Wires A to C are wires with the highest damage accumulation rate. These wires are the ones of most interest and the table shows that the results for them are well-matched between all approaches. Wires D through F are wires with largest errors for setup 2 (FEM done in the red square). These significant errors are due to the fact that the nearby wires that are in the green square but not in the red square are missing in the FEM analysis. More importantly, *R* of wire D is not small, which means it can be a potential hotspot wire and thus the discrepancy on this wire is unacceptable. This further proves the necessity of enlarging the tile. Finally, wires G to I are wires with largest errors for setup 3 (FEM done in the green square). Note that the damage accumulation rates for all these wires are comparatively small, indicating that they are not the vulnerable wires that we are most interested in.

In conclusion, the proposed partition-based method, which is the last setup in the simulation, has achieved high accuracy on high-*E* spots,

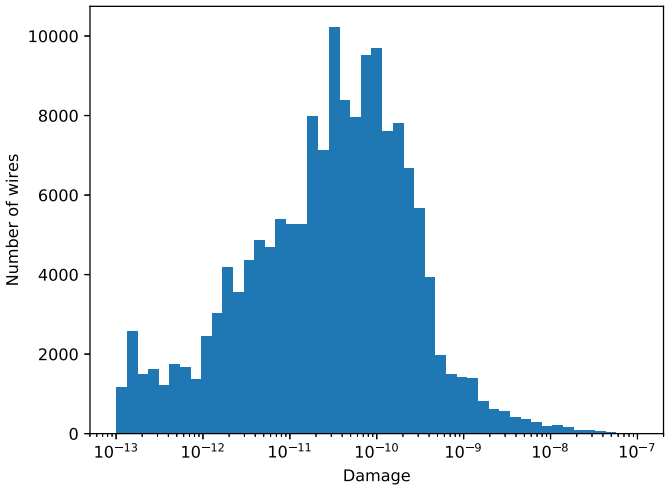

Fig. 10. Distribution of R among all wires.

and high-R interconnect wires, which are the objects of interest in this work.

5.3. Analysis of an example layout

Hotspot detection and full-chip lifetime analysis were carried out with the partition-based scheme on all interconnect metal layers. The number of wires and the damage accumulation rate of the most vulnerable wire in each layer is given in Table 3. Computation time for each layer is also listed in the table. FEM analysis takes most of the time for each layer. Lifetimes of each layer calculated with (7) are also listed. The lifetime of this synthesized chip calculated with (7) is 39.76 years.

M1 turns out to have the shortest lifetime, as opposed to upper metal layers in Ref. [3]. This is reasonable as there are many power delivery rails which are long and DC stressed. They are stressed with relatively higher electric fields because of narrower spaces in M1 and higher wire density. Additionally, M1 also has dielectric materials with the lowest dielectric constants, while upper metal layers with large space use more robust materials. Furthermore, the more complicated geometries compared with other layers make the lifetime even shorter because of the aforementioned layout effect. Hence, M1 is expected to have the shortest lifetime in all layers.

As to hotspot detection, Fig. 10 shows the distribution of R values of all wires. There are 733 wires with R ranging from 10^{-8} to 10^{-7}, and only 74 with R ranging from 5×10^{-8} to 10^{-7}, which means the analysis flow has identified a small number of hotspots wires from all 105286 wires. These wires would be the first ones that a designer would address in order to improve the BEOL TDDB reliability of the chip. Furthermore, it is possible that these 74 hotspot wires are composed of not only power delivery network wires, but also clock tree wires and signal wires. The latter two categories may be treated differently due to the lower duty factor, which would further reduce the number of serious hotspots.

As an example, a wire in M1 is identified as the most vulnerable in all wires across the chip. The full layer of M1 with this wire highlighted is shown in Fig. 11. It can be seen that the wire is actually a long power rail and spans a significant extent of the layout. Results of other interconnect layers also show that the most vulnerable wires are long wires. This is logical as (2) has introduced length scaling so that long wires are likely to be more vulnerable under similar stressing conditions. As the wire density in neighboring area along this wire is comparatively high, the integral in (6) is comparable to that of other wires, so its longer length contributes to its greater vulnerability.

Fig. 11. Full M1 layer view with most vulnerable wire highlighted.

6. Conclusion

A layout partition-based interconnect TDDB analysis flow has been proposed in this paper. Time to failure is evaluated by a newly-defined metric called TDDB Damage defined on each interconnect wire, and by comparing damage accumulation rates, hotspots (vulnerable) wires at high risk of TDDB failure) are identified. Based on electric fields analyzed from FEM, calculation of damage accumulation rate is conducted in each partitioned tile, and final results are obtained by merging and comparing intermediate results from small tiles. Since the approach is based on solving for electric fields, it can cover various electric field acceleration models commonly used and can also account for the non-uniformity of electric field in all layout patterns. The new method compares favorably in terms of accuracy against a recently proposed full chip TDDB method. This allows a better determination of risk and helps avoid overly pessimistic designs due to larger-than-required interconnect spacing.

Declaration of competing interest

No conflict of interests.

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