EMSpice: Physics-Based Electromigration Check Using Coupled Electronic and Stress Simulation

Zeyu Sun, *Student Member, IEEE*, Shuyuan Yu, *Student Member, IEEE*, Han Zhou, *Student Member, IEEE*, Yibo Liu, *Student Member, IEEE*, and Sheldon X.-D. Tan, *Senior Member, IEEE*,

***Abstract*—In this article, a novel full-chip EM simulation tool, called EMSpice simulator is proposed. The new method starts from first principles and simultaneously considers two major interplaying physics effects in EM failure process: the hydrostatic stress and electronic current/voltage in a power grid network. The new tool starts by reading the power grid layout information from Synopsys IC Compiler. It then removes immortal interconnect wires by considering both nucleation phase immortality and incubation phase immortality for multi-segment interconnects. Thereafter, a finite difference time domain (FDTD) solver is employed for stress analysis for every mortal interconnect tree for both nucleation and post-voiding phases. At the whole power grid circuit level, the EM analysis is coupled with IR drop analysis of a whole power grid network at each time step so that we can consider the interaction among stress, void growth, resistance change and IR drop in a single simulation framework. Accuracy of *EMSpice* is validated by comparing with a published EM simulator, XSim, for nucleation phase, and finite element method based COMSOL for post-voiding phase. The comparison results show that *EMSpice* agrees well with both methods with. Experimental results on two practical processor chip designs show that the proposed coupled EM-IR drop analysis method can further reduce the overly conservative EM-aware power grid design as the number of the failed trees found by *EMSpice* simulator is up to 76.7% less than the Black's method and 66.7% less than a recently proposed full-chip EM analysis method respectively. Furthermore *EMSpice* simulator is the least conservative one for lifetime estimation of individual tree wires among the three methods.**

***Index Terms*—Reliability, electromigration, power grid, finite difference method.**

I. Introduction

THE ELECTROMIGRATION (EM) effect remains a key failure mechanism for copper-based interconnects in sub-10nm technologies. Power-ground networks are the most vulnerable part among all the interconnect wires since the current flow on this part is the largest on the chip. A 2015 ITRS report predicts that the EM lifetime of interconnects of VLSI chips will be reduced by half for each generation of technology nodes [1] due to the increasing current density and shrinking wire line cross-sections, which determines the critical sizes for EM effects. As a result, the accurate and scalable full-chip EM assessment and sign-off is critical for VLSI circuits design in sub-10nm regime.

Accurately predicting the EM-induced time-to-failure for a full-chip power grid still remains a challenging task. Existing mean-time-to-failure (MTTF) EM models based on Black's equation [2] and Blech limit [3] only check EM effects based on current density in each individual segment. They are very simple and fast. However, such single-segment based EM assessment methods were shown to be less accurate in general for advanced VLSI nodes and the predicted time to failure can either be over-conservative or over-optimistic [4]–[7].

To mitigate this issue, a number of physics-based EM models and assessment techniques have been proposed recently [4]–[18]. At the core of those methods is the use of more accurate physics-based model, the Korhonen's equation, to describe stress behavior modeling in the confined multi-segment interconnect tree. Note that interconnects of chips are generally in the form of trees rather than single wires. However, this requires the more general, yet expensive numerical solutions of the partial differential equation of hydrostatic stress (Korhonen's equation) in confined metals subject to time-varying stressing current and temperature. Many research efforts tried to build the compact models by finding the analytic solutions to the Korhonen's equations with proper boundary conditions in both phases [8], [10], [11], [13], [19]. But many of those compact models can only work for restricted wire structures and topologies.

Recently, more general numerical solutions such as finite difference time domain methods [5], [17], [20] and finite element method [18] have been proposed. But those existing methods still mainly focus on solving the Korhonen's equation itself with less consideration of the inherent interaction between the stress, void growth, wire resistance and current densities change over time. No integration with commercial EDA flow has been demonstrated and compared on more practical VLSI layouts.

To address the aforementioned problems, in this article, we propose a new full-chip EM failure analysis tool, called *EMSpice*, for physics-based coupled EM and electronic analysis. *EMSpice* takes power grid netlists from Synopsys ICC flow, and outputs the failed EM wires and their resistance changes and resulting IR drops of the power grids over the given aging time. It can be used as a EM sign-off tool or

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The authors are with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA 92521 USA (e-mail: stan@ee.ucr.edu).

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used in the EM optimization engine for commercial EDA physical synthesis flow. Specifically, our new contributions are summarized below:

- *EMSpice* simulator simultaneously considers the hydrostatic stress and electronic current/voltage in a power grid network. The new method starts from first principles and can solve the resulting coupled time-varying partial differential equations in time domain to accurately stress evolution in multi-segment interconnect trees for EM failure analysis.
- *EMSpice* simulator employs a finite difference time domain (FDTD) solver for stress analysis for every interconnect tree for both nucleation and post-voiding phases.
- At the whole power grid circuit level, *EMSpice* simulator also couples the EM analysis with IR drop analysis at time domain. Thus the solver can consider the interplay among stress, void growth, resistance change and IR drop in a single simulation framework. Furthermore, *EMSpice* simulator considers both recently proposed nucleation phase immortality and incubation phase immortality for the first time to remove immortal interconnect trees from EM analysis. From the experiment it can be seen that up to 94.52% immortal trees are filtered out and EM simulation is accelerated by about 20 times.
- The accuracy of *EMSpice* simulator is validated by comparing it against a published EM numerical simulator XSim [21] for nucleation phase and finite element analysis (FEA) tool, COMSOL [22] for the post-voiding phase. The comparison results show that *EMSpice* agrees with both simulators very well with error less than 0.59% for XSim and 1.99% for COMSOL.
- *EMSpice* simulator can work seamlessly with Synopsys IC (ICC) compiler physical synthesis flow. *EMSpice* simulator reads the power grid layout from Synopsys ICC and it can output the power grid layout with current density, hydrostatic stress, IR drop, and void distributions for any given specific time on the power grid layout in a graphic way for better EM failure analysis and optimization.

Experimental results on two practical processors (*Cortex* and *ChipTop*) design show that *EMSpice* simulator can further reduce the overly conservative in EM-aware power grid design. The number of the failed trees found by *EMSpice* simulator is up to 76.7% less than the Black's method and 66.7% less than Huang's method [4].

This paper is organized as following: Section III reviews the EM model employed in this work. Section IV introduces the proposed EM failure check flow. Section V shows the numerical results obtained from our proposed method and comparison against existing works. Section VI concludes the article.

II. Related Works

A few full-chip EM analysis for power grid networks have been proposed recently [4], [5], [15], [20]. Their methods can predict the EM lifetime of the power grid and obtain failed trees. Specifically, Huang *et al.* proposed first physics-EM model based full-chip EM analysis method [4], [8]. The EM model in this method only considers nucleation and growth phase. An approximate closed form obtained from analytic solution of the nucleation phase of Korhonen's equation is employed to estimate nucleation time (t_{nuc}). Initial current densities are used for t_{nuc}. Resistance starts to increase immediately when the void is nucleated, i.e., $t > t_{nuc}$. If the time exceed the t_{nuc}, a simple linear model is used for resistance change calculation. This method indeed considers interaction between the EM and IR drops of power grids but the compact EM models are less accurate.

To get better accuracy, Chatterjee *et al.* and Sukharev and Najm proposed finite difference method (FDM) based full-chip EM analysis tool [5], [20]. In order to accelerate the simulation, a fitting-based immortal wire filter was applied in this work. Trees most likely to form a void were picked out and the FDM based method were only applied to solve these trees. The filter uses a conservative approximation model [23] to quickly estimate the nucleation time, t_{nuc}. If this estimated time is less than a time threshold, the trees were picked out for further EM simulation. Time threshold in this work [5] is estimated by the Monte Carlo process, specifically, being the mean of samples' TTF which has a limited normal distribution. Here the samples are from an IBM power grid.

FDM was applied to solve these mortal wires and a model order reduction technique based on matrix exponential form was applied to reduce simulation costs. However, this method also mainly considers the EM stress without considering impacts from wire resistance changes of power grid networks.

Cook *et al.* proposed a FDM accelerated by Krylov subspace based reduction technique [17]. This method can be applied to general multi-segment interconnect wires with time-varying currents and temperature. To further speed up FDM, the Krylov based subspace reduction techniques in frequency domain were applied, which leads to order of magnitude speedup over plain FDM. But this method still considers the EM stress and ignores the EM and IR drop interaction in power grid networks.

III. Review of EM Physics and Stress Modeling

EM is a physical phenomenon of the migration of metal atoms along the direction of the applied electrical field. Atoms (either lattice atoms or defects/impurities) migrate along the trajectory of conducting electrons. Due to momentum exchange between lattice atoms, hydrostatic stress is generated inside the embedded metal wire during migration process. Before the hydrostatic stress reaches the critical level, the atomic flux flowing caused by electron flow from cathode to anode can still balance with the atomic flux caused by inhomogeneous distribution of hydrostatic stress. When the stress reaches the critical level, a void and a hillock formation caused by conducting electrons will be formed at the cathode end and the anode end. Indeed, when metal wire is passivated into a rigid confinement, which is the case for copper dual damascene structures, the wire volume changes (induced by the atom depletion and accumulation due to migration), and creates tension at the cathode end and compression at the anode end of the line. However, if the hydrostatic

stress cannot reach critical level, the void will not be formed due to the balance between atomic flux flowing caused by electron flow and inhomogeneous distribution of hydrostatic stress.

Some traditional EM models are developed based on empirical data. Black's equation [2] and Blech limit [3] are still employed in the industry. However, these kind of models use empirical data to estimate MTTF conservatively so that the lifetime cannot be predicted accurately.

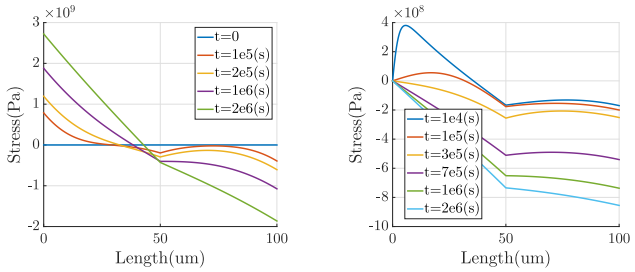
In order to avoid the inaccuracy and conservative issue caused by traditional EM models, many physics-based EM models have been subsequently developed. Some of them focus on steady state immortality check and others focus on transient hydrostatic stress. A physics based three phase model is proposed in [6], [7]. EM failure process in this work is described by nucleation phase(t_{nuc}), incubation phase(t_{inc}) and growth phase(t_{growth}). In nucleation phase, stress starts to accumulate and a void may form if the stress reaches the critical stress level at the cathode nodes. Once the void is formed, the process enters into the incubation phase in which the void starts to grow and no resistance change is observed. When the void depletes the cross section of the via, current will start to flow through the higher resistive barrier, which will lead to wire resistance change. Now the process enters into the growth phase, which can lead to either early failure or late failure depending on the electronic flux direction. In early faliure phase, open circuit can be observed. In late failure case, resistance starts to increase over time until it reaches to some pre-defined threshold like 10% change. TTF can be described as the summation of three phases as following:

$$TTF = t_{life} = t_{nuc} + t_{inc} + t_{growth} \tag{1}$$

The EM model used in this work is mainly based on Korhonen's equation, which is well accepted and experimentally validated. However, other effects such as multi mass transportation in microstructure [24], and effect of grain boundaries [25] are also very important for EM failure process. Impacts of metal microstructure and details of grain boundaries of the metal can affect the activation energy E_a, void nucleation sites, metal migration paths etc., which will affect the after-mentioned three EM phases.

For instance, scaling of the line width or feature size can change the micro-structure of the wires from polycrystalline to near bamboo structures as shown in [24], this can lead to the elimination of high diffusivity grain boundaries, but it may increase the mass transport at the surfaces between metal and capping and barrier layers due to the increased interface areas relative to volume.

On the other hand, for copper interconnect, especially in the deep micro region, the dominant transport paths for migration is between the capping layers and copper metal [26]. As a result, the impact of grain boundaries on EM failure process is less significant for copper wires than aluminum wires. As a mitigation, for instance, we can modify the activation energy E_a to take the effect of pass transportation variations in the changed microstructure and grain boundaries into consider.



(a) (b)

Fig. 1. EM-stress evolution of a two segments wire in the (a) nucleation phase (b) incubation and growth phase.

A. Nucleation Phase Modeling

Stress evolution is described by the stress-based model Korhonen's model [27]. Transient hydrostatic stress $\sigma(t)$ can be described by Korhonen's partial differential equation (PDE) with the following zero-flux boundary conditions (BC) and initial stress condition (IC) as shown in the following:

$$\frac{\partial \sigma(x,t)}{\partial t} = \nabla \cdot \left(\frac{D_a B}{k_B T} (\Omega \nabla \sigma(x,t) - eZ\rho j) \right), \quad \text{in } \Omega_L, \tag{2}$$

$$\nabla \sigma(x,t) = \frac{eZ\rho j_{N_i}}{\Omega}, \quad \text{on } \partial\Omega_L \cap \Gamma_{N_i}, i = 1, \ldots, k, \tag{3}$$

$$\sigma(x,0) = [\sigma_1(x,0), \sigma_2(x,0), \ldots, \sigma_k(x,0)], \ \textit{at } t = 0 \tag{4}$$

where $D_a = D_0\ exp(Ea/k_BT)$ is the effective atomic diffusivity. E_a is the activation energy of the failure process, T is defined as absolute temperature, e is the electron charge, eZ is the effective charge of the migrating atoms, ρ is the wire electrical resistivity, and j is the current density. Ω is the atomic lattice volume. B is the effective bulk elasticity modulus. k_B is the Boltzmann's constant. Ω_L is the domain of simulated copper interconnect and $\partial\Omega_L$ denotes its boundary. Γ_{N_i} is the ith flux termination boundary, where normal current density j_{N_i} are prescribed, among kth termination boundaries. In equation (2), a uniform D_0, synthesized from different body and boundary diffusion coefficients, is used. Note that Korhonen's hydrostatic diffusion equations can be applied to 3D multi-segments interconnect wires with multiple flux-termination boundary nodes, allowing any number of evolving voids to be simulated. Fig. 1(a) shows the stress evolution on a wire in the nucleation phase. As shown in the figure, stress at the cathode increase as time goes on. While, stress at the anode will decrease with time.

B. Incubation Phase Modeling

When stress reaches a critical level at t_{nuc}, a void is formed. However, the resistance of the interconnect remains almost the same since cross section of the via, which is recognized as critical volume, is not consumed by void. Once a void has nucleated when stress reaches a critical level at t_{nuc}, which is typically at or near a terminal node, the normal component of stress at the void boundary is typically zero. We then introduce the effective thickness of the copper-void boundary δ, which is infinitely small. Then we introduce the following stress gradient between the zero stress void surface and the surrounding

metal [27], [28]:

$$\nabla\sigma(x,t) = \frac{\sigma(x+\delta,t)}{\delta}, \quad \text{on } \partial\Omega_L \cap \Gamma_{\text{void}}, \tag{5}$$

where Γ_{void} denotes the void boundary, which can be a union of several discrete voids. The $\nabla\sigma(x,t)$ essentially serves as a force to move the void boundary toward the atomic flux direction. The void volume is determined by the stress distribution on the remaining section of the wire. Specifically, the void volume $V_v(t)$ in a multi-segment wire will satisfy the following atom conservation equation [29], [30].

$$V_v(t) = -\int_{\Omega_L} \frac{\sigma(t)}{B} dV \tag{6}$$

where Ω_L is the volume of the remaining interconnect wire and V is the volume of the wire and defined as $V = W \times h \times l$, where W is width of the wire and h is the thickness of the wire and l is the length of the wire. Notice that Eq. (6) is also true for the void growth phase, which we will discussed later. The incubation time can be defined as follows:

$$t_{nuc} < t < t_i \text{ where } V_v(t) < V_{crit} \tag{7}$$

where V_{crit} is the critical volume, which mainly depends on the cross section of the wire. In 1D case, we actually use width of wire W as the *critical length* instead of using critical volume to indicate the end of the incubation phase when the resistance starts to change. The reason is that $W \gg h$ and void will deplete the whole cross section of the wire when the void's cross-section boundary grows to W wide. Fig. 1(b) shows the stress evolution on a wire in the incubation phase. Stress at the cathode decrease to 0 very fast. Stress at anode keep decreasing until reach the steady state. This will lead to growth of the void since the integration of negative stress increase in Eq. (6). Void volume will saturate when the stress reach steady state.

Also, in the incubation phase, the void volume is not large enough to block the cross section of the via and smaller than critical volume. At the end of incubation phase a void will fill the cross section of the via. The void can cause either early failure or late failure of the wire [31]. Early failure typically happens in via above lines as shown in Fig. 2(a). The via will be blocked by the void and thus the connection to the upper layer will also be blocked (capping layer is fabricated with dielectrics such as Si_3N_4 which does not conduct current flow). In this case, the wire will fail in the end of incubation phase. Late failure typically happens in via-below structures as shown in Fig. 2(b). When the void forms in a via-below line and reaches critical size, current can still go through the barrier layer and the resistance will increase in the growth phase.

C. Growth Phase Modeling

In the void growth phase, the void continues to grow. The major difference between growth phase and the incubation phase is that wire resistance starts to change (at least meaningfully). The reason is that current has to flow over the highly resistive barrier which is made with T_a/T_aN for instance,

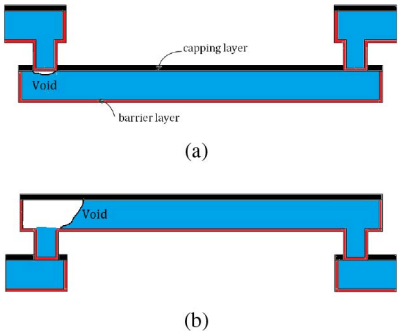


Fig. 2. Side-view of void formation: (a) void in a via-above line (early failure mode); (b) void in a via-below line (later failure mode).

whose resistivity is much higher than C_u. Specifically, the wire resistance change can be approximately described as:

$$\Delta R(t) = \frac{V_v(t) - V_{crit}}{WH}\left[\frac{\rho_{Ta}}{h_{Ta}(2H+W)} - \frac{\rho_{Cu}}{HW}\right], \text{ at } t_{inc} < t \tag{8}$$

where ρ_{Ta} and ρ_{Cu} are the resistivity of the barrier material (T_a/T_aN) and copper, W is the wire width, H is the copper thickness, and h_{Ta} is the barrier layer thickness.

We remark the if the liner/barrier becomes too thin (less than 3nm), then it will not be able to 100% block the metal mass migration as shown in [32] and [33]. In this case, basically metal mass flux will start to migrate over those barrieres and voids will not nucleate in the traditional cathode node so that the short length effects from Blech limit or from our advanced filtering methods will not work any more. This new phenomena will dramatically change the EM modeling and will be a good topic for further investigation once more experimental data is available from industry.

IV. The Proposed New Coupled EMSpice Simulation for EM Failure Check

A. The New Power Grid EM Check Flow

Before presenting the coupled EM-IR drop analysis for full-chip EM check and analysis, we first present the proposed new EM sign-off and check flow as shown in Fig. 3.

The whole EM check flow mainly consists of four major steps: the *power grid generation step* from the EDA tool (Synopsys ICC), *EM immortality filtering step*, the *FDTD EM solver and linear network IR drop solver*, and the *EM check framework GUI*. In the power grid generation step, the power grid information is constructed from Synopsys IC Compiler (ICC) during the physical synthesis process for a specific design. Power grid information is dumped during power grid synthesis step in ICC flow and the P/G layout geometrical and layer, via information as well as branch currents are also dumped at the same time. After this, the power gird and corresponding branch current are first passed to the EM immortality filter step (to be discussed in Section IV-C). Immortal trees are filtered out since they will never fail and resistance of these trees will never change. After this step, all the mortal trees are passed to the coupled solver step. The coupled solver consists of the FDTD for EM stress solver and linear network IR drop solver (which will be discussed in Section IV-B). In

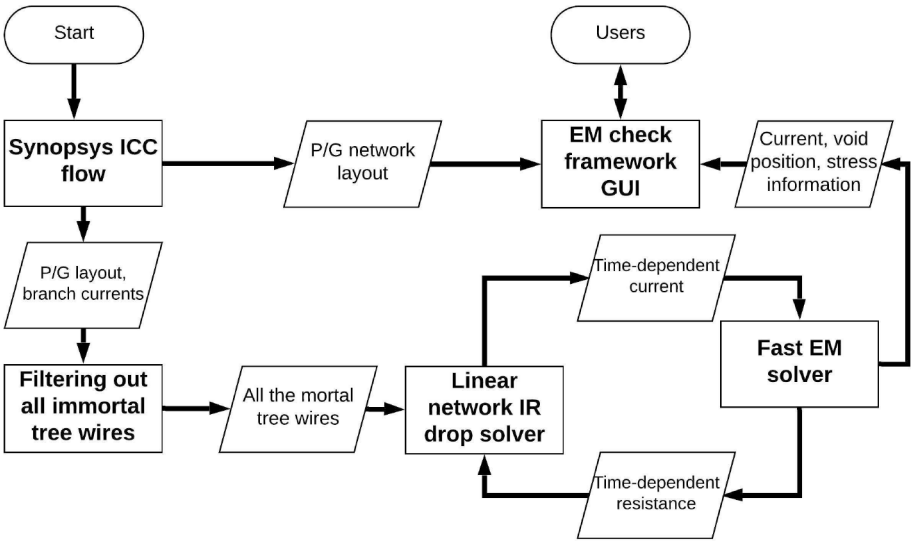


Fig. 3. Simulation Framework for *EMSpice* Simulator.

this step, hydrostatic stress on these mortal tree wires will be simulated and void position and volume size will be calculated. All this information will then be passed to the EM check framework graphical user interface (GUI) for interactive user analysis. The EM check framework GUI can show the current density, hydrostatic stress, IR drop, and void distributions for a given specific time. In the following section, we will present computing steps in detail.

B. Physics-Based Coupled Multi-Physics Power Grid Simulation

In order to improve the accuracy of the EM stress estimation in the full-chip power grid level, we have to consider multiple physics effects and their interaction: the stress evolution modeled by (2), atom conservation equation for void volume, and electrical potential change over time. It was shown, when void is formed, that the void volume (shapes) and the stress distributions of the remaining wire are correlated by the following atom conservation equation [29]

$$V_S(t) = \frac{1}{B}\int_{\Omega_L} \sigma(V,t)dV, \quad \forall t \tag{9}$$

where V_S is void volume. As a result, we can estimate void volume or sizes once we know the stress distributions.

For electrical potential, since EM analysis is done on a time scale of at least days, we treat the electrical potential distribution u as quasi static so it can be described by the strong form Laplace equation

$$\nabla \cdot \left(\frac{1}{\rho(\phi)}\nabla u\right) = 0, \quad \text{in } \Omega_L, \tag{10}$$

$$u = g_u, \quad \text{on } \partial\Omega_L \cap \Gamma_u, \tag{11}$$

$$\vec{n} \cdot \frac{1}{\rho(\phi)}\nabla u = g_j, \quad \text{on } \partial\Omega_L \cap \Gamma_j \tag{12}$$

where $\rho(\phi)$ is the copper resistivity that is implied by the phase field, Γ_u denotes boundaries where Dirichlet (voltage) conditions are applied and g_u represent voltage/potential source, Γ_j denotes the boundaries where Neumann (normal current flux) conditions are applied and g_j represents current density source. For our full-chip EM analysis, however, it will be very expensive to solve (10) using the numerical approaches. Instead, we assume that homogeneous current density distribution along the wires and simple resistance network is extracted from the power grid network layout. The modified nodal analysis (MNA) is applied, which will lead to

$$\mathbf{M}(t)u(t) = \mathbf{P}I(t) \tag{13}$$

where $\mathbf{M}(t)$ is the admittance matrix for the power grid network, which is time-varying due to the fact that wire resistance will change with EM failure effects over time. $\mathbf{P}$ is the $b \times p$ input matrix, where p is the number of inputs or the size of driving current density sources $I(t)$. $u(t)$ represent the nodal voltages in the network and $I(t)$ are the current sources from the function blocks of the chips. From this equation, we can also compute the branch current and nodal voltages of all the branches, which are required for both immortality check and Korhonen's equation.

For Korhonen's equation, the FDTD method is carried out for each multi-segment interconnect tree for detailed stress analysis over time. We follow the similar work [17] without the model order reduction feature. After the finite difference discretization process, the partial differential equation in (2) with boundary conditions will be converted to the following linear time invariant (LTI) system:

$$\begin{aligned} \mathbf{C}\dot{\sigma}(t) &= \mathbf{A}\sigma(t) + \mathbf{P}I(t), \\ \sigma(0) &= [\sigma_1(0), \sigma_2(0), \ldots, \sigma_n(0)] \end{aligned} \tag{14}$$

C, A are $n \times n$ matrices. $\mathbf{P}$ is the $b \times p$ input matrix, which is also used in (13). Note that $\sigma(0)$ is the initial stress at time 0. For each new simulation step, the stress from previous simulation will be used as the initial condition. Now we are ready to present the final coupled EM-IR drop partial differential equations which can be written as follows:

$$\begin{aligned} \mathbf{C}\dot{\sigma}(t) &= \mathbf{A}\sigma(t) + \mathbf{P}I(t), \\ V_v(t) &= \int_{\Omega_L} \frac{\sigma(t)}{B} dV, \\ \mathbf{M}(t) \times u(t) &= \mathbf{P}I(t), \\ \sigma(0) &= [\sigma_1(0), \sigma_2(0), \ldots, \sigma_n(0)], \ \textit{at } t = 0 \end{aligned} \tag{15}$$

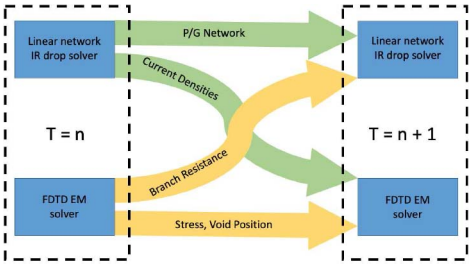


Fig. 4. Block diagram of coupled FDTD and IR drop power grid simulator.

The three equations are coupled and solved together as shown in Fig. 4. Linear network IR drop solver passes time-dependent current density information and P/G layout information to the FDTD EM solver. Once the voids are formed and IR drops in the power grid will change, the current at each time step will be different. The FDTD EM solver will provide the IR drop solver with new resistance information for wires with voids. As we can see, these two simulations are coupled together, and wire current and resistance depend on each other for each mortal wires. Note that **C, A** matrices, which depend on wire structures, are time-independent in the coupled equation.

We note that wire length also change with void growth, which is considered in the coupled simulation. The length of segment with void is updated each iteration and become shorter with void growth. This change is very small, and do not have very significant effect on the stress distribution on the tree since the void size generally is less than 1% of the total size of a tree.

We remark that the voids of all mortal wires will reach to saturation volume after a number of simulation steps/cycles. Typically we select one month as one simulation step. So the number of steps for void to reach saturation depends on the specific wire and its current density distributions.

Impact of resistance change of power grid networks may loosen the EM constraint significantly since current densities of the interconnects reduce. However, this effect is not thoroughly studied in aforementioned methods in Section II. Huang's method [4], [8] considers this impact in the growth phase with linear model. But the accuracy of compact linear model is not high enough for resistance estimation. Besides, Chatterjee's method [5], [20] and Cook's method [17] focus on EM stress analysis and ignore the impact of resistance change caused by EM and IR drop interaction in power grid networks.

We remark that the proposed work can be easily extended to consider statistical aspects of EM failure process using Monte Carlo or other stochastic analysis methods as as shown in some existing works [5], [34].

C. EM Immortality Filtering

FDTD based EM simulation is still computationally intensive for full chip EM analysis. With the sheer number of interconnect trees in a chip, FDTD is not efficient. However, in most designs, the tensile stress of many trees will not exceed the critical level and no void will be formed on these trees. Besides, trees that do nucleate a void do not mean they will fail since the void may not be large enough to exceed the critical void volume. If a tree is either nucleation phase immortal or incubation phase immortal, the resistance does not change. In other words, these trees will not have any impact on the IR drop and FDTD EM simulation is not necessary on these trees. We first present the immortality filter flow.

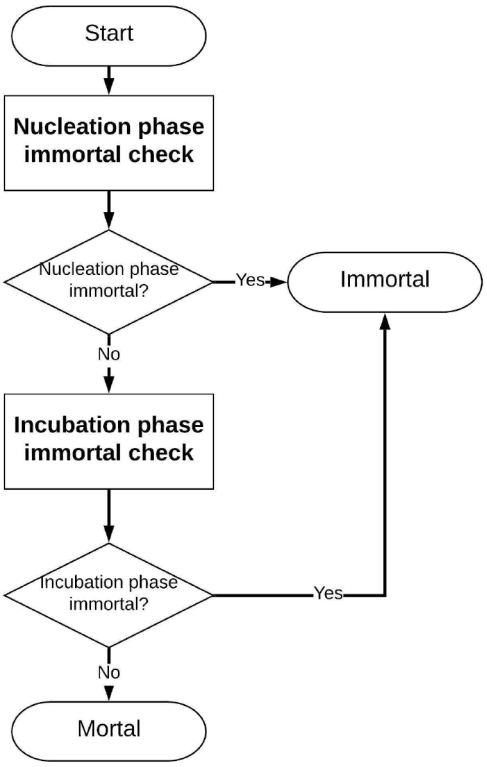


Fig. 5. Block diagram of EM immortality filter.

1) The Immortality Filtering Flow: The immortality check flow is shown in Fig. 5, which consists of two filtering algorithms. First, a tree in the power grid is checked by nucleation phase filtering to see if voids can be nucleated. If no void can be nucleated, the wire is immortal. If voids will be nucleated, the tree is then passed to incubation phase immortality filter. If voids volume cannot exceed critical void volume, the tree is still treated as immortal. Only the mortal trees whose resistance will change are simulated with coupled EM-IR simulation.

We remark that the Blech's product was widely used to find the immortal wire before. However, it only works for single-segment [3]. For multi-segment wires, a conservative approximation method has been proposed [5], [20]. The proposed EM filtering method is based on physics-based models for the immortality and thus is more predictable for over a wide range of stress conditions and technology nodes. Also we consider both nucleation and incubation immortal cases for the first time. In the section, we briefly discuss the two filtering algorithms.

2) Nucleation Phase Immortality Filtering: If the stress on the cathode of a tree, at steady state (σ_{steady}), is lower than the critical stress (σ_{crit}), then the tree is considered to be *EM nucleation phase immortal*. Based on the well-known

steady state analysis method *Blech product* [3], if the current density and the wire length are not large enough, σ_{steady} cannot exceed σ_{crit}. However, this method is only suitable for a single wire with only one branch. Recently, a voltage-based EM nucleation phase immortality analysis method for multi-branch interconnect trees has been proposed [12], [15].

In this method, an *EM voltage* ($\mathcal{V}_E$) which is proportional to stress at the cathode node (σ_c) is calculated as

$$\mathcal{V}_E = \frac{1}{2A}\sum_{i\neq c} a_i \mathcal{V}_i \tag{16}$$

where $\mathcal{V}_i$ is the normal nodal voltage (with respect to cathode node c) at node i, a_i is the total area of branches connected to node i and A is the total area of the wire. This equation was derived based on atomic conservation principle [12]. With the voltage of the ith node($\mathcal{V}_i$), steady state stress at that node (σ_i) can be calculated as $\sigma_i = \beta(\mathcal{V}_E - \mathcal{V}_i)$, where $\beta = \frac{eZ}{\Omega}$, e is elementary charge. A *critical EM voltage* $\mathcal{V}_{crit,EM}$ is defined by

$$\mathcal{V}_{crit,EM} = \frac{1}{\beta}(\sigma_{crit} - \sigma_{init}) \tag{17}$$

where σ_{init} is the initial stress.

EM failure will not happen if cathode node can pass the immortality check since it has the lowest voltage among all the nodes on a tree. Following equation is the condition of immortality of the tree:

$$\mathcal{V}_{crit,EM} > \mathcal{V}_E - \mathcal{V}_{cat} \tag{18}$$

where $\mathcal{V}_{cat}$ is the voltage at the cathode.

3) Incubation Phase Immortality Filtering: Voids are formed on trees that do not pass the nucleation phase immortality. After a void is formed, it will keep growing until saturated. Void saturation happens when two kinds of flux balance with each other. One is the flux of atoms previously located in metal which is consumed by the growing void and the other is the back flux of atoms generated by a gradient of growing stress. If the void volume is smaller than the volume of the intersection, which is recognized as critical volume V_{crit}, current can still flow through the copper wire as the wire cross-section is not blocked by the void. Once the void size is large enough and occupies the wire cross-section, current has to go through the liner whose resistivity is much higher than copper and the resistance of the wire will increase. As can be seen, if the saturation volume is smaller than critical volume, the wire is still immortal although a void is formed. This case is called *EM incubation phase immortal*.

In order to determine if a wire is immortal, a model predicting the saturation volume V_{sat} was proposed in [35] shown as following

$$\begin{aligned} V_{sat} &= \sum_i V_{sat,i} = h \times \sum_i A_{sat,i} \\ &= h \times \sum_i \left[\left(-2\sigma_{c,i} + \frac{j_i l_i \rho e Z}{\Omega} \right) \times \frac{l_i w_i}{2B} \right] \\ &= h \times \sum_i \left[\left(-2\sigma_{c,i} + \frac{\mathcal{V}_i e Z}{\Omega} \right) \times \frac{l_i w_i}{2B} \right] \end{aligned} \tag{19}$$

where h is thickness of the wire and $V_{sat,i}$, $A_{sat,i}$, $\sigma_{c,i}$, $\mathcal{V}_i$, j_i, l_i and w_i represent the contribution to void volume, contribution to void area, stress at the cathode, current density, voltage and length and width of the ith segment respectively. For the segment in which a void has nucleated, $\sigma_{c,i}$ is 0 on the cathode where the void is nucleated. Except for the segment with the void, steady-state stress on the cathode of other segments are the same as the anode of the segment connected to them.

As shown in the Eq. (19), voltage and width on each branch i can contribute to the void volume. So saturation void volume can be adjusted in order to reach incubation immortality by modifying the voltage and width of the branches.

In order to know if the wire is EM incubation phase immortal, saturation volume is compared with the critical volume, specifically, it should satisfy the following equation

$$V_{crit} > V_{sat} \tag{20}$$

We remark that our incubation phase filtering is based on the assumption that void is nucleated in the cathode node, which has the largest tensile stress. However, for cases that void nucleated outside the cathode nodes, the immortality study needs to be future investigated.

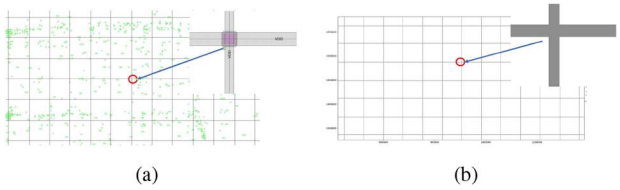
V. Numerical Results and Discussions

In this section, we present the numerical simulation and comparison results of the proposed *EMSpice* simulator. In our implementation, EM immortality filtering and Linear network IR drop solver are implemented in C++, FDTD EM analysis engine/solver was implemented in MATLAB and EM check framework GUI is implemented in Python 3.6.0 with Matplotlib. The experiments were carried out on a Linux server with dual 3.3-GHz Xeon processors and 316GB memory.

In order to validate our work, we use two test cases. The first test case is the power grid of the Cortex-M0 DesignStart processor, named (*Cortex*). This is a 32-bit processor that implements the ARMv6-M architecture [36]. This processor is synthesized using Synopsys Design Compiler, and is placed and routed with Synopsys 32/28*nm* Generic Library [37]. The power grid of *Cortex* has two layers, and there are 68 trees in total.

The second case is also microprocessor design called *ChipTop*. *ChipTop* was provided by Synopsys Electronic Design University Program [38]. It is a low power design processor architecture, which contains cache blocks, I/O standard cells and digital standard cells. It is also synthesized using Synopsys Design Compiler, and is placed and routed with Synopsys 32/28*nm* Generic Library [37]. *ChipTop* has a 4 layers power grid with 912 trees.

Fig. 6 shows the power grid layout of *Cortex* from Synopsys ICC and the same power grid in the EM check framework GUI (graphic user interface) system. In the Fig. 6(a), green boxes are standard cells and the mesh structure is the power grid. The zoomed area of this power grid is also shown in Fig. 6(a). Fig. 6(b) is the power grid from the EM check framework GUI. EM check framework GUI can also display the layout in an interactive way like Synopsys ICC. Zoomed power grid is also displayed in Fig. 6(b).



(a) (b)

Fig. 6. (a) Part of power grid of *Cortex* in Synopsys ICC. (b) Part of power grid of *Cortex* in proposed EM GUI.

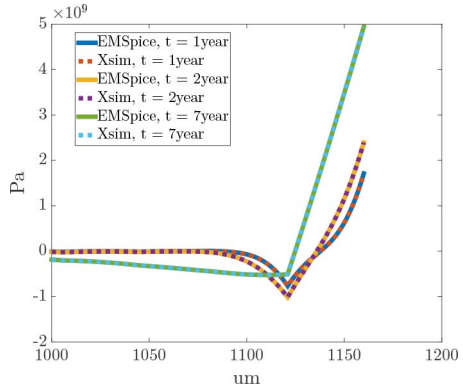


Fig. 7. Stress comparison between the *EMSpice* and Xsim on a wire from *Cortex*.

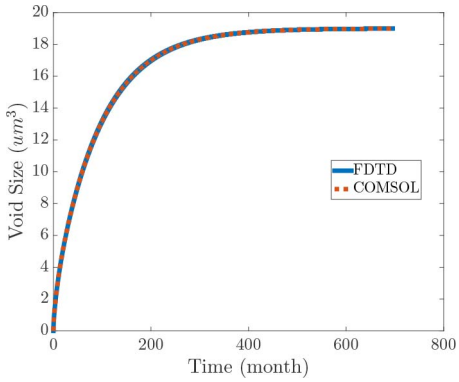


Fig. 8. Void size comparison between *EMSpice* and COMSOL on a wire from *Cortex* design.

TABLE I
VOID SIZE COMPARISON BETWEEN *EMSpice* (FDTD) AND COMSOL ON A WIRE FROM *Cortex*

Time after void formed	1 year	3 year	7 year
Void size from *EMSpice* (um^3)	3.63	7.38	12.04
Void size from COMSOL(um^3)	3.69	7.53	12.16
Error	1.65%	1.99%	0.98%

Power grid information obtained from Synopsys ICC is then fed into the proposed *EMSpice* simulator. For power grid network for *Cortex*, the *EMSpice* simulation takes about 67.14 second to finish. It takes 381.2 seconds for the simulation of power grid of *ChipTop*. In the following, we present more analysis and comparison results for these two cases.

A. Accuracy Comparison Against Existing EM Analysis Methods

We first compare the proposed *EMSpice* method with existing EM analysis methods in terms of accuracy. We verify the accuracy of the FDTD EM analysis engine used in the *EMSpice* for both nucleation and post-voiding phases on a few wire trees from the *Cortex* design.

We first compare the *EMSpice* with a published EM simulator XSim [21] for stress analysis of multi-segment wires in the nucleation phase. XSim is widely used to calculate the hydrostatic stress evolution in an interconnect which is assumed to be confined within diffusion barriers and it has been validated by the measured results. We take a tree from *Cortex* for stress comparison in nucleation phase. Fig. 7 shows the stress comparison between *EMSpice* and XSim at different time. Average error between these two method is only 0.53%, which is very small and can be ignored.

For EM post-voiding phase comparison, we compare *EMSpice* with the simulation result of a finite element analysis (FEA) tool, COMSOL [22] based on the same partial different equation and post-voiding boundary conditions in [28]. The void volume is also computed by using atom conservation equation (Eq. (6)). A 2D structure wire was used in the COMSOL simulation. This is a multi-segment straight wire with length 1170*um* and width 0.2 *um*. And there are 34 vias on this wire. Fig. 8 shows comparison on void size over time between *EMSpice* and COMSOL, which shows that their results match very well.

Table I shows detailed void size comparison between the two methods on different time for the aforementioned wire in Fig. 8. As can be seen, the error is less then 1.99% and accurate enough for the void volume estimation.

We want to remark that the Korhonen's equation for EM failure modeling is well accepted in the research communities as it has been validated against the silicon data and explained well the EM failure processes observed in experimental data in many published works [7], [23], [26]–[28], [39], [40]. XSim [21] is also tested against the measured results from the properly designed wire test structure. As a result, comparison against FEM analysis based on Korhonen's equation and XSim will provide good accuracy validation for EMSpice.

B. Filtering and Coupled Simulation Results of Cortex

Firstly, efficiency of EM immortality filter is employed to reduce time of EM simulation of *Cortex*. This power grid has 68 trees in total. Among all of these trees, 42 trees are filtered out by nucleation immortality filter and 15 mortal trees among them are filtered out by incubation phase immortality filtering algorithm. So the proposed EM immortality can filter out 78% trees, which translating to accelerating the whole simulation by almost 5 times. Fig. 9 shows the mortal trees (highlighted with current density distribution in the whole chip layout). As we can see, most of the mortal wires are located around the peripheral of the chip.

After the filtering of the immortal wires, we start to analyze the lifetime of mortal wires in the coupled *EMSpice* simulator. As time passes, the stress starts increasing and voids are

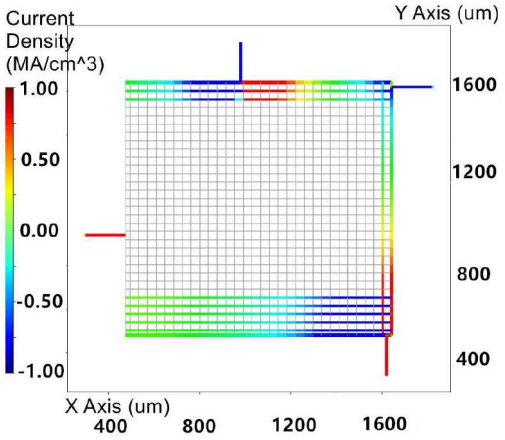


Fig. 9. Current densities of the mortal trees. (X and Y in *um* and current densities in MA/cm^2).

TABLE II
PARAMETER FOR THE EM SIMULATION

Name	Symbol	Value
Atomic lattice Volume	Ω	$1.19 \times 10^{-29} m^3$ [43]
Critical stress	σ_{crit}	$500Mpa$ [44]
Critical EM voltage	$\mathcal{V}_{crit,EM}$	$3.69 \times 10^{-3} V$ [15]
Critical volume	V_{crit}	depends on via size
Effective bulk elasticity modulus	B	$1 \times 10^{11} Pa$ [45, 46]
Effective charge number	Z	10 [47]
Temperature	T	373K

formed. Fig. 10 shows the stress evolution and void formation in the power grid.

As can be seen from the Fig. 10 in the 8th year, all the wires are still in the nucleation phase. Stress at some hotspots has increased to a high level. In the 12th year, some voids are formed and stress near to the void starts decreasing. These wires get into incubation phase and void sizes at that time are very small and not enough to block vias cross sections. In the 20th year, more voids are nucleated and most of them are in the growth phase. Some voids have grown to the saturation volume. As aforementioned in Section III-B, stress accumulated on the cathode before void nucleation and decrease to zero very fast after the void formed. A set of zoomed figures of void growth process is shown in Fig. 11.

Fig. 12 shows the voltage drop on the full-chip power grid. As we can see, there are significant voltage drop in two areas where the void forms. It also shows that the void formation causes the resistance change and leads to large voltage drop.

Fig. 13 shows resistance change over time of one of the mortal trees experiences the late failure effect. As shown in the figure, the void is formed at the end of nucleation phase. However, the resistance does not change at that time. At the end of incubation phase, the void occupies the cross section of the via, and resistance starts to change since this is a late failure case. The resistance change pattern shown in Fig. 13 based on the three-phase EM model mentioned in Section III, is consistent with the experimental observation [46]. When the increment of resistance reaches 10% (note that this failure criterion is used for illustration purpose), this tree is marked as failed. Finally, the void saturates and resistance change stops. Node voltages keep changing with time after void volume exceeds a critical level. As shown in Fig. 14, voltage changes

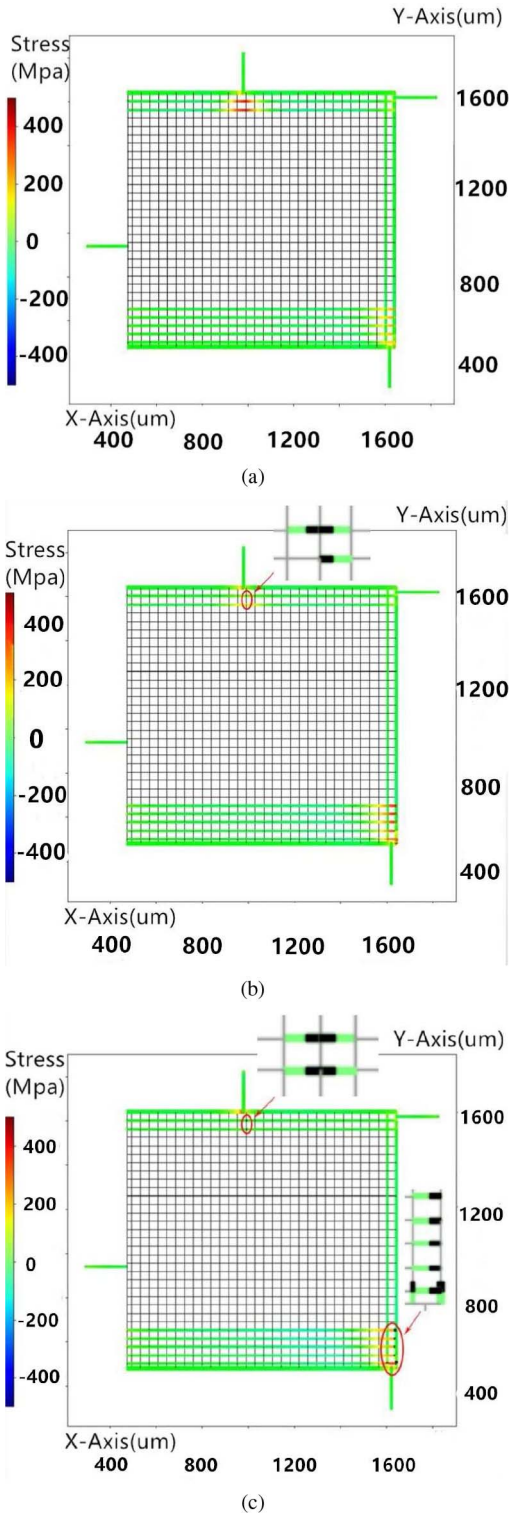


Fig. 10. (a) Stress distribution and void formation at 8th year; (b) 12th year; (c) 20th year for *Cortex* design. (X and Y in *um* and stress in *Mpa*).

with void growth and a sudden voltage drop happens once a new void exceeds the critical level. Compared with Fig. 14 and Fig. 15, it can be observed that the time when sudden voltages drop matches well with the time when voids exceed critical volume.

Fig. 15 shows the resistance of some failed tree wires. We can see that trees failed at different times. Both early failure

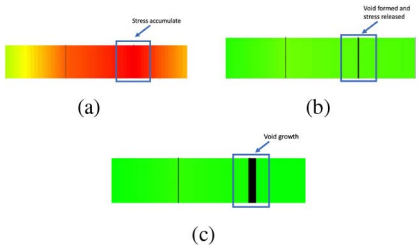


Fig. 11. (a) Zoomed stress distribution and void formation at 8th year, (b) 12th year, (c) 20th year of *Cortex* design.

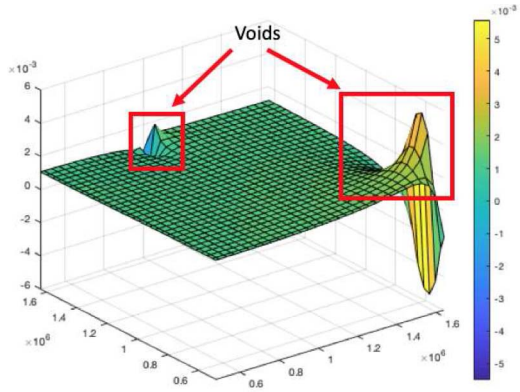


Fig. 12. Voltage drop on the power grid of *Cortex*.

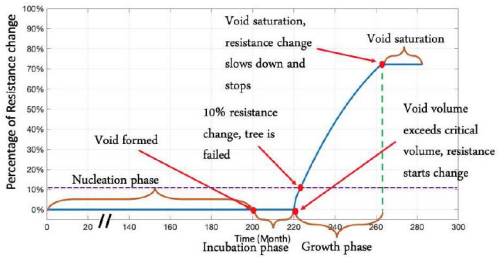


Fig. 13. Resistance change over time on a mortal tree on power grid of *Cortex*.

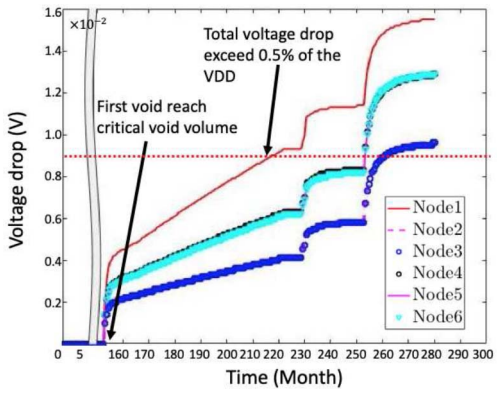


Fig. 14. Voltage drop change over time for different nodes on power grid of *Cortex*.

and late failure can happen in this power grid. Early failure cause open circuit and resistance goes to infinite. Resistance of late failure trees increase gradually and finally stop when voids reach saturation volume.

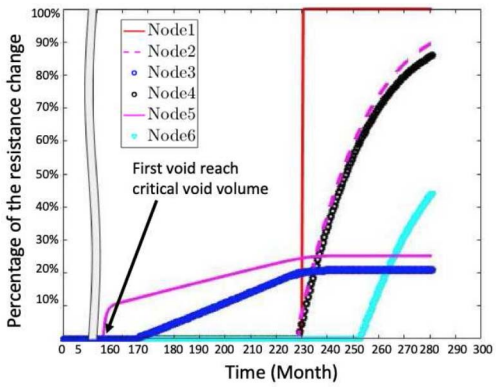


Fig. 15. Resistance change over time of failed interconnect tree wires on power grid of *Cortex*.

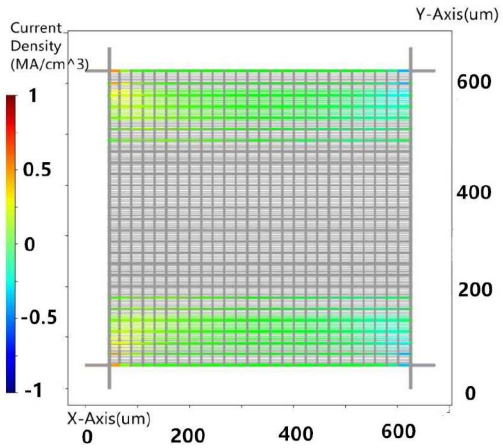


Fig. 16. Current densities of the mortal trees on power grid of *ChipTop*. (X and Y in *um* and current densities in MA/cm^2).

C. Filtering and Coupled Simulation Results of ChipTop

EM immortality filter is also applied for power grid of *ChipTop* which has 912 trees in total. As shown in Fig. 16, there are only 50 failure trees on the power grid. Among all of these trees, 695 trees are filtered out by nucleation immortality filter and 177 immortal trees are filtered out by incubation phase immortality filtering algorithm. After filtering, there are only 5.48% mortal trees which need further EM analysis. The immortality filtering dramatically reduce the simulation by about 20 times. Fig. 16 shows the mortal trees (highlighted with current density distribution in the whole chip layout) of *ChipTop* design. We observe that many mortal tree wires are thin wires. The reason is that these thin wires has small critical volume, although their saturation volume is not that large, they are still mortal. On the other hand, some large wires have larger critical volume. Even though their saturation volume is larger than thin wires, they are still incubation phase immortal.

Fig. 17 shows void formation process of *ChipTop*. Voids are not nucleated at 8th year. This time all trees are in the nucleation phase. As can be seen in the figure, stress are accumulated at cathodes. At 10th year, voids start to be formed and many wires enter incubation phase. We can see the stress near voids decreasing to zero in this figure. At 17th year, most voids

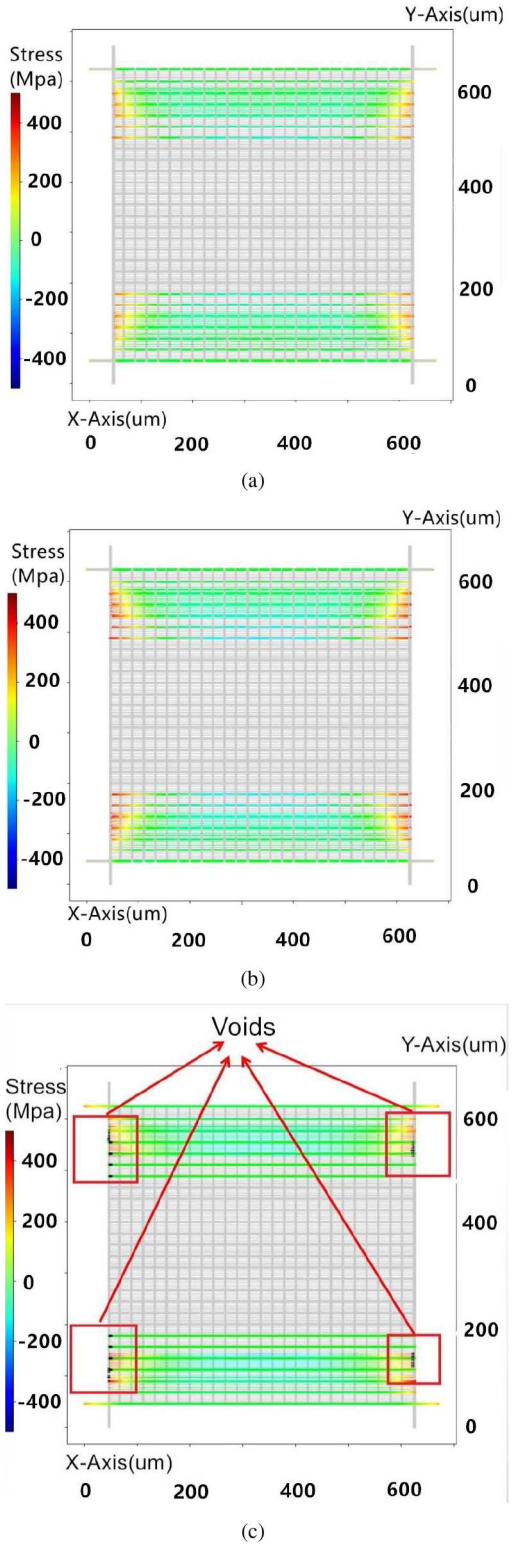


Fig. 17. (a) Stress distribution and void formation on power grid of *ChipTop* at 8th year; (b) 10th year; (c) 17th year. (X and Y in *um* and stress in *Mpa*).

are formed and some of them already reaching saturation volume. Zoomed figures of voids are shown in Fig. 18. As can be seen in the figure, the voids are gathered in the edges of the power grid. Similar with the *Cortex*, the lines on the edge have larger current densities and they are more vulnerable. Based

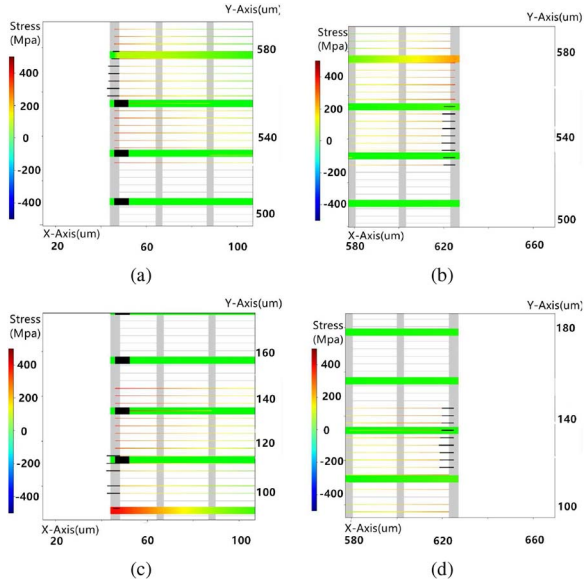


Fig. 18. Void distribution on the *ChipTop* at 17th year on (a), left up corner (b) right up corner, (c) left down corner, (d) right down corner.

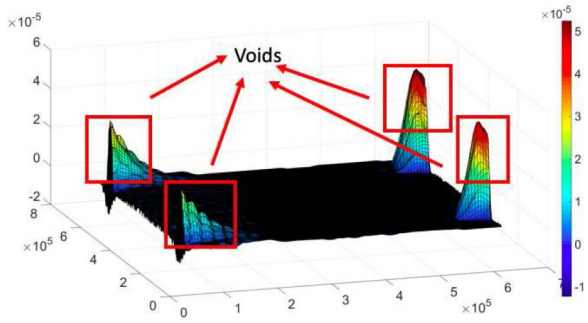


Fig. 19. Voltage drop on the power grid of *ChipTop*.

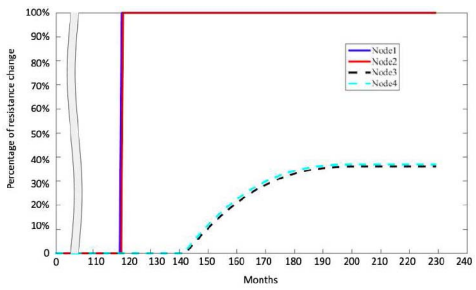


Fig. 20. Resistance change of mortal wires on the power grid of *ChipTop*.

on the result of these cases, in the design, wires on edges of the power grid need to be optimized to avoid EM failure.

Fig. 19 shows the voltage change on the power grid of *ChipTop*. The voltage change significantly on the location where voids are formed. As can be seen, hill of voltages changes are in the four corners of power grid. Both early failure and late failure contribute to the voltage change in these locations.

Fig. 20 shows resistance change of some typical wires. In the figure, two wires are early failure and the other two wires are late failure. Here two early failure wires are with smaller

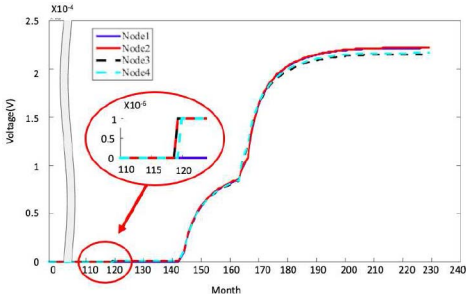


Fig. 21. Cathode voltage drop of mortal wires on the power grid of *ChipTop*.

TABLE III
COMPARISON OF FAILED TREE NUMBER OF THREE METHODS ON THE POWER GRID OF *Cortex*

Simulation time		8 years	12 years	20 years
Black's method	Failed tree number	24	24	24
	Failed tree percentage	35.3%	35.3 %	35.3%
Huang's method	Failed tree number	11	13	16
	Failed tree percentage	16.2%	19.1 %	23.5%
EMSpice simulator	Failed tree number	0	2	9
	Failed tree percentage	0%	2.9 %	13.2%

current. They fail faster since the cross section of the vias on these wires are also smaller. The other two late failure wires have larger current. They are wider wires with large cross section of the vias and long incubation phases. So their resistance change happens later. As can be seen in the Fig. 21, wires with less current have less contribution to voltage change even though they have early failure and have significant resistance change. Voltage change caused by these wires are only about 1% of the voltage change caused by wires with large current density. However, for wires with large current, there is very obvious voltage change when their resistance starts increasing.

D. Comparison Against Existing Full-Chip EM Analysis Methods

In this section, we compare the proposed *EMSpice* simulator against one existing full-chip EM analysis method. We compare the *EMSpice* against two methods: the traditional Black's method in which the time to failure is calculated for each segment based on Black's equation [2] with the same parameters used; we also employ Huang's method [4] as another baseline.

The comparison result of power grid of *Cortex* is shown in Table III and result of power grid of *ChipTop* is shown in Table V.

In the Black's method, tree failure only depends on the current densities on that tree. It cannot consider time-varying current change in the power grid. Compared with other methods, Black's method leads to most conservative results. Around 35% of the trees in the power grid of *Cortex* and 30.4% of the trees in the power grid of *ChipTop* are estimated to be failed by this method. Huang's method considers both nucleation phase and growth phase. But this method still is less accurate as compact models are used for both nucleation and growth phases. It marks 23.5% trees in the power grid of *Cortex* and 18.9% trees in the power grid of *ChipTop* as the failed trees in the 20th year.

The proposed *EMSpice* simulator shows only 13.2% failed tree wires in the power grid of *Cortex* and 4.4% failed trees in the power grid of *ChipTop* in the 20th year. As we can see, at the 20th years, the number of the failed trees by *EMSpice* simulator is 63.5% less than the Black's method and 43.8% less than Huang's method in the *Cortex* case. There are 76.7% less than the Black's method and 66.7% less than Huang's method in the *ChipTop* case. As we can see, *EMSpice* method can significantly reduce the over-conservations from the existing two methods, which can lead to more aggressive design with less guard bands, which leads to better performances under the same design costs.

TABLE IV
LIFETIME COMPARISON OF THE THREE FULL-CHIP EM ANALYSIS METHODS ON THE POWER GRID OF *Cortex*

Trees name	Time to Failure (years)		
	Black's method	Huang's method	*EMSpice* simulator
Tree 1	8.33	immortal	immortal
Tree 2	4.45	9.17	immortal
Tree 3	3.08	6.16	16.67
Tree 4	2.17	4.50	14.58
Tree 5	1.67	3.67	10.41

TABLE V
COMPARISON OF FAILED TREE NUMBER OF THREE METHODS ON THE POWER GRID OF *ChipTop*

Simulation time		8 years	10 years	17 years
Black's method	Failed tree number	227	227	227
	Failed tree percentage	30.4%	30.4%	30.4%
Huang's method	Failed tree number	98	144	165
	Failed tree percentage	10.7%	15.8 %	18.9%
EMSpice simulator	Failed tree number	0	17	40
	Failed tree percentage	0%	1.9 %	4.4%

TABLE VI
LIFETIME COMPARISON OF THE THREE FULL-CHIP EM ANALYSIS METHODS ON POWER GRID OF *ChipTop*

Trees name	Time to Failure (years)		
	Black's method	Huang's method	*EMSpice* simulator
Tree 1	12.14	immortal	immortal
Tree 2	6.39	12.77	immortal
Tree 3	4.35	9.58	12.1

Furthermore, we also look at the lifetime of some immortal and failed trees. Their lifetime given by the three methods are shown in Table IV. As we can see, the proposed *EMSpice* still gives the long lifetime estimation among the three methods for the five tree wires. The difference can be quite significant (up to 6.71X longer). Further, we observe that the immortal tree wire marked in the *EMSpice* method can be considered as mortal tree wires in both the Black's method and Huang's method. The reason is that the *EMSpice* method considers the unique incubation phase immortality case and it can identify the nucleated wires as immortal as long as their void sizes are small enough.

We want to remark that longer lifetime estimation for EM analysis does not alway mean better accuracy as recent work shows that Black's model can be also optimistic as well [5]. But in general, Korhonen's based EM models, more physics-based EM immortality filtering, and more accurate post-voiding analysis tend to lead to more accurate results, which typically are less conservative than existing Black-Blech based EM models and other compact models as shown in many recent works [4]–[6], [11], [16], [20].

VI. Conclusion

In this paper, we have proposed a novel full-chip electromigration verification for power grid network of nanometer VLSI chips. The new method simultaneously considers two physics effects in interaction: the hydrostatic stress and electronic current/voltage in a power grid network. It can solve the resulting coupled time-varying (partial) differential equations in time domain to accurately predict time-to-failure for a power grid in the entire chip. The new tool reads the power grid layout from Synopsys ICC. Then an immortality filter considering both nucleation phase immortality and incubation phase immortality is applied to remove immortal interconnect trees from EM analysis. A finite difference time domain solver is employed for stress analysis for every interconnect tree. Metal atom conservation equation is used to estimate the void volume change and resistance increments over time. The EM analysis is coupled with IR drop analysis of a whole power grid networks at each time step so that we can consider the interplay among stress, void growth, resistance change, and IR drop in a single simulation framework. Accuracy of *EMSpice* has been validated by comparing with a published EM simulator, XSim, for nucleation phase, and finite element method based COMSOL for post-voiding phase. The comparison results show that *EMSpice* agrees well with both methods very well. The experimental results on commercial processor chips design have shown that the proposed *EMSpice* simulator can further reduce the over-conservation in EM-aware power grid design as the number of the failed trees found by *EMSpice* simulator is 76.7% less than the Black's method and 66.7% less than recently proposed full-chip EM analysis method respectively.

VII. Future Work

EM failure process on mainstream copper interconnect is a complicated physics phenomenon with a statistical nature. The proposed work can be extended to different aspects. First we would like to consider the Joule heating effects, which can be significant depending on the applications. Second we would like to consider the statistical aspects of the EM failure process using Monto Carlo or other stochastic methods as EM is statistical in nature. Third, we would like to consider many other effects such as microstructure changes with feature size scaling, voids on non-cathode nodes, grain boundary effects as well as the barrier thickness/integrity impacts on void nucleation, incubation and growth phases.

Acknowledgment

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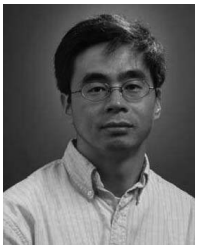
Zeyu Sun (Student Member, IEEE) received the B.S. degree in electronic and computer engineering from the Hong Kong University of Science and Technology in 2015. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA, USA. His current research interests include electromigration modeling and assessment and reliability-aware performance optimization.

Shuyuan Yu (Student Member, IEEE) received the B.S. and M.S. degrees in communication engineering from Fudan University, Shanghai, China, in 2015 and 2018, respectively. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA, USA. His current research interests include reliability-aware performance optimization and neural network.

Han Zhou (Student Member, IEEE) received the B.Eng. degree in electronic science and technology from Beijing Jiaotong University in 2013 and the M.S. degree in electronic science and technology from the Beijing Institute of Technology in 2016. She is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, University of California at Riverside, Riverside, CA, USA. She is focusing on VLSI reliability effect modeling, simulation, and optimization.

Yibo Liu (Student Member, IEEE) received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2017, and the M.S. degree in computer engineering from the University of California at Riverside, Riverside, CA, USA, in 2019, where he is currently pursuing the Ph.D. degree with the ECE Department. His current research interests include electromigration modeling reliability.



Sheldon X.-D. Tan (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Fudan University, Shanghai, China, in 1992 and 1995, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Iowa, Iowa City, in 1999. He is a Professor with the Department of Electrical Engineering, University of California at Riverside, Riverside, CA, USA, where he also is a Cooperative Faculty Member with the Department of Computer Science and Engineering. He was a Visiting Professor with Kyoto University as a JSPS Fellow from December 2017 to January 2018. He has published more than 280 technical papers and has coauthored six books. His research interests include VLSI reliability modeling, optimization and management at circuit and system levels, hardware security, thermal modeling, optimization and dynamic thermal management for many-core processors, parallel computing and adiabatic and Ising computing based on GPU and multicore systems.

Dr. Tan received the NSF CAREER Award in 2004. He also received the three Best Paper Awards from ICSICT'18, ASICON'17, ICCD'07, and DAC'09. He also received the Honorable Mention Best Paper Award from SMACD'18. He is currently serving as an Editor in Chief of *Integration* (Elsevier), the *VLSI Journal*, he also served as the Associate Editor for three journals: the IEEE TRANSACTIONS ON VLSI SYSTEMS, the *ACM Transactions on Design Automation of Electronic Systems*, and *Microelectronics Reliability* (Elseviers).