Layer Dependent Bit Error Variation in 3-D NAND Flash Under Ionizing Radiation

Preeti Kumari, Sijay Huang, Maryla Wasiolek, Khalid Hattar, and Biswajit Ray, *Senior Member, IEEE*

***Abstract*—In this paper we studied the total ionization dose (TID) effects on the multi-level-cell (MLC) 3-D NAND flash memory using Co-60 gamma radiation. We found a significant page to page bit error variation within a physical memory block of the irradiated memory chip. Our analysis showed that the origin of the bit error variation is the unique vertical layer dependent TID response of the 3-D NAND. We found that the memory pages located at the upper and lower layers of the 3-D stack show higher fails compared to the middle layer pages of a given memory block. We confirmed our findings by comparing radiation response of four different chips of the same specification. In addition, we compared the TID response of the MLC 3-D NAND with that of the 2-D NAND chip, which showed less page to page variation in bit error within a given memory block. We discuss the possible application of our findings for the radiation-tolerant smart memory controller design.**

***Index Terms*—3-D NAND flash, bit error, ionizing radiation, memory controller.**

I. Introduction

RADIATION tolerance is an important reliability concern for non-volatile memories (NVMs) in the space nuclear and defense applications. State of the art radiation hard NVMs have very limited capacity (in mega-bytes range), and very high cost making them impractical for several applications that require larger storage capacities. In this context, NAND flash memory is very attractive due to the associated high density (> 1 tera-bytes/sq. inch) relatively low cost (< $1 per giga byte), light weight and small form factor.

Since the traditional two-dimensional (2-D) NAND flash technology is approaching its fundamental scaling limits, the flash industry is going through a transition from planar to three-dimensional (3-D) architecture, which promises to extend the incredible growth of bit-density over the next decade [1]–[3]. Thus, 3-D NAND is one of the possible candidates for mass data storage in the future electronic applications. Radiation tolerance characteristics of 3-D NAND flash is a topic of great interest for both defense and space industry. Previously, it was demonstrated that the 2-D NAND flash technology has fundamental reliability concern for total ionization dose (TID) and single event effects (SEEs) [4]–[8]. Recent reports [9]–[11] show improved radiation response of 3-D NAND compared to its 2-D counterpart, making it an interesting option for radiation environments. However, the 3-D NAND technology is fundamentally different than the traditional 2-D NAND in terms of cell geometry (cylindrical gate-all-around cell vs. planar-gate cell), transistor channel material (poly-Si vs crystalline Si), and the array structure (vertical layer-by-layer vs planar cells). Hence, the radiation response characteristics of the standard 2-D NAND technology does not directly apply to 3-D NAND technology. This demands for re-evaluating all the carefully executed radiation-effects experiments on 3-D NAND that were previously performed on 2-D technology, before embracing it for nuclear, space and other mission-critical applications.

In order to understand the structural difference between the 3-D and 2-D NAND memory, it is important to recognize their underlying fabrication process [1], [12], [13]. Fabrication of 2-D NAND cells is similar to the standard Complementary-Metal-Oxide-Semiconductor (CMOS) process where the memory cells sit on the crystalline Si wafer. The 3-D NAND fabrication process is fundamentally different from the 2-D NAND fabrication. The 3-D NAND fabrication starts with deposition of alternate metal and oxide layers as illustrated with the schematic in Fig 1(a). Each metal layer forms the word line of the memory array connecting multiple memory cells in that layer. The channel of the memory cell is formed by creating a hole through the 3-D stack with reactive ion etching (RIE) process. The gate stack of the cells is then formed by sequentially depositing blocking oxide (oxide-nitride-oxide), charge trap layer or floating gate, and tunnel oxide along the sidewall of the cylindrical trench. Finally, a thin layer of poly-Si channel is deposited with hollow core filled with oxide. Hence the cell structure of 3-D NAND resembles vertical-channel (made of poly-Si) gate-all-around Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) (Fig 1(b)). The tapered shape of the cylindrical memory hole (as shown in Fig 1(a) results from the inefficient RIE at the bottom layers. Thus, memory cells at the bottom layers typically have smaller diameter than the top and middle layers.

Due to the unique nature of 3-D NAND fabrication process, the cell size and shape varies significantly across the different vertical layers [14]. The layer to layer variability of the 3-D NAND memory has been confirmed by recent studies in terms of its endurance and data retention characteristics [15], [16]. To

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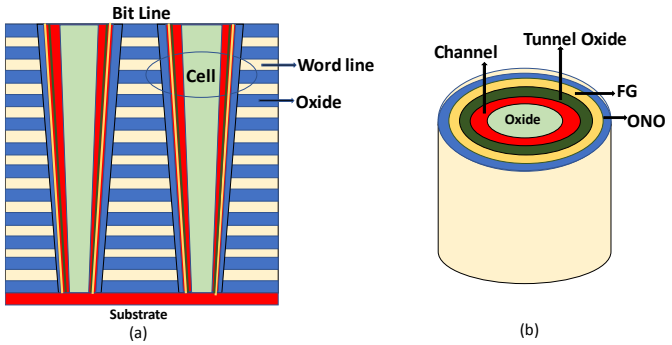

Fig. 1 (a) Vertical cross section of the 3-D stack consisting of alternate metal-oxide layers. (b) One single cell structure similar to gate-all around transistor.

our knowledge, however, no research has been published on the layer dependent radiation response of 3-D NAND memory. The purpose of this paper is to explore and quantify the layer dependent TID response of 3-D NAND memory in terms of radiation induced bit error ratio (BER). BER is defined as the number of corrupted bits divided by total number of bits. With this goal, we exposed commercial-off-the-shelf (COTS) 32-layer 3-D NAND MLC memory from Micron Technology to Co-60 gamma radiation and characterized the TID-induced BER at the different vertical layers of the chip. More details on the chip specifications, the experimental set-up and measurement procedure as well as the details of gamma irradiation conditions and the data collection method are discussed in Section II. We also provide possible implications of the results for smart memory controller design in Section III. Section IV concludes the paper.

II. Device and Experimental Details

A. Device details

We used COTS NAND flash memory chips from Micron Technology for evaluating the radiation response. The part number for the 3-D memory chips was MT29F256G08CBCBBWP-10: B which were 256 Gb MLC memory chips from Micron. Four different chips were used to improve statistics. Each 3-D memory chip contains 2192 logical blocks, where each block consists of 1024 logical pages of size 18,592 bytes (16,384 bytes of user data with 2208 bytes of error correction codes). The chip is fabricated using 3-D NAND technology with 32-vertical layers. The study included three 2-D NAND chips. The part number of the 2-D NAND chips that were used in the study was MT29F64G08CBABAWP: B TR, which were MLC chips of 64 Gb capacity. Each 2-D memory chip contains 2048 logical blocks of 256 pages, each containing 8000 bytes. The 2-D chips are fabricated using 20 nm technology. All the memory chips (3-D as well as 2-D) were in thin small outline package (TSOP).

Fig. 2(a) shows the typical block diagram of a NAND flash memory chip. The peripheral circuits in Fig. 2(a) consist of charge pump (for voltage amplification), data buffers, and sense amplifiers which are used during NAND array operations. The memory blocks are organized in multiple physical planes. For example, the 3-D NAND chip that we used in our analysis has four different planes each containing 548 blocks. Fig. 2(b) shows the arrangements of memory cells within a memory block. Each memory block consists of a fixed number of memory pages. The cells in each memory page are electrically connected through a metal word line (WL). WL acts as the control gate of memory cells which are essentially floating gate (FG) metal-oxide-semiconductor field effect transistor (MOSFET). Each column (or string) of cells in a block is connected to a different bit line (BL). Memory-read and program operations are performed at the page granularity, while erase is performed at the block granularity [17], [18]. Any flash cell that is set to a logic '0' by a program operation on a page can only be reset to a logic '1' by erasing the entire block. Both 2-D and 3-D NAND have similar circuit representation of memory block shown in Fig. 2(b). However, the individual cell structure for 2-D vs. 3-D NAND is very different as illustrated in Fig. 2(c) and 2(d). The cell structure of 2-D NAND memory (Fig. 2(c)) is similar to planar gate FG-MOSFET, while cells of 3-D NAND memory resemble vertical-channel gate-all-around MOSFET (Fig. 2(d)).

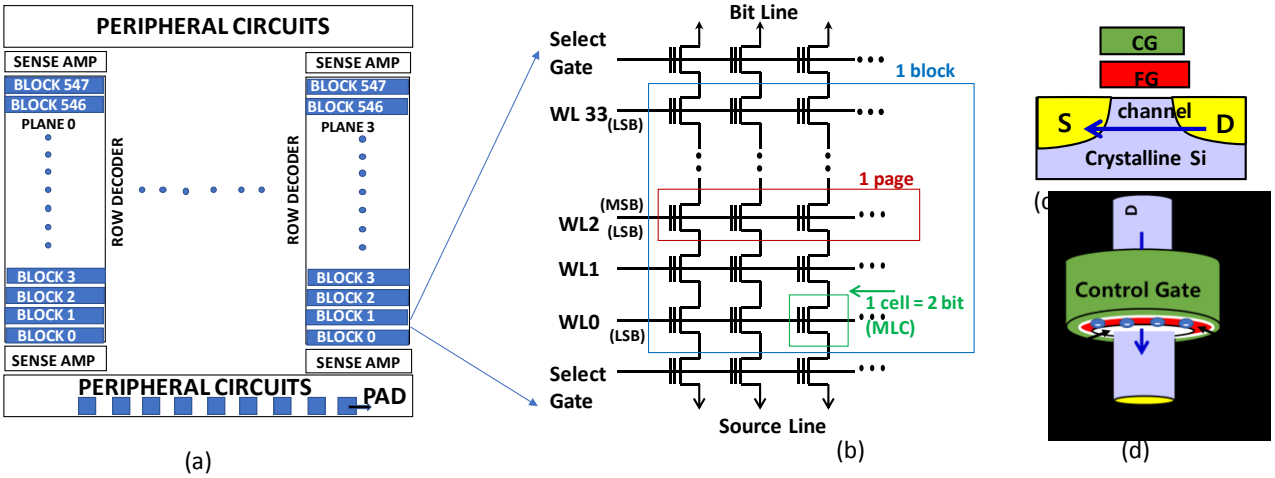

Fig. 2: (a) Schematic and organization of a flash memory chip. (b) Organization of a memory block in NAND flash chip. (c) Structure of 2-D NAND Flash memory (d) Structure of 3-D NAND Flash memory.

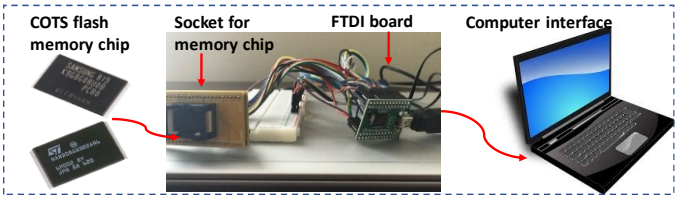

Fig. 3. Our measurement set-up to interface commercial off the shelf (COTS) flash memory chip with computer to measure radiation induced bit error.

B. Gamma ray irradiation

The flash memory chips were irradiated using Co-60 sources to evaluate their TID response. The irradiation was carried out at Sandia National Laboratories Gamma Irradiation Facility [19]. The chips received a total ionizing dose (TID) of 10 krad(Si) at a dose rate of 18.5 rad(Si)/s. We have chosen TID 10 krad(Si) in our experiment as it is the typical TID tolerance specification for short duration(~ 1 year) Low Earth Orbit (LEO) mission's electronic systems [20]. If not otherwise stated, all doses in the following are expressed as absorbed dose in Silicon. Gamma irradiation was performed on the packaged devices (TSOP) in unbiased condition, where all the pins of the chip were at floating condition. Unbiased or unpowered state is a common use condition for non-volatile memories which are designed to retain data without any external power. Hence the irradiation of these chips in an unbiased state represents an important test condition. In addition, the unbiased state irradiation ensures minimal damage to the peripheral circuitry (e.g., charge pump) of the chip, which allows us to explore radiation effects mainly on the floating-gate memory cells. The direction of gamma rays during irradiation was perpendicular to the flat surface of the chip. The entire unbiased chip in unlidded condition went through the gamma irradiation.

C. Measurement setup and procedure

To interface the raw NAND chip with the computer, we used a custom designed hardware board (Fig. 3). The board includes a socket to insert the NAND flash chip and an FT2232H mini module from Future Technology Devices International (FTDI) to interface the memory chip with computer through Universal Serial Bus (USB) connection. The FT2232H mini module enables USB to UART interface with high speed (480Mb/s). The hardware setup allowed us to access the raw memory bits without any error correction. The hardware setup was not exposed to gamma radiation. It was only used to write/read the memory chips that were irradiated. Before sending the chips for radiation exposure, we wrote a known random data pattern on four to six memory blocks in each chip. The same data pattern was used for all the chips. We read all the blocks immediately after writing data. We found very low BER (~ 0.00028%) in the memory just after writing data on them. A small number of bit errors were observed as the chips are of MLC configuration which has very low voltage margin between different memory states. We then exposed the NAND memory chips to gamma radiation. Finally, we read the data from the corresponding memory block and computed BER. There was a time delay of approximately one-week duration between the radiation exposure at the Sandia National Laboratories and the data read-out event at The University of Alabama in Huntsville. We would like to emphasize that a reference chip was programmed with the same data pattern in order to monitor the intrinsic failures due to the data retention effects. The irradiated chips showed orders of magnitude higher fails compared to the reference chip even though they were programmed at the same time, which confirms that the bit errors are due to radiation effects even though the read-out was performed after one week of exposure.

III. Experimental Results And Analysis

Data are read from the NAND flash chip byte by byte. We compare each bit, read from the chip after irradiation, with the original random data pattern to compute the BER. In the following section we present the radiation induced BER analysis to understand the layer-to-layer variability of 3-D NAND.

A. Pre & post irradiation BER

Here we present the BER data for a given memory block before and after the radiation exposure. A memory block of the 3-D NAND chip under test consists of 1024 logical pages. Fig. 4(a) shows the BER due to the absorbed dose on the 1024

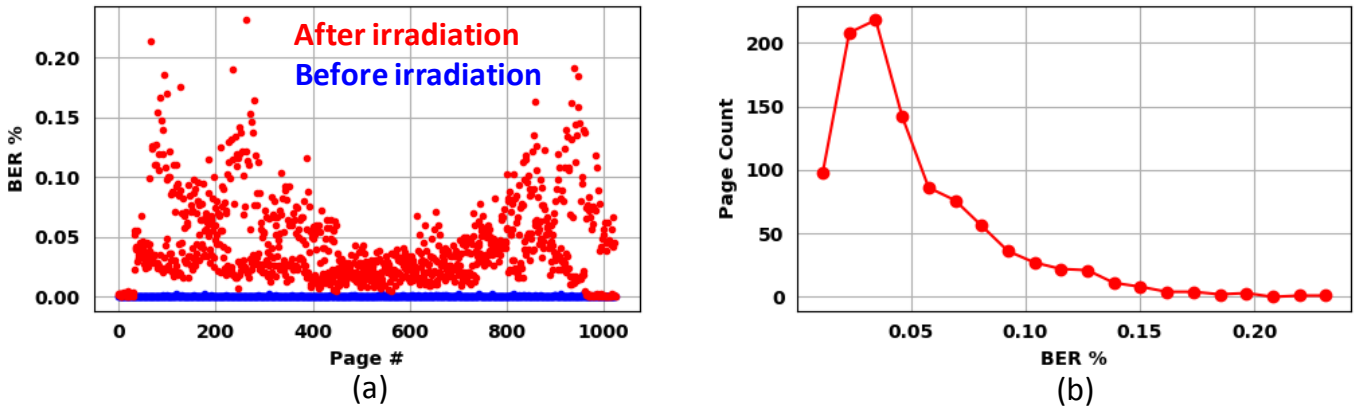

Fig. 4 (a) Scatter plot of BER before irradiation (Blue) and after irradiation with TID =10 krad(Si) (Red) (b) Histogram plot of the BER after irradiation (TID = 10 krad(Si)).

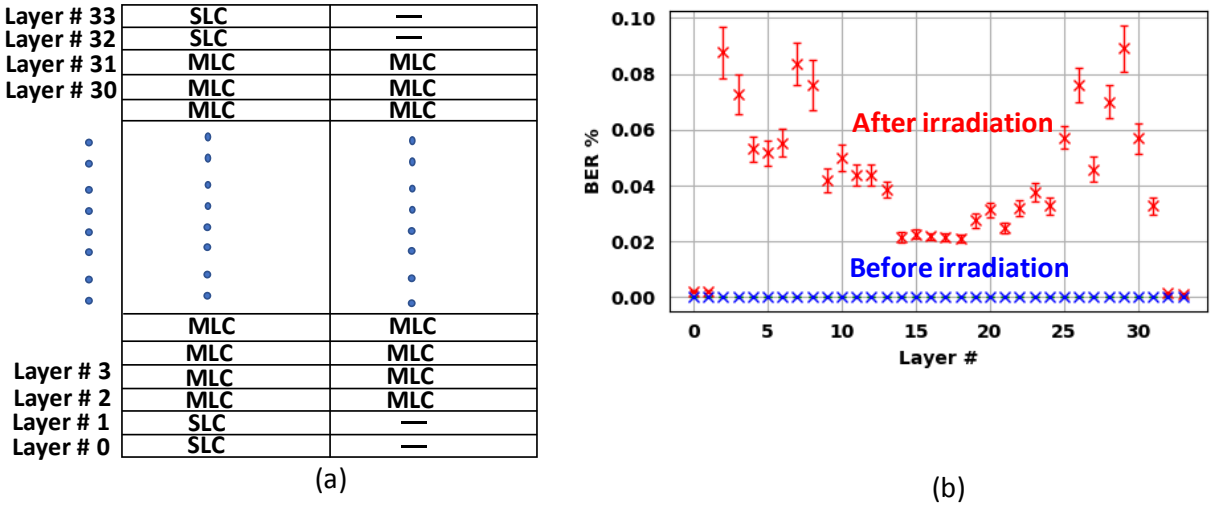

Fig. 5 (a) Organization of SLC and MLC pages in the different word lines in the 3-D NAND chip from Micron. (b) Word line or layer dependent BER for MLC 3-D NAND, before irradiation (Blue) and after irradiation with TID = 10 krad(Si) (Red).

logical memory pages of a given block. In Fig. 4(a), blue points are for the pre-irradiation data, red is for post-irradiation BER data (TID =10 krad(Si)). The BER is very low in all the pages before radiation exposure. The few errors observed before irradiation are inherent in high density MLC NAND due to very minimal voltage margins between the different programmed states. We observed that the inherent BER remains almost the same or slightly increases (over a few months of time) at room temperature. However, BER significantly increases on all the memory pages after radiation exposure. The average BER increased from 0.00028% (before irradiation), to 0.044% for TID = 10 krad(Si). Please note that the radiation-induced bit errors are not due to functionality loss of peripheral circuitry or any permanent failure of the memory cells. Once we erased the data and reprogrammed the memory block, the BER reduced to a negligible level, similar to pre-irradiation condition. Thus, we confirmed that the radiation induced errors are soft-errors typically caused by charge loss from the floating gate.

In addition to increased BER, we observed significant page to page BER variation on the post-irradiated chip. To illustrate the page to page BER variation, we constructed the histogram plot of the measured BER values on the 1024 pages as shown in Fig. 4(b). Each dot in Fig. 4(b) represents the height of the histogram which is obtained by counting the number of memory pages having BER values in a range given on the x-axis of the plot. The BER distribution shows a long upper tail which implies there are certain pages having significantly higher BER compared to most of the pages in a memory block. In the next section we examine the origin of such wide page to page BER variation.

B. Layer dependent TID response in 3-D NAND

The logical pages of a 3-D NAND memory block are distributed across the vertical layers of the 3-D structure. Ideally, each vertical layer should hold 32 logical pages if the pages are uniformly distributed across the 32 physical layers (total 1024 pages per block). However, according to the datasheet of the 3-D NAND memory (part # MT29F256G08CBCBBWP-10: B) the chip under test has non-uniform page distribution, especially on the edge layers (top two and bottom two layers) as illustrated in Fig. 5(a). Fig.5(a) shows the layer dependent page distribution for a specific sub-block structure (there are total 16 identical sub-blocks in a memory block) in the memory array. Note that there are total 34 physical layers in the 3-D stack, where the bottom as well as top two layers have non-shared memory pages, similar to single-level-cell (SLC) technology. In other words, the edge layer memory pages operate as SLC storage, while the remaining 30 layers operate as the MLC storage. Most likely, the manufacturer designed the edge layers to operate in single bit per cell (or SLC) type memory storage to improve the data reliability on the edge layers' memory pages [21].

Fig. 5(b) shows the BER on memory pages across different vertical layers before and after irradiation (10 krad(Si)). Each BER point in the plot represents the average value of the BER obtained from all the memory pages in a specific vertical layer of a given memory block. Before radiation exposure, the BER is very low in all the layers and does not show any layer dependent BER trend (blue symbols). The BER from the same memory block after receiving a gamma radiation dose of 10 krad(Si)is shown with red symbols. We found that BER significantly increased in all the layers after radiation exposure. Since the edge layers (top two and bottom two) operate in the SLC storage mode, their radiation tolerance is relatively higher and hence BER was least increased in those layers after irradiation. However, all the intermediate 30 layers operating in the MLC storage mode showed significantly higher BER after radiation exposure of 10 krad(Si). The most interesting and important observation in Fig. 5(b) is the unique "U" like shaped BER pattern for the intermediate 30 layers operating in the MLC storage. The "U" like shaped BER pattern implies that the MLC memory pages located near both edges of the 3-D stack are more vulnerable to ionizing radiation compared to pages located in the middle of the stack.

C. Analysis of chip-to-chip variation in TID response

We have performed the TID induced BER analysis for four different 3-D chips of the same specification. Fig. 6 summarizes

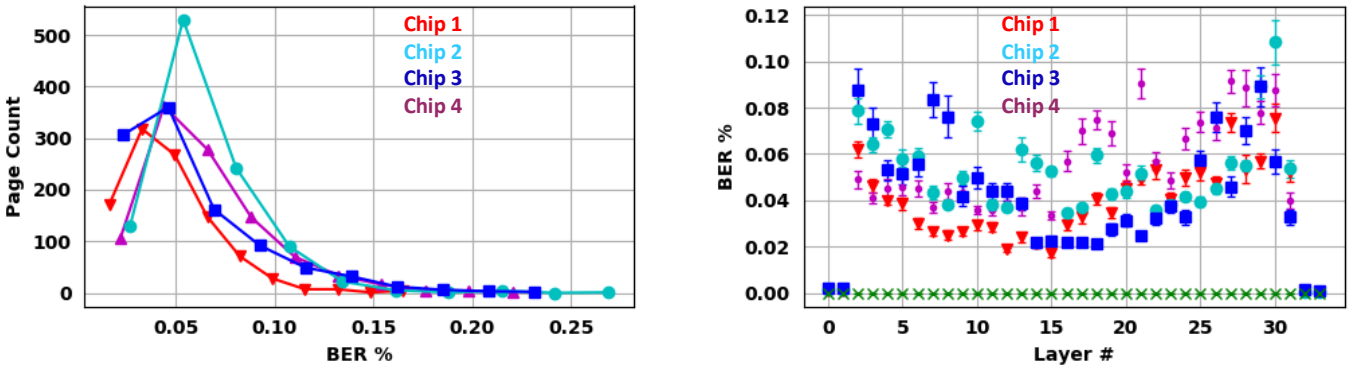

Fig. 6 (a) Histogram plot of the BER for four different MLC 3-D NAND chips exposed to gamma radiation at TID = 10 krad(Si) (b) Word line or layer dependent BER for four different MLC 3-D NAND chips, before irradiation (Green), after irradiation with TID = 10 krad(Si)) (Red, Cyan, Blue and Magenta).

the chip-to-chip variation of the TID response. We find that even though the average BER varies from chip-to-chip after gamma irradiation, the page to page BER variation within a given memory block remains high in all the four chips. As shown in Fig 6(a), all the four chips show long upper tail in the histogram plot of the BER distribution. Thus, we can conclude that long tail BER distribution is a unique feature of TID response in the 3-D NAND memory. Next, in Fig 6(b), we show the average BER values at each vertical layer for all the four memory chips. We found that majority of the chips follow the "U"- shaped BER dependence with the vertical layer number, which explains that the long tail distribution of the BER is due to the high BER values at the edge layers. In other words, the edge layer memory pages (excluding the SLC pages) are more vulnerable to TID exposure in 3-D NAND memory. Please note that the exact value of the BER may change based on directionality of the radiation exposure [22] and the type of ionizing radiation, however, the long tail BER distribution and the "U"- shaped BER dependency on vertical layers remain the unique feature of the TID response in the 3-D NAND technology.

The BER variation presented so far were obtained when the chips were exposed to TID of 10 krad(Si). To investigate if this effect persists at a higher TID level, three MLC 3-D NAND chips were exposed to TID of 20 krad(Si). Fig. 7 compares the

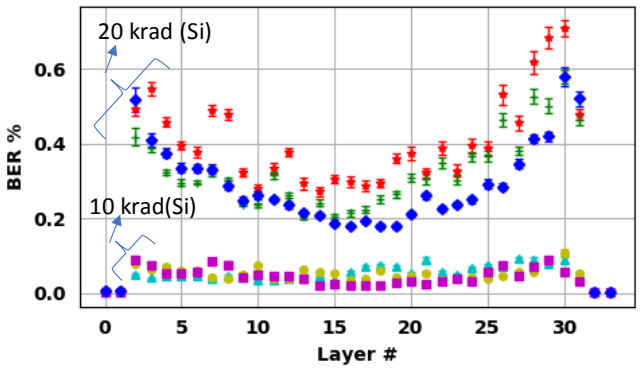

Fig. 7. Average bit error on different layers of the 3D NAND memory for 10 krad(Si) and 20 krad(Si) TID exposure. Three different chips (different symbols) were used for this evaluation.

layer dependent BER for TID values of 20 krad(Si) and 10 krad(Si). We find that BER increases in all the vertical layers with higher dose. The average BER after 20 krad(Si) exposure was nearly three times the BER after 10 krad(Si). More importantly, the "U"-shaped nature of the BER variation across different layer was preserved even after 20 krad(Si) of exposure.

D. Explanation for the layer dependent TID response

Since commercial memory chip manufacturers do not provide all the details of the chip structure and the underlying materials (such as the back end of the line (BEOL) metals), it is difficult to provide a comprehensive explanation for the observed layer dependent BER trend in 3-D NAND memory. In the following, we provide a plausible explanation for the layer dependent BER based on the dose enhancement effects[23]–[26] and the tapered structure[27] of the 3-D NAND array.

The tapered shape of the cylindrical memory hole (as shown in Fig 1(a)) is inherent in the 3-D NAND technology due to the RIE process, which is a key step in 3-D NAND fabrication[14], [28]–[30], [27]. The tapered shape naturally emerges due to the high aspect ratio of the cylindrical shaped memory hole making the RIE inefficient at the bottom layers. Thus, memory cells at the bottom layers typically have smaller diameter (D) than the top layers. The diameter difference (ΔD) depends on tapering angle (θ) and the height of the 3-D stack (H) as follows: $\Delta D \sim 2H \times \tan(\theta)$. The exact values for the tapering angle and the height of the 3-D stack are proprietary information and are not available in the public domain. Assuming typical values [27] of tapering angle ($\theta \sim 0.5^0$) and height of one layer ($\approx$ 80 nm), we can estimate the diameter difference $\Delta D \sim 45$ nm for 32-layer stack. Since the typical diameter of the memory hole is $\sim 80 - 90$ nm, the estimated diameter difference is quite significant and may result in roughly two-times smaller diameter in the bottom layer cells compared to the top or middle layer cells. Since smaller sized cell experience quicker charge loss, we expect roughly two times higher BER in the bottom layer compared to the middle layer cells, which is observed in the experimental data shown in Fig 6 and Fig 7.

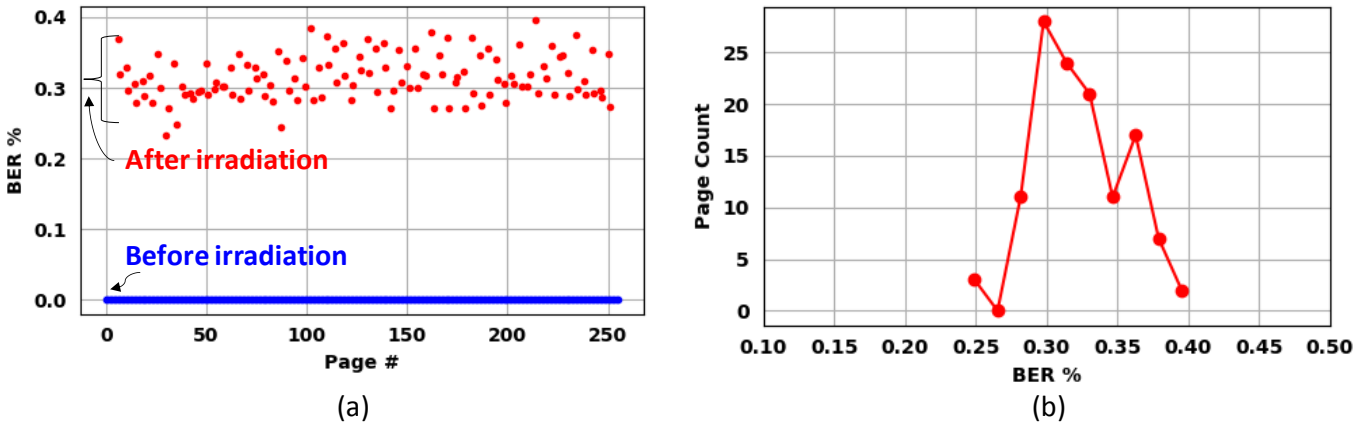

Fig. 8 (a) Word line or layer dependent BER for MLC 2-D NAND, before irradiation (Blue) and after exposure to gamma radiation at TID 10 krad(Si)(Red). (b) Histogram plot of the BER for MLC 2-D NAND exposed to gamma radiation at TID 10 krad(Si).

Our hypothesis for the higher BER in the top layers of the memory array is based on dose enhancement effect [23]–[26] due to the BEOL metals as recently explored by Gadlage et al. [22] in the context of NAND flash memory. Since the top layer cells are relatively closer to the BEOL metal layers, top layer cells are expected to experience higher dose enhancement effects compared to the middle or bottom layer cells and hence higher BER is observed on the top layer memory pages. Please note that several other factors such as different amount of charge storage at different layer cells during program operation, may also contribute to the observed layer dependent TID response and hence further investigation is necessary to completely understand the observed layer-dependent phenomena of the 3-D NAND memory technology.

E. Comparison of TID response in 3-D and 2-D NAND

To compare the TID response of 3-D NAND with that of 2-D NAND, we performed similar gamma radiation exposure experiments on Micron's 64 Gb 2-D MLC NAND chip. Fig. 8 summarizes the BER results from the 2-D NAND chip before and after TID exposure. The TID exposure results of 2-D NAND do not show any strong page to page BER variation (Fig. 8(a)). Unlike 3-D memory, we do not observe any long upper tail in the histogram plot of the BER distribution (Fig 8(b)). Since 2-D NAND memory cells are located on the same plane and have relatively uniform cell size, the page to page BER variation is minimal. Please note that while the BER values for 2-D NAND chip was found higher compared to the 3-D chip for the same total dose, the 2-D NAND cells are from 20 nm planar technology node which is fundamentally different compared to the 3-D NAND technology. The purpose of this comparison is to illustrate the fact that the significantly large page to page variation is a special property of the 3-D NAND which was relatively lower in case of 2-D NAND technology.

F. Implication of layer dependent BER for radiation-tolerant memory system design:

The layer dependent BER trend has significant implications for the design of radiation tolerant smart memory controller. The goal of any smart memory controller is to improve data reliability with least amount of resources, time and power [31], [32]. The layer dependence of the radiation induced BER observed for 3-D NAND can be utilized by the memory controller for improved data reliability in the following ways:

1) Data refresh: Memory controllers in solid state drives and other critical NVM systems periodically monitor the accumulated errors in the stored data and re-allocate data to a different physical location if accumulated errors exceed certain threshold. This feature is called data refresh. Our analysis here confirms that it is not necessary to monitor each page of a 3-D NAND memory block for TID tolerance. Based on the results shown in Fig. 4(a), it may be sufficient to monitor the worst-case pages located in the edge layers of 3-D stack to ensure data integrity in the other pages of that block. This will significantly reduce power consumption of the memory system.

2) Layer dependent data protection: Error correcting codes (ECC) are typically used by standard memory controller to recover data. The memory controller usually writes the ECC code word on the same page where data are stored. The length of the code word decides the number of correctable bits. Since the edge layers of the 3-D NAND are found more vulnerable to radiation exposure, controller may implement stronger ECC (or more ECC bits) for data stored in the edge layers while less ECC bits for middle layer pages. Since all NAND flash based storage system comes with ECC engine, no additional circuitry is needed to implement this idea. In this way, memory controller will ensure reliability of stored data in all the vertical layers.

IV. Conclusion

In summary, we conclude that the top and bottom layers cells of 3-D NAND flash are more vulnerable to TID compared to the middle layer cells. Due to the layer dependent TID response in the 3-D NAND, we observe a unique "U"-shaped BER variation for memory pages within the same physical memory block. In addition, the page level BER distribution of the 3-D chip, shows a long upper tail implying significantly high BER in certain memory pages. In comparison, the TID induced page to page BER variation is found minimal in case of 2-D NAND memory. Thus, we can conclude that long tail BER distribution is a unique feature of TID response in the 3-D NAND memory.

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