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Alloying conducting channels for reliable neuromorphic computing

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A memristor[1] has been proposed as an artificial synapse for emerging neuromorphic computing applications[2,3]. To train a neural network in memristor arrays, changes in weight values in the form of device conductance should be distinct and uniform[3]. An electrochemical metallization (ECM) memory[4,5], typically based on silicon (Si), has demonstrated a good analogue switching capability[6,7] owing to the high mobility of metal ions in the Si switching medium[8]. However, the large stochasticity of the ion movement results in switching variability. Here we demonstrate a Si memristor with alloyed conduction channels that shows a stable and controllable device operation, which enables the large-scale implementation of crossbar arrays. The conduction channel is formed by conventional silver (Ag) as a primary mobile metal alloyed with silicidable copper (Cu) that stabilizes switching. In an optimal alloying ratio, Cu effectively regulates the Ag movement, which contributes to a substantial improvement in the spatial/temporal switching uniformity, a stable data retention over a large conductance range and a substantially enhanced programmed symmetry in analogue conductance states. This alloyed memristor allows the fabrication of large-scale crossbar arrays that feature a high device yield and accurate analogue programming capability. Thus, our discovery of an alloyed memristor is a key step paving the way beyond von Neumann computing.

To operate large-scale memristor arrays, the device properties should meet a variety of requirements. Metal-oxide-based memristors recently demonstrated promising functionalities and applications in large-scale arrays, such as for signal processing and image classification tasks[9–13]. However, in most of these demonstrations, an additional transistor was required to serially connect to each memristor, which serves as the selecting device, and to regulate the analogue switching properties[12,14,15]. Although a good analogue weight update can be modulated by the gate voltage of the selecting transistor[12], the addition of a transistor not only limits the scalability and stackability of the memristors, but also substantially increases the design complexity and peripheral overheads. Without a transistor, the performance of the memristor array becomes more vulnerable to high switching variations and loses grasp of fine-grained conductance tunability[16]. However, ECM memory[17,18] also demonstrates good analogue switching properties towards a more linear and/or symmetric weight update even without transistors[6], in which Ag is typically employed as an active metal owing to its high mobility[5,19]. However, such mobility causes variation in the weight and reduces long-term reliability, particularly in low conductance states because of weakly formed conduction channels[20]. Even though fine analogue states can be modulated from these devices, they cannot be preserved for computing applications. Therefore, a new memristor that can provide good analogue tunability while maintaining good stability in every level of conductance is still highly desired.

Here we introduce an ultimate weight control technique that can substantially improve switching uniformity while retaining multiple tunable weights in the memristors across a wide range of conductance levels. We applied a metallurgical strategy in designing ECM devices in which we tailored the conduction channels formed in a switching medium. We alloyed binary metals by carefully considering the thermodynamic stability of mixing of metal–metal as well as metal–switching medium. We chose Si as the switching medium as its interactions with various metals are well understood. We discovered that conduction channels formed by Ag alloyed with Cu in a Si medium tremendously enhanced the memristive performance and demonstrated several unique properties compared with those of existing memristors, which include: (1) a uniform gradual switching, (2) reliable retention at multilevel conductance states and (3) enhanced symmetry and/or linearity of analogue conductance updates. With these performances, we fabricated 32×32 transistor-less alloyed memristor crossbar arrays, achieved a 100% yield and demonstrated reliable operation and programming. The substantially enhanced data retention also enabled us to perform inference tasks, and thus pave the way for efficient analogue computing with transistor-less memristor arrays.

We first attempted to understand the switching behaviours of our Si ECM memory that depend on the active metals. A device layer includes a 6-nm-thick amorphous Si (a-Si) film on a p-type Si substrate (0.01 Ω cm) with various active metals, which included Ag, Cu, Ni, Cr and Ti (see Methods for details about the device fabrication). Among the active electrodes, depending on their reactivity with Si, a noticeable difference in their resistive switching performances was observed under a d.c. operation mode, as shown in Fig. 1a. Ag devices exhibited a reversible resistive switching—the device conductance increased under a positive biased condition (that is, set) and vice

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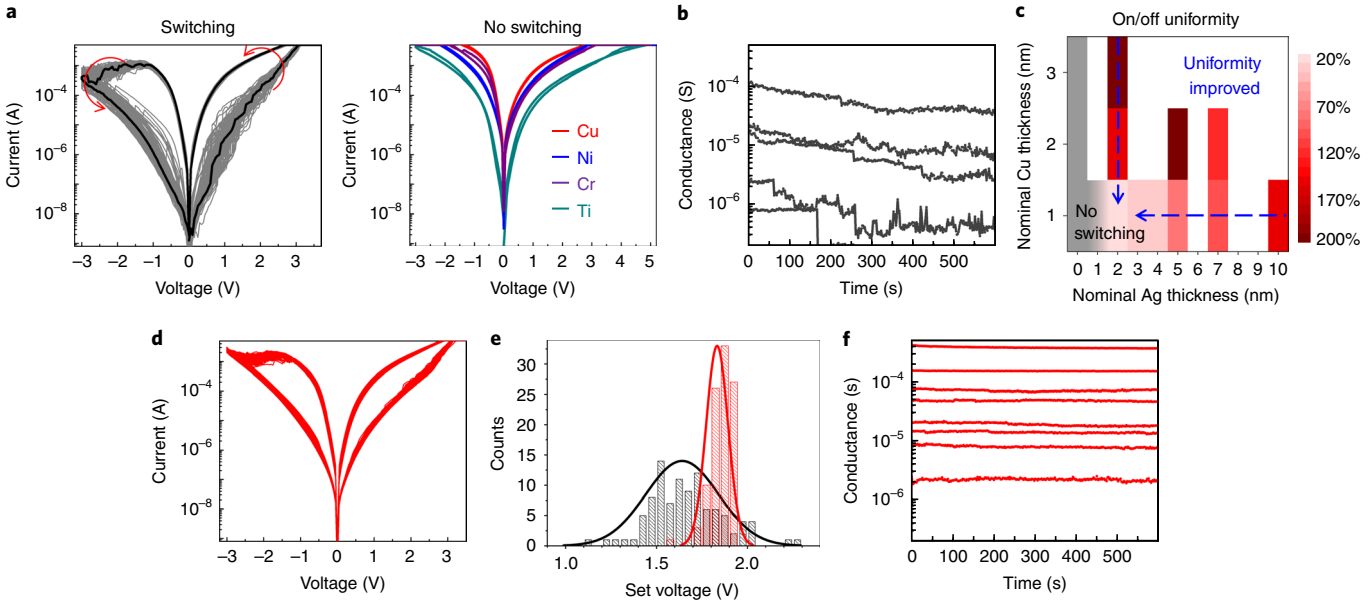

Fig. 1 | The d.c. switching performance of a Si memristor with a Ag–Cu alloy. a, Typical current–voltage curves of Ag (left) and silicidable metals (Cu, Ni, Ti and Cr) (right) after the forming process. **b**, Retention properties of Ag devices (read at 0.5 V) with multiconductance levels. **c**, Effect of the Ag–Cu thickness ratio on alloying during the formation on the d.c. switching uniformity—normalized on/off uniformity during 100 cycles. **d**, Uniform switching of the Ag–Cu device during 100 cycles. The nominal thicknesses of Ag and Cu are 2 and 1 nm, respectively. **e**, Histogram for the set voltage distribution of the Ag device (black) and the Ag–Cu device (red) shown in **a** and **d**. **f**, Improved retention properties of Ag–Cu devices (read at 0.5 V) with various compliance currents.

versa under a negative bias condition (that is, reset). However, irreversible conductance changes were observed for Cu, Ni, Ti and Cr devices after the forming process. These metal-dependent switching behaviours are relevant to previous studies on Si ECM memory[21–24] and can be elucidated by analysing their phase diagram with Si (Supplementary Fig. 1). As shown in the phase diagram, Ag is thermodynamically unstable in the Si, which implies that it can be electrochemically mobile and results in a resistive switching behaviour. However, Cu, Ni, Ti and Cr interact strongly with Si, which promotes the formation of a thermodynamically stable interface between the conduction channel and Si (related with silicides), which can cause irreversible switching. Although the thermodynamic instability of Ag to Si allows resistive switching, it also causes a large switching variation as well as poor data retention. The set voltage and on/off ratio of the corresponding 100 d.c. switching of the Ag device exhibit 16.4 and 97.6% temporal variations, respectively (Supplementary Fig. 2a,b). This device also exhibits a high spatial variation for different fabrication batches (Supplementary Fig. 2c,d). In addition, conductance levels of the device decay substantially in every conductance level, as shown in Fig. 1b.

Enhancing the interactivity of active metals to the switching medium may alleviate issues in non-uniform switching and short data retention. However, selecting active metals that are strongly reactive to the switching medium induces electrochemically irreversible conduction channels. These conflicting results motivated us to design binary Ag alloys with silicidable metals to obtain resistive switching with an enhanced uniformity and data retention. Thus, we considered the following design rules. First, the silicidable metals also must be thermodynamically stable to Ag to enhance the stability of Ag in Si. Second, the diffusivity of the silicidable metals, relevant to drift mobility of metal cations[25], must be similar or higher than that of Ag so that they can migrate into Si simultaneously or prior to Ag migration to form the backbones of Ag conduction channels. Third, the amount of the silicidable metals must be low enough to preserve dominant Ag switching characteristics. To search for the best alloying elements, we referred to the phase diagrams of silicidable metals with Ag (Supplementary Fig. 3) and metal diffusivity in Si (Supplementary Fig. 4). We decided to use Cu as the complementary alloying element for the following reasons: (1) Cu diffusivity is higher than that of Ag (ref. [26]), which thus allows backbone formation (Supplementary Fig. 4), and (2) Cu is partially miscible with Ag, whereas Ni and Cr are fully immiscible, and this stabilizes Ag in Si as a bridge (Supplementary Fig. 3). To verify our hypothesis about the Ag–Cu alloying conduction channel formation, we performed a density functional theory calculation of the interfacial energy between Si and Ag–Cu to evaluate the conduction channel stability and performed a kinetic Monte Carlo simulation to estimate the switching dynamics based on the Ag–Cu alloy (Supplementary Note 1, Supplementary Figs. 5–7 and Supplementary Video 1). These simulation results suggest that alloying Ag with Cu stabilizes the conductance channel, but Ag can still diffuse in and out on set and reset. The optimal Ag–Cu ratio was determined through an evaluation of the d.c. switching performance according to various Ag–Cu mixing ratios by a nominal thickness control of Ag and Cu during evaporation (see Fig. 1c and Extended Data Figs. 1–3 for more details). As shown in Fig. 1d, a noticeable enhancement in d.c. switching uniformity was achieved for Ag–Cu devices compared with pure Ag devices (Fig. 1a). The dramatic change in the set voltage temporal variation from 16.4 to 3.3% with an enhanced spatial uniformity was statistically measured (Fig. 1e and Supplementary Fig. 8), although the forming voltage was nearly unchanged (Supplementary Fig. 9). More importantly, a substantial improvement in the data retention was recorded from the low to high conductance states for Ag–Cu devices, as shown in Fig. 1f (see Supplementary Fig. 10 for details of the retention properties with elevated temperatures and longer evaluation times). Furthermore, uniform switching properties with a stable data retention were weakly dependent on the ambient moisture level (Supplementary Fig. 11), which has substantially affected switching characteristics[27,28]. Note that alloying Ag with silicidable metals does not always guarantee an improved memristive performance as it must follow the above-listed rules. For examples, Ag–Ti

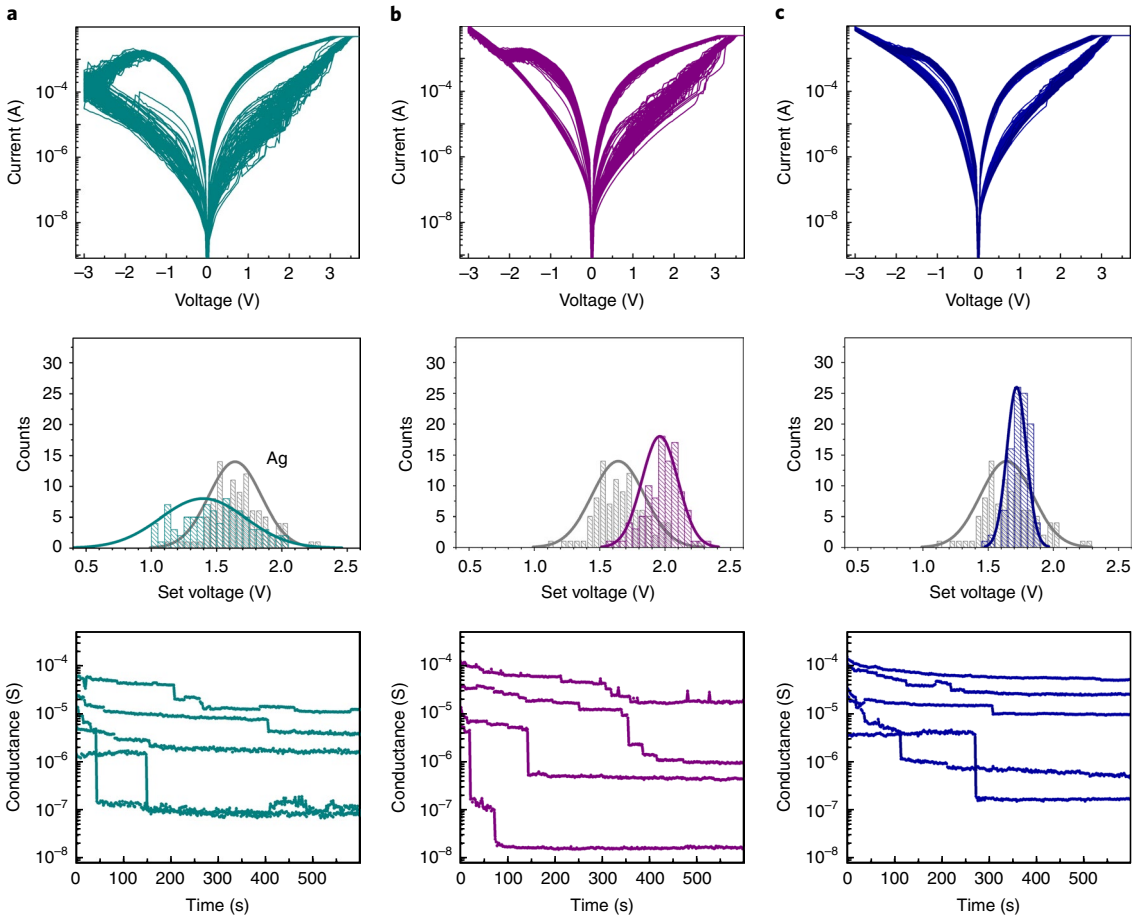

Fig. 2 | Kinetically and thermodynamically limited alloying effect on d.c. switching performance. a, Ag–Ti. **b**, Ag–Cr. **c**, Ag–Ni. 100 switching curves (top), set voltage histogram (middle) and retention properties with various compliance currents (bottom). The nominal thicknesses of Ag and the alloying element are 2 and 1 nm, respectively.

devices only satisfy the rule of having miscibility with Ag but has a lower diffusivity than Ag in Si (Supplementary Fig. 4). Its low diffusivity may not allow backbone formation before Ag has migrated, although Ti forms stable compounds with Si. Thus, as shown in Fig. 2a, Ag–Ti devices show a non-uniform d.c. switching behaviour and poor data retention, similar to Ag devices. However, Ag–Cr and Ag–Ni devices have a higher diffusivity than Ag (Supplementary Fig. 4), but are not miscible with Ag. Thus, Ag–Cr and Ag–Ni show an improved d.c. switching uniformity compared to Ag devices owing to the backbone formation (Fig. 2b,c). However, a long-term stability of the conductance levels was not found with the Ag–Cr and Ag–Ni devices owing to their immiscibility with Ag. Throughout these design rules, we discovered that a Ag–Cu alloying is desirable to drive a uniform switching and stable multilevel data retention of a Si memristor.

The much-improved multilevel switching performance can be of great benefit to analogue switching properties of our memristors. The analogue switching properties of the Ag–Cu alloy and pure Ag devices were evaluated by applying 50 repetitions of 50 ns of positive voltage pulses for potentiation followed by 50 repetitions of 50 ns of negative voltage pulses for depression. As shown in Fig. 3a,b, the conductance update in the Ag–Cu alloy devices is more gradual and linear compared with those in the Ag devices. To quantify such behaviour, we obtained temporal and spatial statistic values of the asymmetric non-linearity factor (ANL) for the Ag–Cu alloy and Ag devices (see Methods for a detailed experimental set-up for the analogue measurement). As shown in Fig. 3c, the average ANL of Ag–Cu alloy devices was 0.30 (s.d. = 0.06), whereas that of Ag is 0.59 (s.d. = 0.14). We speculate that such a non-linear and asymmetric analogue update with a sudden drop of the conductance in Ag devices originates from a thermodynamically unfavourable accommodation of Ag into Si, which causes a stochastic dissolution of the conduction channel. However, the stabilized interaction of conduction channels to Si by alloying leads to a more reliable and less abrupt conductance update. In addition, Ag–Cu devices exhibit a uniform analogue switching compared with that of Ag devices, as shown in Fig. 3c, which shows the normalized probability density of ANL and conductance (G) contrast, deduced from Supplementary Fig. 12. As presented in Fig. 3d, the improvement of conductance update in Ag–Cu alloy devices was tested for endurance through 3,000 pulse repetitions of 50 levels up-and-down sweep. Supplementary Fig. 13 shows the result of an extended endurance test of the Ag–Cu alloyed device. To characterize the nanosecond switching, the change in conductance as a function of pulse amplitude and duration was measured (Supplementary Fig. 14). We also tested 512 levels of conductance (Supplementary Fig. 15). The improved linear and symmetric analogue conductance update with resolvable conductance levels can substantially promote the programmability of a memristor in storing and training neural networks in large-scale array implementations, even without transistors.

To demonstrate the computing capability of our alloyed ECM memristors, 32 × 32 transistor-less arrays of Ag–Cu devices were fabricated as shown in Fig. 4a–c. The fabrication process was designed to optimize the use of Si bottom electrodes (Methods,

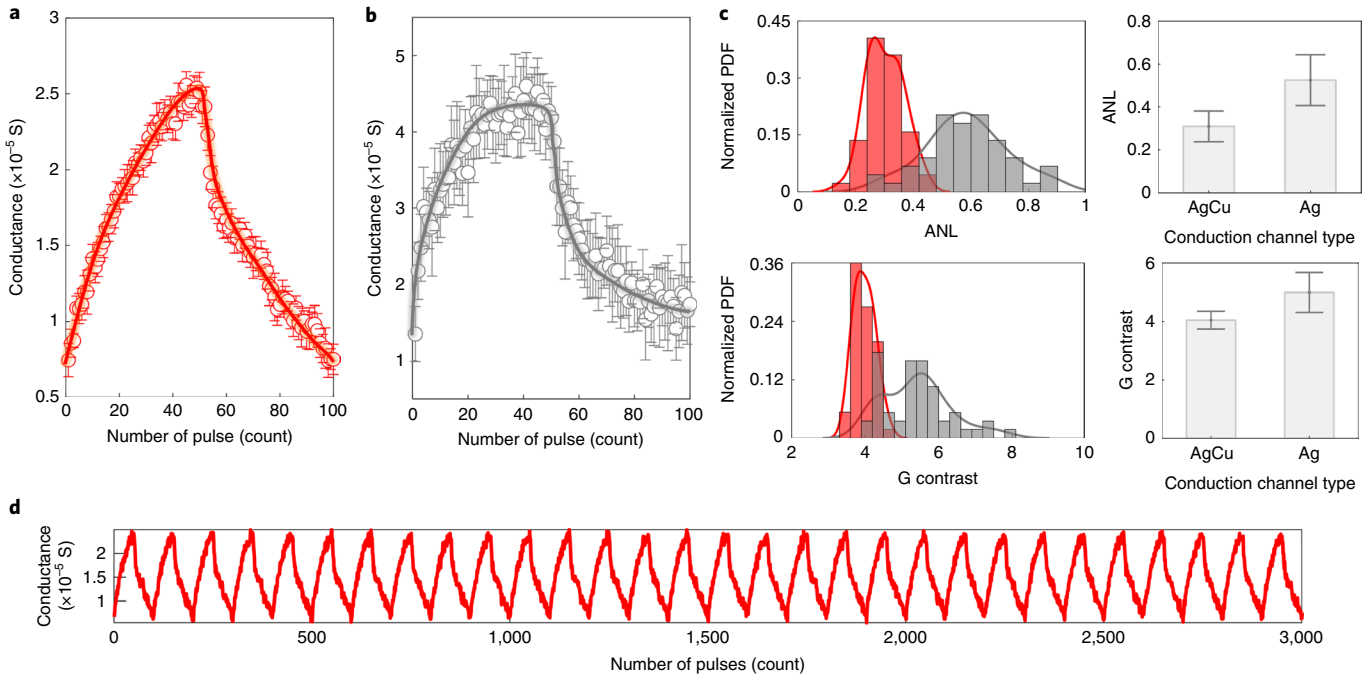

Fig. 3 | Alloy effect on analogue nanosecond switching behaviours of Si memristors. a,**b**, Average and s.d. of 50P/50D ten-cycle conductance updates under the same pulse condition in the Ag–Cu alloy (**a**) and pure Ag (**b**) (pulse conditions: potentiation (P) of 50 ns, 4.8 V and $n = 50$, depression (D) of 50 ns, -2.9 V, $n = 50$ and V_{read} of 1 V, 1 ms. **c**, Normalized probability of density function (PDF) of the ANL and G contrast from ten devices (50P/50D, five cycles each) for the Ag–Cu alloy (red) and pure Ag (grey). ANL = $(G_P(N/2) - G_D(N/2))/(G_{max} - G_{min})$, where G_{max}, G_{min}, $G_P(N/2)$ and $G_D(N/2)$ represent the conductance maximum, conductance minimum, median value of potentiation and medium value of depression, respectively. G contrast = G_{max}/G_{min}. **d**, Endurance test of a Si memristor based on the Ag–Cu alloy conduction channel. 50P/50D 30-cycle conductance programming was performed. Pulse condition for the endurance test: potentiation of 50 ns, 5 V and $n = 50$, depression of 50 ns, −3 V and $n = 50$ and V_{read} of 1 V, 1 ms.

Supplementary Note 2 and Extended Data Fig. 4). To study the alloying effects in the crossbar arrays, we also fabricated arrays with Ag and Ag–Ni devices. All the electrical operations of the array, which included electroforming, programming and inferences, were performed using a customized measurement system (Methods). The conductance ranges chosen for the programming were between 0 and 15 μS (Supplementary Fig. 16), in which ranges a poor retention can be detected. To demonstrate the weight storing capability, a 256-level greyscale image was programmed into the Ag–Cu, Ag and Ag–Ni arrays, as shown in Fig. 4d. All the arrays showed a 100% device yield and the visualized evolution of weight values clearly showed that the Ag–Cu alloy array maintained the programmed image owing to the significantly improved data retention. However, the contrast and integrity of the images programmed in the Ag–Ni and Ag arrays degraded drastically, almost losing all the stored information. These results demonstrate the effectiveness of the alloy strategy in enhancing the long-term stability of ECM memristors. As a result, array operations at lower conductance ranges become possible, which can help reduce the programming power (Supplementary Note 3 and Supplementary Fig. 17) and mitigate the sneak path and line resistance issues (Supplementary Note 4 and Supplementary Figs. 18–21).

To verify the functional operation of Ag–Cu transistor-less arrays, we programmed convolutional kernels into them and performed image processing tasks. During the convolutional process, a kernel (with a small matrix of weights) was applied to each pixel and its local neighbours of an image and produces output pixels from the weighted sum operation between the kernel weights and the input pixel values. Owing to the improved data retention provided by the Ag–Cu memristor, faithful image processing based on convolutional kernels were demonstrated, as shown in Fig. 4e. Four image kernels (sharpen, box blur, vertical and horizontal edge detection) were programmed into four columns of the array and processed in parallel (Methods and Extended Data Fig. 5). Two memristors in the same output column were used as a differential pair to implement negative weights and received either positive- or negative-valued input pixels (1 × 18 pixels in total for each input vector). The successful image processing using the Ag–Cu memristor arrays confirms the effectiveness of our alloy method for computing applications. To host more-complex tasks, large array sizes may be required. Scaling up the array dimension can also provide a quadratic increase in the parallelism of multiply-accumulate operations. However, further scaling of the array dimension requires optimization of the array design (Supplementary Note 4) to reduce line resistances and overcome more severe sneak-path issues in large-scale arrays (for example, integrating selector devices). The analogue tuning accuracy should also be carefully evaluated because the programming voltage may be disturbed by different weight patterns and increasing line resistances in large arrays.

In the mission to find the ideal device for neuromorphic computing, we propose that alloying the conduction channels in ECM devices will fundamentally solve the 'tunability–stability dilemma' between robust weight tuning and long-term stability. The effective engineering of interactivity and migration of alloying elements in conducting channels offers a great degree of freedom to tailor the electrical performance of the devices. This enabled us to build large-scale transistor-less crossbar arrays that demonstrated faithful operations in storing and inferencing neural network weights. We believe our alloy design rule for reliable memristor performances can be expanded to other material systems to optimize the conduction channels and switching dynamics for a better performance in neuromorphic computing applications.

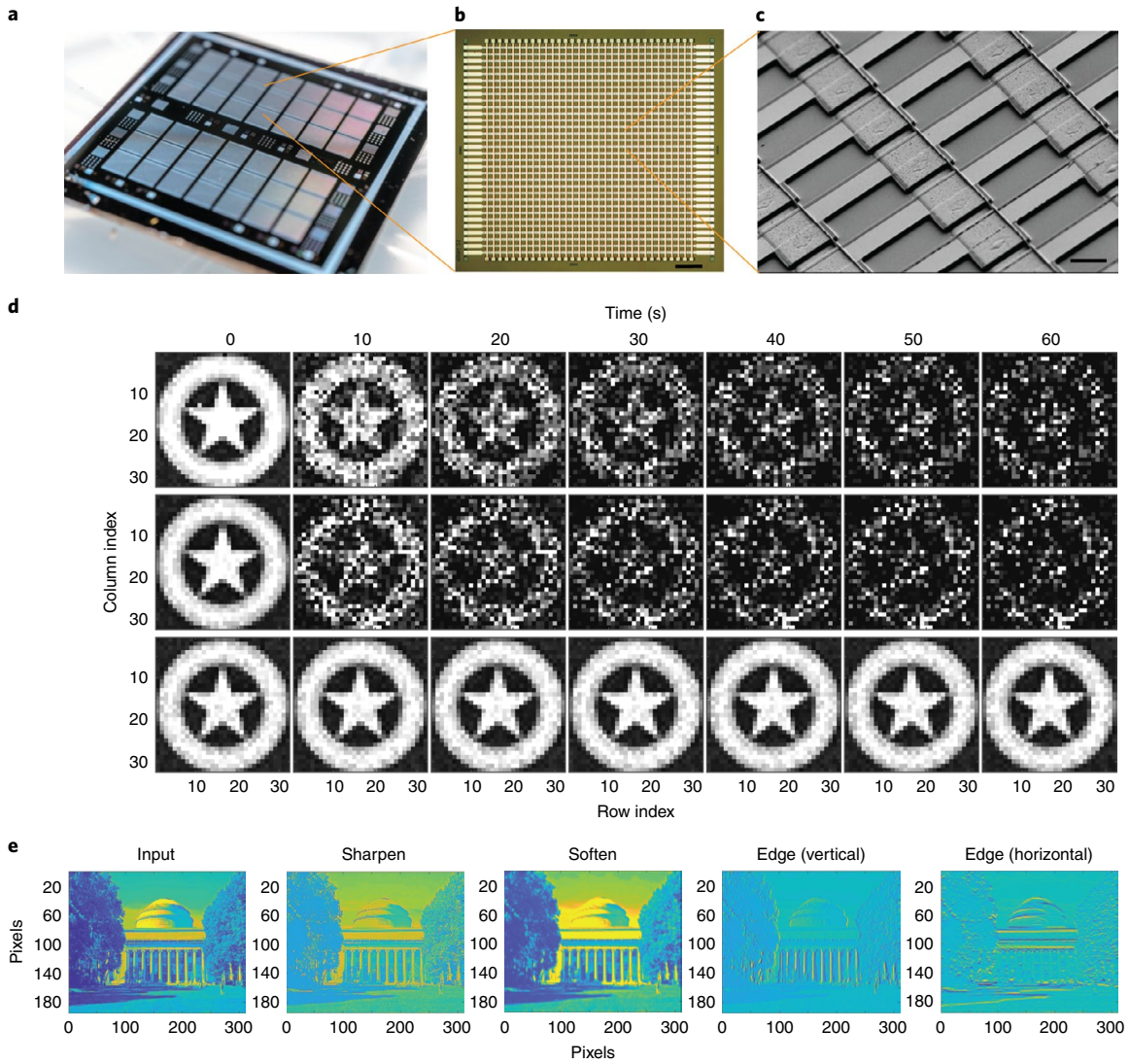

Fig. 4 | 32 × 32 transistor-less Si memristor arrays with Ag and alloy active electrodes. a, Image of the Ag–Cu alloy memristor chip. **b**, Optical micrograph of one 32 × 32 array. Scale bar, 240 μm. **c**, SEM image of part of the array, showing the crossbar structure. Scale bar, 15 μm. **d**, Image programming in Ag (top), Ag–Ni (middle) and Ag–Cu (bottom) arrays and their data retention tests. **e**, Convolutional kernel processing in the Ag–Cu array, showing the capability of using the Ag–Cu array for computing.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41565-020-0694-5.

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Methods

Trench-type Si memristor fabrication. A 6-nm-thick intrinsic a-Si film was deposited on a p-type (100)-oriented Si wafer (0.01 Ω cm, boron doping concentration of ~10^{19} cm^{-3}) by plasma-enhanced chemical vapour deposition (PECVD) at 200 °C and a PECVD SiO_2/SiN_x isolation layer (120 nm/20 nm) was formed at 300 °C. After through-hole patterning in the isolation layer (25–800 μm²), 20-nm-thick active metals were deposited into the hole to form contact with the a-Si and a Cr/Au layer (20 nm/100 nm) was formed for the passivation of the active metals. An Au/p-Si ohmic contact was formed as a counter electrode of the ECM memory. Cr (refs. [29,30]) and SiN_x (refs. [31–33]) were selected to suppress moisture penetration into the Si switching medium, and thereby enhance the device reliability against ambient changes.

Ag alloy deposition. Step-by-step evaporation was conducted for the Ag alloy deposition. After Ag evaporation, the alloying metal was evaporated (Extended Data Figs. 1 and 2). The Ag alloying ratio in the switching medium was modulated by the nominal thickness of the metals measured by a quartz crystal microbalance.

Si memristor crossbar array fabrication. A 150-mm (100)-oriented silicon-on-insulator wafer was used as a substrate. After the initial wafer cleaning, a stack of a 500-nm-thick heavily doped p-type Si layer (0.001 Ω cm) and a 200-nm-thick p-type Si layer (0.01 Ω cm) was homoepitaxially grown on a silicon-on-insulator wafer at 940 °C by ultrahigh vacuum chemical vapour deposition, followed by the deposition of a 6-nm-thick intrinsic a-Si thin film using PECVD. Photolithography and dry etching were used to pattern and isolate the Si bitlines from each other. Additional Cr/Au layers (1 nm/100 nm) were patterned and deposited on the top of the bitlines using photolithography and electron-beam evaporation to reduce the wire resistance and serve as input/output pads for measurement, as shown in Extended Data Fig. 4. An SiO_2/SiN_x layer (120 nm/20 nm) was then deposited by PECVD to cover the entire wafer as the passivation layer to the bitlines. After that, the active device area and input/output contact pads for the bitlines were patterned by photolithography etch through the combination of reactive ion etching and wet etching based on a buffered oxide solution to selectively remove the capping layer. The Ag alloy layer (20 nm) and Cr/Au capping layer (20 nm/50 nm) were deposited to cover the active area as the active top electrodes to the memristor. The fabrication was concluded by the patterning and deposition of the wordline by the tilted sputtering of Au.

Device d.c. measurements. Quasi-static d.c. current–voltage measurements and room-temperature state-retention measurements were executed with a B1500A semiconductor device parameter analyser with a B1517A high-resolution source measure unit. Si memristors were tested with bidirectional current–voltage sweep measurements with a compliance current during the forming and set process.

Ultrafast pulse measurement. To perform an ultrafast (nanoscale) analogue switching measurement, an oscilloscope (DSOX3024T, Keysight), pulse generator unit (PGU 33600A, Keysight) and transimpedance amplifier (DHPCA-100, Edmund 59–179) were used. A sequence of programming pulses for potentiation and depression in weight update was applied with identical amplitude but opposite polarity. Read pulses were sent to our memristive devices after each programming pulse to monitor the change in conductance. A current from the read pulse was integrated and averaged for 1 ms to secure the stabilized conductance values. To avoid wave reflections in the radio-frequency regime, the impedance value of the oscilloscope was set to 50 Ω and the load impedance of the pulse generator unit was set to infinite.

Array measurement. A customized board-level peripheral system with a parallel accessing and programming capability was used to perform the array measurement. The detail of the system is given in a previous publication[34]. The memristor arrays were accessed through a 32 × 32 probe card connected to the peripheral system. A 1/2 voltage biasing scheme was employed for the selective programming and to mitigate the sneak-path issues (selected rows were biased at 1/2 of the operating voltage, and selected columns were biased at −1/2 of the operating voltages, whereas all the unselected rows and columns were grounded). In the meantime, the ground scheme (all column outputs were virtually grounded by the transimpedance amplifiers) was used for inference to suppress the sneak current during computing. The detailed analysis of array operations in our passive Ag–Cu memristor array is given in Supplementary Note 4. The fabricated array requires an initial electroforming process for each device. The forming process was done in series by applying a train of ramping voltage pulses to the device until its conductance exceeded the 1 μS threshold. The formed device was subsequently reset to its off state after forming. The forming voltages (chosen between 4 and 8 V) were small enough to not encounter problems of unselected devices being set at 1/2 voltages. After electroforming, every device in the array was cycled between 5 and 20 μS at least 5 times before applications.

Image programming and retention test. Greyscale images were programmed into different alloy arrays using a closed-loop algorithm. The 256-scale pixel values were linearly mapped to conductance values between the maximum and minimum conductance defined for each task. The conductance tuning of pixels and devices were done in parallel inside each column for fast programming. The retention test was carried out by repeatedly monitoring the device conductance at an interval of 10 s. Both the raw conductance value and the reconstructed image based on 256-scale pixel values were used to compare between different alloy memristors. The greyscale pixel values were reversely and linearly mapped back from the conductance values.

Convolutional kernel operation. Four convolutional kernels were selected as a proof-of-concept demonstration of Ag–Cu alloy memristor arrays for reliable inference applications. Each kernel had 3 × 3 pixels and two memristors were used to represent both positive and negative weight values. The 3 × 3 × 2 memristors were mapped into a 18 × 1 vector and programmed into one column of the array. The 3 × 3 input pixels were applied accordingly to the input rows, with both positive- and negative-valued pixel amplitude for the differential memristor pair. After programming the kernels, 3 × 3 input matrices from a 310 × 194 pixel image were fed to the array in series for iterative convolutional kernel operations. The column outputs from each cycle were converted into voltage amplitude through a transimpedance amplifier, read out by analog-to-digital converters and recorded as one pixel in the filtered images.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

H.Y. and J.K. conceived this work and J.K. supervised the team. H.Y., P.L., C.C. and J.K. designed the experiments and prepared the manuscript. H.Y., P.L., C.C., S.H.T., Y.P. and D.L. performed the device fabrication. H.Y. and C.C. conducted the d.c. switching measurements. C.C., P.L., S.K. and Y.P. performed the pulse-switching measurements. P.L. performed the array measurements. H.Y., C.C., F.X., B.G., H.W., H.Q. and Y.N. performed and analysed the ab initio calculations and kinetic Monte Carlo simulations. All the authors discussed and contributed to the discussion and analysis of the results regarding the manuscript at all stages.

Competing interests

The authors declare no competing interests.

Additional information

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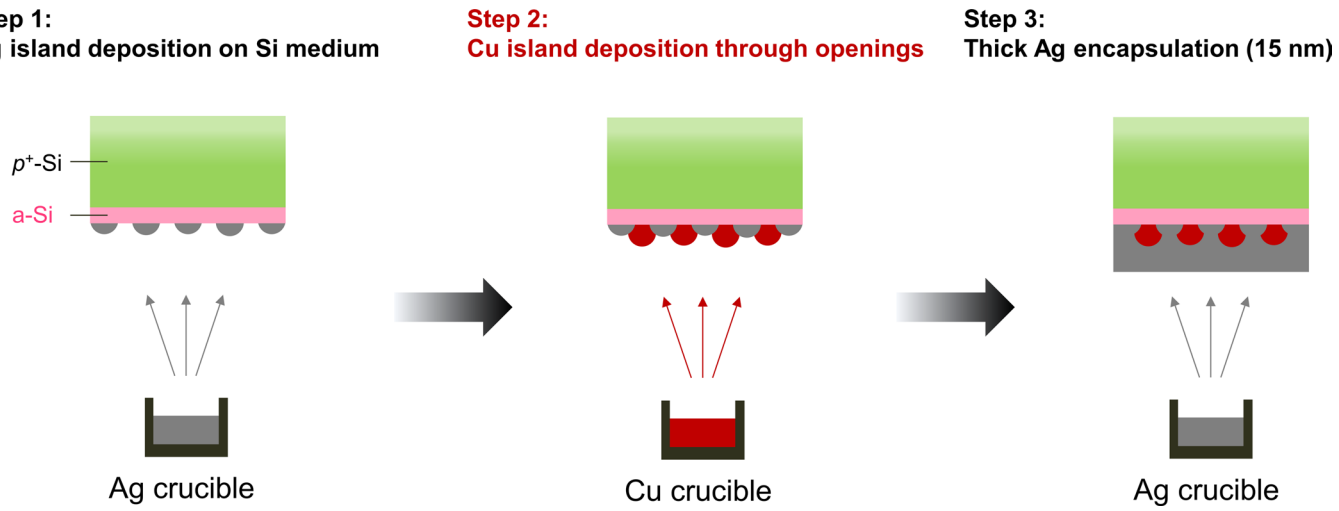
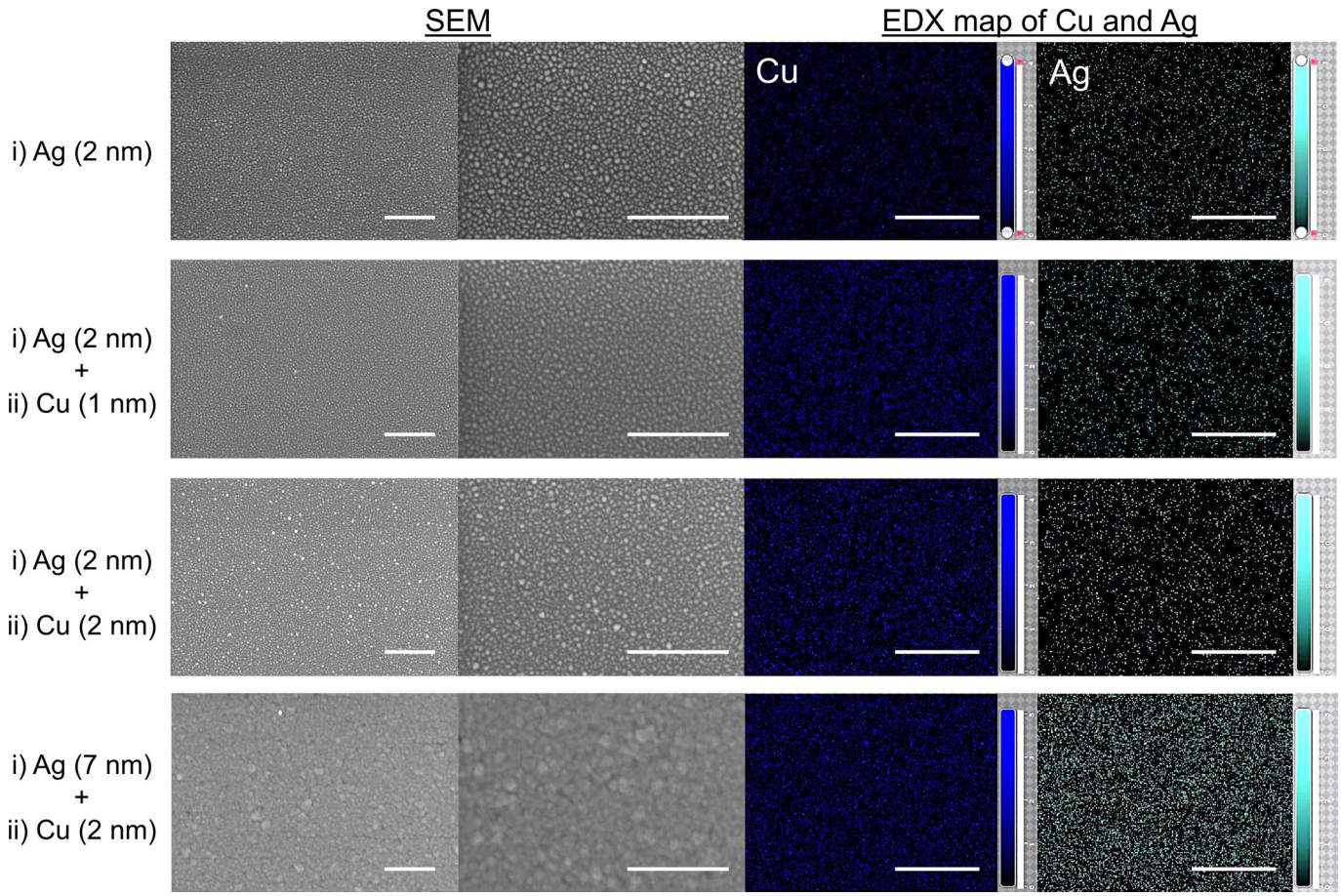
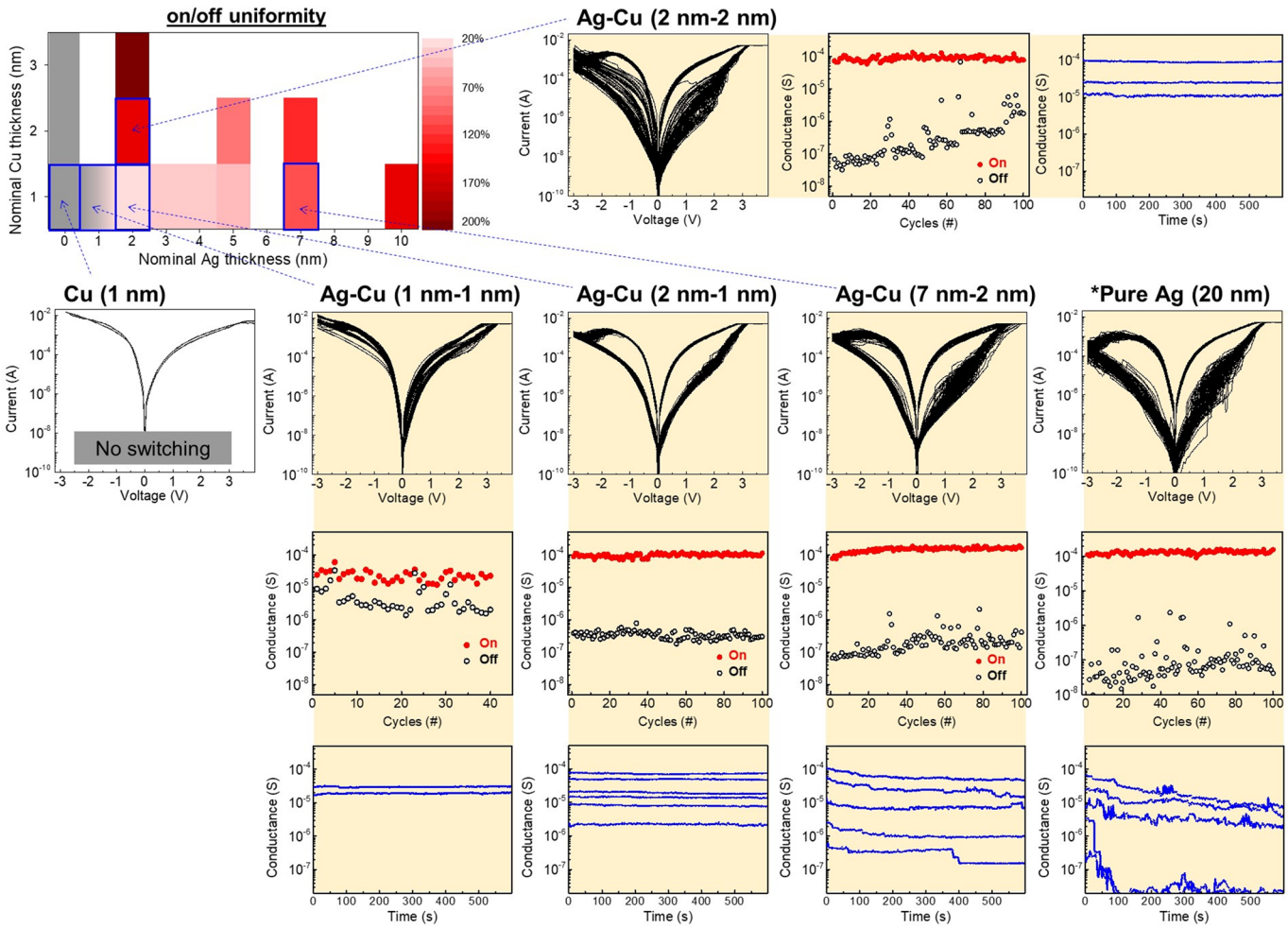


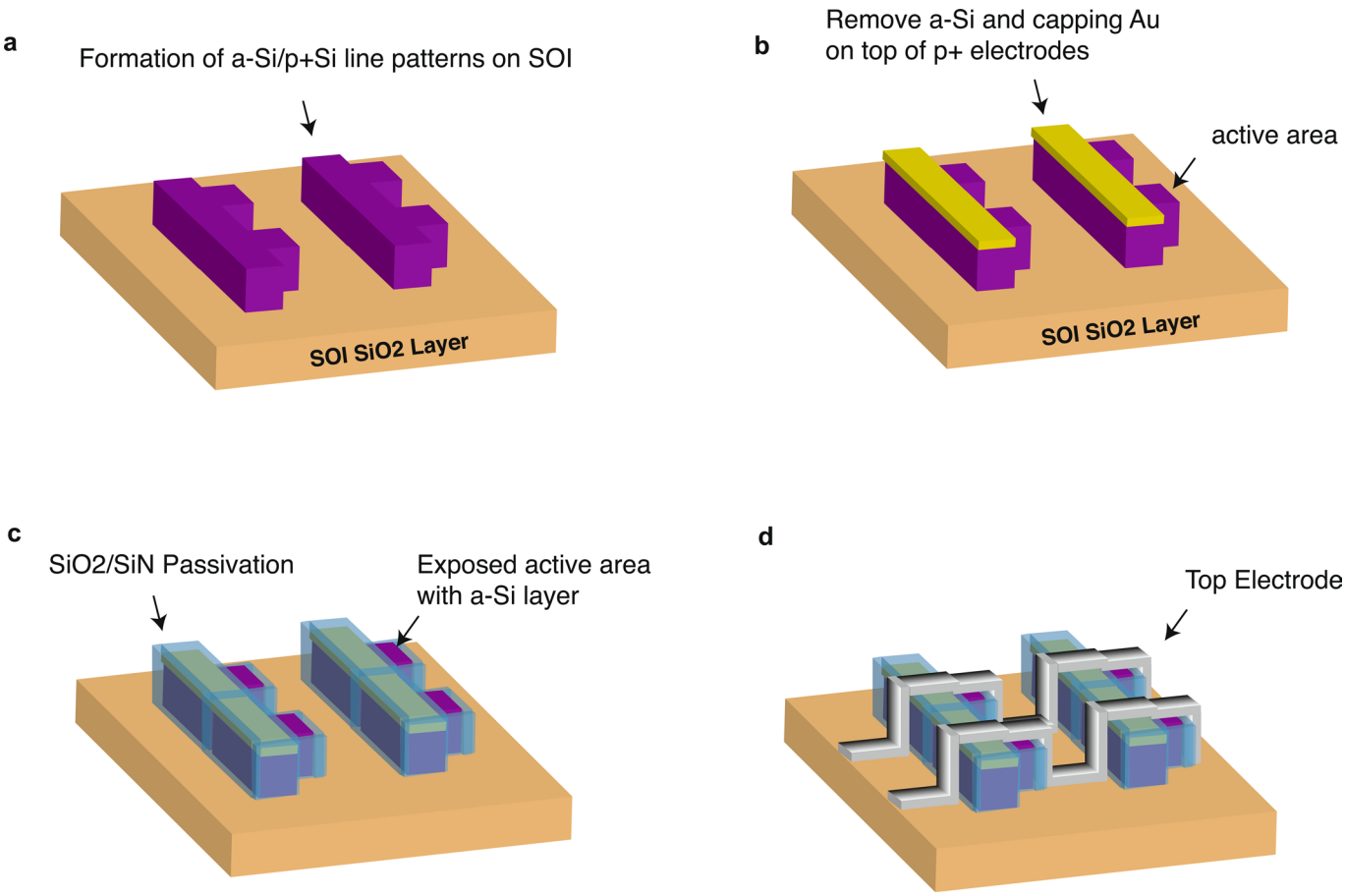
Extended Data Fig. 1 | Process flow of depositing Ag-Cu films for active metals. We have design step-by-step metal deposition process to drive Ag-Cu together into switching medium on the stage of forming. We first deposited ultrathin Ag islands on switching medium, where the thickness of Ag islands determines the opening area of Si (step1). Next, we deposited ultrathin Cu on top of Ag islands-deposited Si where Cu islands make the direct contact with the switching medium (step2). Last, we encapsulated Ag-Cu islands with 15 nm thick Ag film (step3). The amount of Cu involved in switching is determined by 'Ag-Cu thickness ratio'. The thicker Ag film is deposited, The less Cu is contributing to the switching. The Ag-Cu alloying conduction channels are formed in the switching medium during forming process.



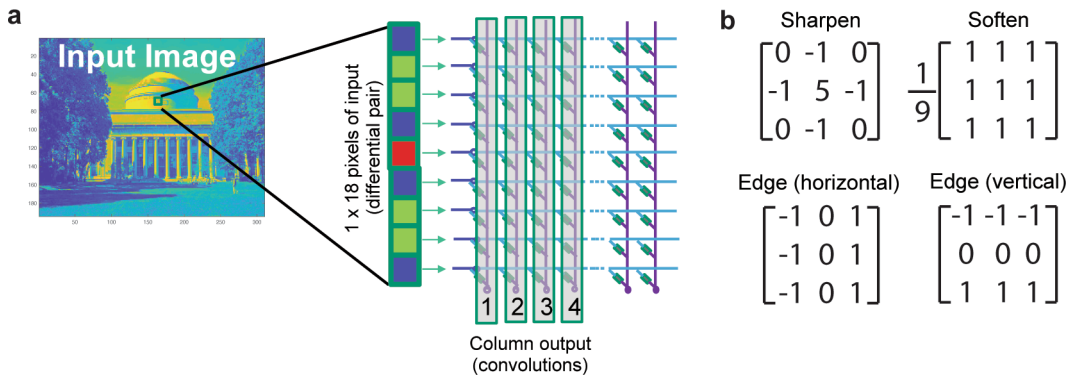
Extended Data Fig. 2 | Ag-Cu alloy formation. Scanning electron microscopy (SEM) images and energy dispersive X-ray (EDX) mapping of Ag-Cu alloying film on amorphous Si surface. Scale bars: 400 μm. When the total thickness was 2 ~ 4 nm, discontinuous metal films were formed and the metal clusters were uniformly distributed. A merging of metal clusters was observed at 7-nm-thick Ag with 2-nm-thick Cu film Source data.



Extended Data Fig. 3 | Ag-Cu alloying ratio effect on DC switching uniformity and retention. Normalized on/off uniformity with respect to nominal thickness of (i) Ag and (ii) Cu layers. 15-nm-thick additional Ag layer was applied after the step-by-step evaporation. At each alloying condition, best-performed-device during 100 cycles at compliance current of 5 mA was selected for this mapping. Furthermore, DC switching curves with temporal on/off conductance variations and room temperature retention results are included. When Cu was evaporated even for 1 nm in advance to Ag, devices showed irreversible breakdown behavior that is similar results with pure Cu devices (20-nm-thick Cu layer). As Ag thickness increased under fixed Cu thickness (1 nm), switching performance dynamically modulated and Ag (2 nm)/Cu (1 nm) layers drove optimized switching performance: highly uniform switching with stable retention behavior at multi-level states. As Ag-Cu ratio was deviated from 2 nm-1nm, non-uniform switching with poor retention was observed (7 nm-1 nm) or on/off degradation occurred, although stable data retention was obtained (2 nm-2 nm). These results strongly suggest that Cu additives into Ag active electrode significantly affect the switching performance, even though the amount of Cu is too small to form continuous film on Si surface. Furthermore, the role of Cu can be summarized as follows. (1) Cu enhances stability of Ag-based conduction channel, but decreases maximum on/off ratio due to residual Cu elements bound to Si switching medium (called backbone of the conduction channel). (2) Excess Cu in Ag active electrode deteriorates on/off window with increasing cycle number. However, optimized Ag-Cu ratio can drive uniform switching with relatively stable data retention Source data.



Extended Data Fig. 4 | Crossbar layout for alloy arrays with metal capping. Metal capping for p^+ Si bottom electrodes is preferred to reduce the line resistance in large array implementations. A new process was developed to make alloy array with gold capping layer. (**a**) formation of isolated a-Si/p^+ Si line patterns on SOI wafer by photolithography and dry etching. The protrusions on the line patterns are active device areas. (**b**) capping Au on top of the p+ line patterns to reduce line resistance. The active areas remain intact. (**c**) passivation of the bottom electrodes while exposing the active areas. (**d**) patterning the top electrodes to finish device arrays.



Extended Data Fig. 5 | Demonstration of the stability of Ag-Cu alloy memristor array for inference. (a) four convolutional kernels shown in (**b**) were programmed into four columns of the 32 × 32 array for parallel kernel operation. Two memristors are used as differential pair to represent both positive and negative weights.