Double-Gate MoS_2 FET with a Multilayer Graphene Floating Gate: A Versatile Device for Logic, Memory, and Synaptic Applications

Michael A. Rodder, Sudhanva Vasishta, and Ananth Dodabalapur

Microelectronics Research Center, The University of Texas at Austin, Austin, Texas, 78758, United States

Supporting Information Placeholder

ABSTRACT: 2D materials with low-temperature processing hold promise for electronic devices that augment conventional silicon technology. To meet that promise, devices should have capabilities not easily achieved with silicon technology, including planar FDSOI (Fully-Depleted Silicon-on-Insulator) with substrate body-bias, or vertical finFETs with no body-bias capability. In this work, we fabricate and characterize a device (double-gate MoS_2 FET with h-BN gate dielectrics and multi-layer graphene floating gate) in multiple operating conditions to demonstrate logic, memory, and synaptic applications; a range of h-BN thicknesses is investigated for charge retention in the floating gate. In particular, we demonstrate this device as a i) logic FET with adjustable V_T by charge stored in the floating gate, ii) digital flash memory with lower pass-through voltage to enable improved reliability, and iii) synaptic device with decoupling of tunneling and gate dielectrics to achieve a symmetric program / erase conductance change. Overall, this versatile device, compatible to back-end-of-line integration, could readily augment silicon technology.

Electronic devices made from various two-dimensional (2D) materials are being actively researched for separate logic, memory, and synaptic applications.[1–5] Logic FETs comprised of a single-gate or double-gates, with a channel comprised of thin semiconducting transition metal dichalcogenide (TMD) material, e.g. MoS_2, and with a gate dielectric comprised of hexagonal boron nitride (h-BN), for a nearly defect free interface to the TMD channel, have been demonstrated with superb gate control, near-ideal subthreshold slope, and (for double-gate logic FETs) threshold voltage (V_T) modulation.[6–9] Non-volatile memory (NVM) devices, including resistive random-access memory (RRAM),[10] ferroelectric FETs,[11] floating gate memory devices,[12] and charge-trapping memory devices,[13] have been fabricated with 2D materials. NVM devices with a single-gate, MoS_2 channel layer, high-k gate dielectric, and a floating gate comprised of multi-layer graphene,[14] or with a double-gate, MoS_2 channel layer, and high-k gate dielectric / charge-trapping layer[15] have been demonstrated with excellent hysteresis, charge retention, and (for the double-gate NVM), hysteresis modulation. Memory devices have taken on further importance due to a renewed focus on neuromorphic computing[16] and the need for non-volatile analog memory devices with multiple conductance states, i.e. weights.[17–19] As example, synaptic devices have been demonstrated with a single gate, MoS_2 channel layer, h-BN gate dielectric, and a floating gate comprised of graphene.[20]

It is noted that the above-mentioned devices each serve and/or focus on one application, i.e. either a logic or memory or synaptic application. However, to augment conventional silicon technology with 2D-materials technology, we suggest that there should be a versatile device having capabilities not easily achieved with conventional silicon technology, that enables logic and memory and synaptic applications, and with compatibility to back-end-of-line (BEOL) integration. Such a device could be formed in a single level in the BEOL but serve multiple applications at different chip locations; in this manner, only one device structure needs to be added to the BEOL rather than multiple device structures for each of the applications. Additionally, the versatile device should be able to overcome some of the variations inherent to device processing or device operation. Accordingly, the versatile device must have double gates, an easily integrable and robust gate dielectric with a high-quality dielectric / channel interface on both top and bottom of a FET channel, and a memory charge storage layer of small height for further ease of integration.

To this end, we fabricate and characterize a double-gate MoS_2 FET with h-BN gate dielectrics (on top and bottom of the MoS_2 channel layer) and a multi-layer graphene floating gate in multiple operating conditions to demonstrate its logic, memory, and synaptic applications; a range of h-BN thicknesses is investigated for charge retention in the floating gate. (It is noted that the h-BN serves as both a conventional gate dielectric and a tunneling dielectric.) First, we demonstrate this device as a logic FET (using the top gate as the logic FET control gate) with threshold voltage (V_T) adjustable by charge stored in the floating gate to e.g. meet target V_T specs (using the bottom gate to affect charge storage in the floating gate), without need for doped silicon substrate regions for body-bias as in FDSOI technology. Second, we demonstrate this device as a digital NAND flash memory (using the bottom gate to affect charge storage in the floating gate) with enablement of improved reliability by bias applied to the top gate (to shift hysteresis curves of the memory device), without need for high pass-through voltage as in conventional silicon technology. Third, we demonstrate this device for synaptic applications with multiple conductance states, i.e. weights in a synapse (using bottom gate pulsing to modulate charge in the floating gate) and with symmetric conductance change between program and erase (by operating the top-gated device in subthreshold), without need to utilize the tunneling dielectric to affect both charge storage and symmetry of conductance change as in conventional single-gate silicon technology.

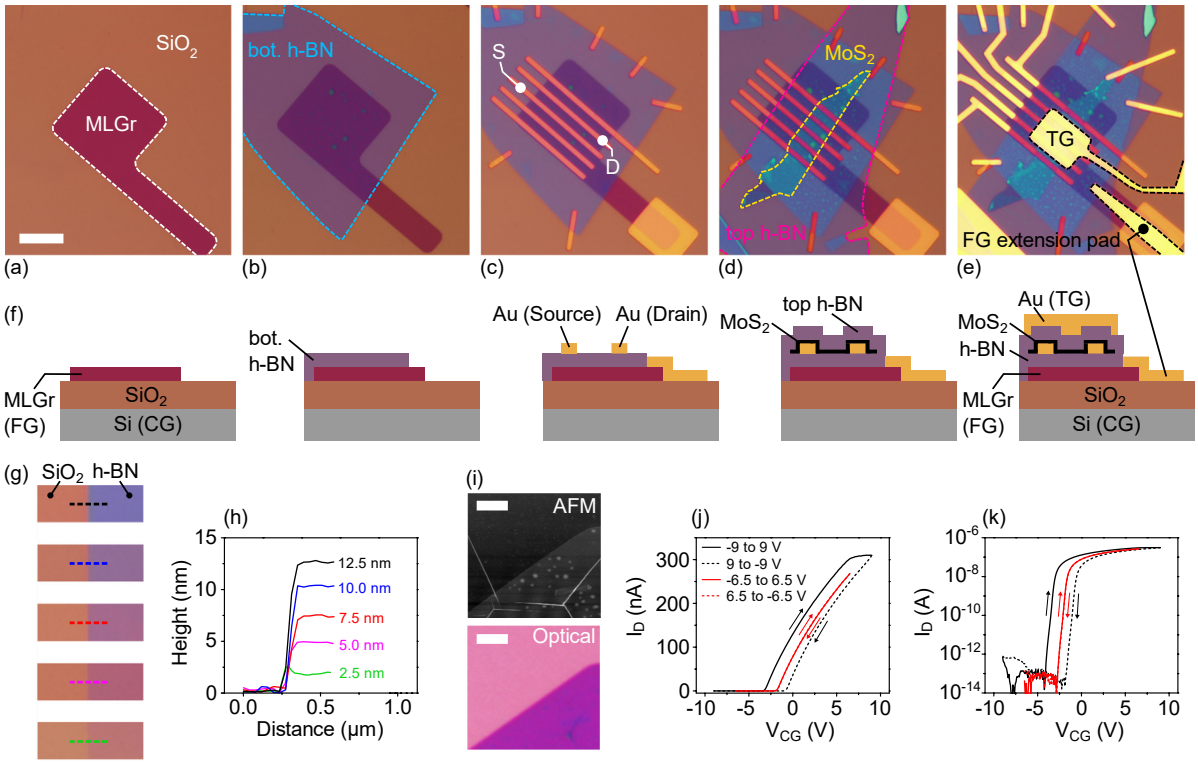

Figure 1. Optical micrographs of the fabrication process flow for the device, showing (a) the patterned multi-layer graphene (MLGr) floating gate (FG) on an n^{++} Si/SiO_2 wafer, with n^{++} Si used as the control gate (CG) and SiO_2 used as the control gate dielectric; (b) a first h-BN (tunneling dielectric) dry-transferred onto the MLGr FG; (c) the patterned Au source/drain (S/D) electrodes; (d) a second h-BN (gate dielectric) and the MoS_2 channel layer dry-transferred on top of the S/D electrodes; and (e) the patterned top gate (TG), S/D pads, and MLGr FG extension pad. (f) Cross-sectional schematics of the optical micrographs of the process flow in (a-e). (g) Optical micrographs showing the color contrast between SiO_2 and exfoliated h-BN flakes of varying thicknesses. (h) AFM step heights corresponding to the h-BN flakes shown in (g). (i) AFM scan and optical micrograph (of the same location) showing some wrinkling of a 5 nm thick h-BN dry-transferred onto the MLGr FG. (j) Linear-linear plot of I_D-V_{CG} sweep showing hysteresis (when charge tunnels to/from the MLGr FG) only for the case of a sufficiently large (magnitude of) CG voltage (shown for the case of thick h-BN). (k) Log-linear plot of same sweep as in (j).

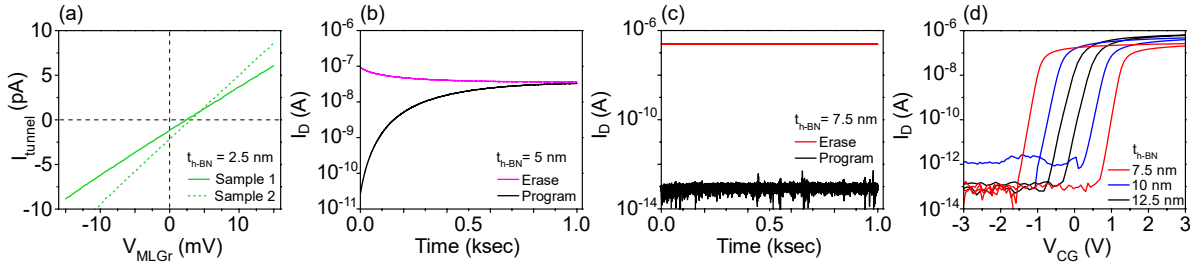

Figure 2. (a) Tunneling current vs. MLGr FG voltage through a 2.5 nm h-BN tunneling dielectric (measurement using the MLGr FG extension pad). Retention time of drain current (I_D) in the Erase and Program states for the case of a h-BN tunneling dielectric thickness of (b) 5 nm and (c) 7.5 nm. (d) Log-linear transfer characteristics showing well-defined hysteresis loops for cases of sufficiently thick h-BN tunneling dielectric: 7.5 nm, 10 nm, and 12.5 nm, showing larger hysteresis width at thinner h-BN (shown for the case of a CG voltage sweep of -6.5 V to 6.5 V, then from 6.5 V to -6.5 V; V_S = 0 V; V_D = 10 mV; and V_{TG} (top gate voltage) = 0 V).

RESULTS AND DISCUSSION

Devices are fabricated as shown by the optical micrographs of the process flow in Figure 1a-e, and by the corresponding cross-sectional schematics in Figure 1f. The fabrication process flow utilized a dry-transfer technique[21–23] for pick-up / placement of the exfoliated flakes (MoS_2, h-BN), electron beam lithography, and metal patterning by deposition / liftoff. Fabrication details are in the Materials and Methods section. The n^{++} Si substrate is referred to as the control gate (CG), the multi-layer graphene (MLGr) serves as the floating gate (FG), and the top Au metal is referred to as the top gate (TG). The bottom h-BN is referred to as the tunneling dielectric; the top h-BN is referred to as the gate dielectric. A metal extension pad (area = 300 μm^2) is connected to the MLGr FG to enable electrical probing of the FG, or to increase coupling capacitance.[12,20] (Unless otherwise specified, the MLGr FG is floating.) h-BN tunneling dielectric thickness from 2.5 nm to 12.5 nm is studied. Color contrast and AFM step height of varying thickness, bottom h-BN flakes are shown in Figure 1g-h. Figure 1i shows that

thin h-BN flakes ≤5 nm were observed to have wrinkles from the dry-transfer process. Figure 1j-k shows well-defined hysteresis loops for (non-wrinkled) thick h-BN flakes, for the case of a sufficiently large CG sweep. Figure 2 details the characteristics of different thickness h-BN tunneling dielectrics to determine an appropriate choice of h-BN thickness for subsequent device characterization. Figure 2a shows linear I-V even at small bias for thin 2.5 nm h-BN (V_S = 0 V; V_D = 10 mV; $|V_{MLGr}| < 15$ mV applied to the metal extension pad connected to the MLGr FG); this indicates that 2.5 nm h-BN is too thin for charge storage retention in the FG, consistent with Vu, *et al*.[24] Figures 2b-c show retention time of drain current (I_D) in the Erase and Program states for h-BN thicknesses of 5 and 7.5 nm. Charge retention is poor for 5nm h-BN but improved for 7.5 nm h-BN, i.e. no charge loss is observed up to 1000 sec (maximum stress time investigated for the purposes of this work). Figure 2d shows I_D-V_{CG} (for V_{CG} sweeps of ±6.5 V) for devices with h-BN thickness = 7.5, 10, and 12.5 nm. Well-defined hysteresis loops are observed for h-BN thickness ≥ 7.5 nm; as expected, a larger hysteresis width is observed at thinner h-BN due to higher tunneling current. From Figures 2c-d, subsequent device characterization is with h-BN tunneling dielectric thickness ≥ 7.5nm.

Logic application: We first demonstrate this device as a logic FET (using the top gate as the logic FET control gate) with threshold voltage (V_T) adjustable by charge stored in the FG. Threshold voltage plays a major role in the performance of most of the analog/mixed signal circuits. Tuning threshold voltage post-fabrication helps tackle V_T-mismatches in current mirrors[25] and offset calibration in differential amplifiers and mixers.[26] Manipulation of threshold voltage aids in altering logical switching threshold of inverters[27] and to accomplish the required static noise margin[28] of digital circuits in case of on-chip V_T variation.

Figure 3a, which details the hysteresis loops from electron and hole tunneling into the FG, shows that charge in the FG can be negative (from electron tunneling) or positive (from hole tunneling). The dashed black curve is a plot of I_D-V_{MLGr} (V_{TG} = 0 V; V_{CG} = 0 V); subsequently, the FG is de-probed (floating) and the CG is swept from ± 3.5 V (green reference curve); $|V_{CG}| \leq 3.5$V is small so that no charge tunneling occurs. (Green and black curves overlie due to negligible voltage drop across the 300 nm SiO_2 due to the large extension pad on the FG and large overlap between extension pad and CG.) Compared to the green reference curve, sweeping V_{CG} to a large positive bias (red curve) results in negative charge in the FG (from electron tunneling) and positive V_T shift. Correspondingly, sweeping V_{CG} to a large negative bias (purple curve) results in positive charge in the FG (from hole tunneling) and negative V_T shift.

The results of Figure 3a suggest that V_T of the top-gated logic FET, with MoS_2 channel, can be readily shifted to desired values within a fairly wide range, e.g. to a target V_T spec, by controlling the amount and polarity of the charge in the FG; this is shown in Figure 3b. Figure 3b shows linear-linear plots of I_D-V_{TG}, for -8 V ≤ V_{CG} ≤ +10 V, for a single 100ms V_{CG} pulse except as specified for V_{CG} = +10 V with pulse number from 1, 4, to 100 pulses (each at 100ms). Indeed, V_T of the top-gated logic FET can be shifted from negative V_T (e.g. V_T = -1 V, at V_{CG} = -8 V, single pulse) to positive V_T (e.g. V_T = +1 V, at V_{CG} = +10 V, 100 pulses). That is, V_T can be shifted by different amounts just by pulsing the CG at a single voltage (e.g. V_{CG} = 10 V) but with a variable number of pulses (rather than requiring variable V_{CG}). Figure 3c shows the correspondingly shifted log-linear plots of I_D-V_{TG}, due to the shifted V_T. It is noted that V_{TG} does not alter the stored charge in the FG, due to screening of V_{TG} by the (MoS_2) channel layer.[29]

This demonstration of the versatile device as a logic FET with

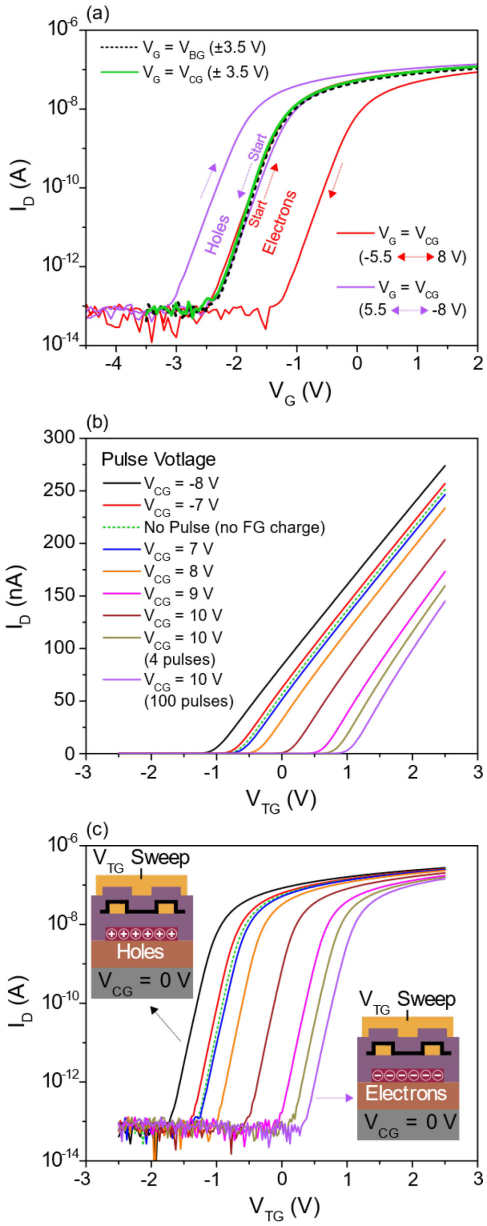

Figure 3. (a) Log-linear transfer characteristics showing positive and negative charge storage in the FG. (b) Linear-linear transfer characteristics showing shift in V_T by varying V_{CG} with a single CG voltage pulse (100ms), or by fixing V_{CG} and varying the number of CG voltage pulses. (c) Correspondingly shifted log-linear transfer characteristics (as in (b)) due to shifted V_T. V_{DS} = 10 mV.

adjustable V_T for logic circuitry, as shown in Figures 3a-c, while also having memory and synaptic applications (to be discussed in next sections), is important for three reasons. First, for any logic application, it is important to be able to meet target V_T specs, for which V_T may range from low V_T (for higher speed) to high V_T (for lower leakage). In many circuits, it is advantageous to adjust V_T post-processing, to further overcome process variations which occur in manufacturing. Second, it is difficult to adjust V_T of a FET with a TMD channel by directly doping the TMD channel layer.[30,31] However, we have demonstrated that we can adjust the V_T of a FET with a MoS_2 channel by electrostatically doping the MoS_2 channel, by directly adjusting the charge stored in the FG. (It is noted that while a conventional double-gate FET architecture, with a MoS_2

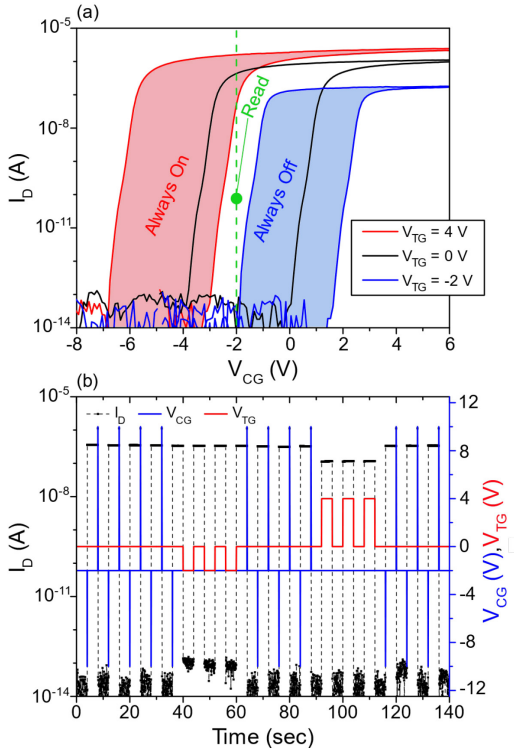

Figure 4. (a) Log-linear transfer characteristics showing shifted hysteresis loops for I_D-V_{CG} (V_{CG} swept from ± 10 V), for V_{TG} = 0, -2, or 4 V. (b) Switching of a memory device from a read condition (V_{TG} = 0 V) to an 'Always Off' condition (V_{TG} = -2 V) or to an 'Always On' condition (V_{TG} = 4 V). V_{DS} = 100 mV.

channel but without the FG, enables one of the dual gates to adjust V_T by electrostatic doping,[7] a conventional double-gate FET architecture cannot achieve all of logic, memory, and synaptic applications.) Third, the device has capabilities not easily achieved with conventional silicon technology. For example, vertical silicon finFETs have no body-bias capability (i.e. no V_T adjust capability, post-processing). Additionally, planar FDSOI requires substrate body-bias applied to separately doped silicon substrate regions to variably adjust V_T. (Note also that in FDSOI, there is no capability of a single body-bias voltage, but with varying pulse number, to variably adjust V_T to multiple values.) The versatile device in this work indeed does not require SOI technology, and is able to adjust V_T to a target spec, post-processing, unlike vertical finFETs.

Memory (NAND flash) application: We next demonstrate this device as a digital flash memory (using the bottom control gate (CG) to affect charge storage in the floating gate) with enablement of improved reliability by biasing of the top gate (TG). Conventional digital NAND flash memory has reliability problems due to read disturb errors, data retention errors, and/or errors induced by program/erase (P/E) cycle count.[32] For example, in conventional single-gate silicon technology, read disturb errors can arise due to repeated use of high pass-through voltage (V_{pass}) applied to the CG (V_{pass} = V_{CG} > highest V_T of all memory devices on a bitline), required to turn all devices in series on a same bitline to an 'Always On' condition (except the device being read) during a read operation.[33] Since V_{pass} is applied to the CG (i.e. the only gate in a single-gate memory), high V_{pass} affects (increases) the charge stored in the FG, eventually leading to read disturb errors in conventional silicon technology.[34]

Accordingly, reliability of digital flash memory will be increased if a series of memory devices can be turned on without significantly

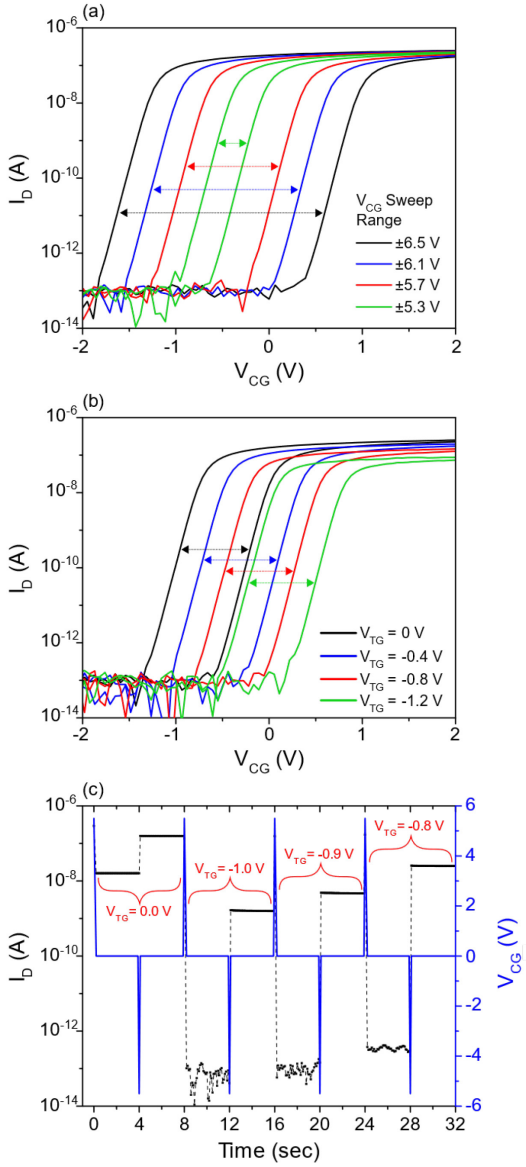

Figure 5. (a) Log-linear transfer characteristics (7.5 nm h-BN tunneling dielectric) for various V_{CG} sweeps (with V_{TG} = 0 V). (b) Log-linear transfer characteristics for fixed V_{CG} sweep of ±5.5 V, with varying V_{TG} = -0.4, -0.8, -1.2 V. (c) Switching between Program (off) and Erase (On) states by use of alternating V_{CG} pulses (± 5.5 V, 100 ms), at varying V_{TG}, showing dependence of On/Off ratio on V_{TG} for the case of read voltage at V_{CG} = 0 V. V_D = 10 mV.

disturbing the stored charge in the FG during a read operation (while a particular memory device is being read). Such an increase in reliability is not readily achieved with a conventional single-gate flash memory for which high V_{pass} = V_{CG} disturbs the stored charge in the FG, but is readily achieved with the device in this work; V_{TG} does not affect the stored charge in the FG (since V_{TG} is screened by the MoS_2 channel layer) and V_{TG} can be biased such that the memory devices can be 'Always On' as shown in Figure 4. Figure 4a shows hysteresis loops for I_D-V_{CG} (from a V_{CG} sweep ± 10 V), for V_{TG} = 0, -2, or 4 V. The memory device being read is shown for a read voltage at e.g. V_{CG} = -2 V, centered within the hysteresis loop (shown in black) at V_{TG} = 0 V. The memory device(s) being turned 'Always On' is shown for a low (in magnitude) V_{pass}, also

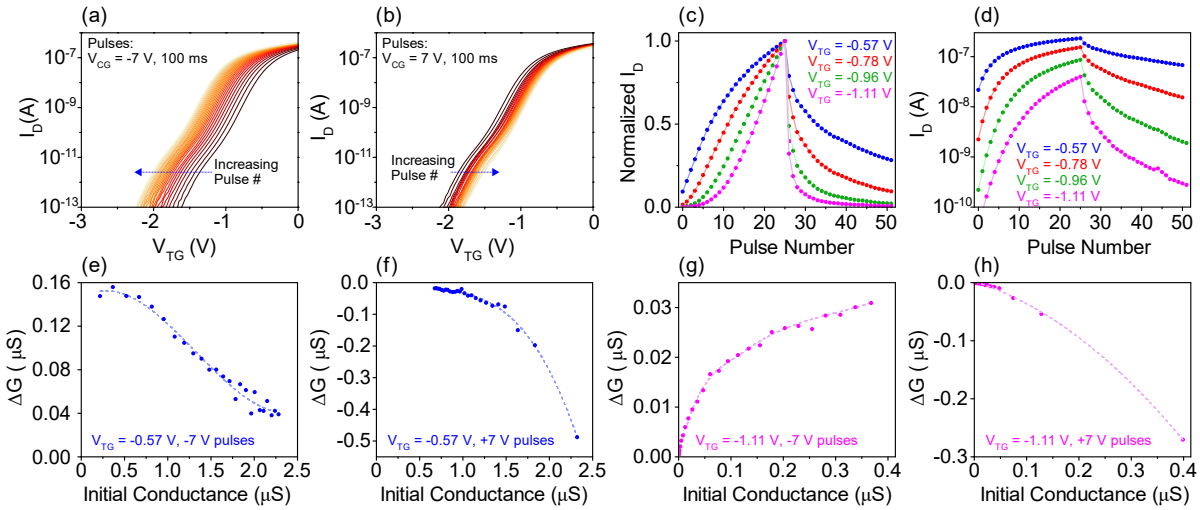

Figure 6. (a) I_D-V_{TG} for the top-gated device after each of 25 CG pulses (pulses 1-25; V_{CG} = -7 V, 100 ms), showing shift to a higher conductance in an analog manner. (b) I_D-V_{TG} for the top-gated device after each of 25 CG pulses (pulses 26-50; V_{CG} = +7 V, 100 ms), showing shift to a lower conductance in an analog manner. (c) Normalized I_D vs. pulse number, for varying V_{TG} (at V_{CG} = 0 V) with pulses 1-25 at V_{CG} = -7 V (V_{TG} = 0 V), and pulses 26-50 at V_{CG} = +7 V (V_{TG} = 0 V). (d) Actual I_D vs. pulse number, as in (c). Change in conductance vs. initial conductance at (e) read voltage V_{TG} = -0.57 V, after each of 25 CG pulses (pulses 1-25; V_{CG} = -7 V, 100 ms), (f) read voltage V_{TG} = -0.57 V, after each of 25 CG pulses (pulses 26-50; V_{CG} = +7 V, 100 ms), (g) read voltage V_{TG} = -1.11 V, after each of 25 CG pulses (pulses 1-25; V_{CG} = -7 V, 100 ms), (h) read voltage V_{TG} = -1.11 V, after each of 25 CG pulses (pulses 26-50; V_{CG} = +7 V, 100 ms).

set to V_{pass} = V_{CG} = -2 V, but with V_{TG} = 4 V, to shift the hysteresis loop (shown in red) fully to the left of V_{CG} = -2 V, to achieve the 'Always On' condition, i.e. I_D is high for both Program and Erase states. (Additionally, it is noted that a memory device can also be shifted to an 'Always Off' condition, if desired; e.g. for V_{TG} = -2 V, the hysteresis loop (shown in blue) is fully to the right of V_{CG} = -2 V, i.e. I_D is low for both Program and Erase states). Figure 4b shows switching of a memory device from a read condition (V_{TG} = 0 V) to an 'Always Off' condition (V_{TG} = -2 V) or to the 'Always On' condition (V_{TG} = 4 V). V_{CG} (blue curve) is pulsed using 100ms pulses at ±10 V to switch states between Program (Off) and Erase (On). Consistent to Figure 4a, Figure 4b shows that the device can be 'Always Off' using the TG with V_{TG} = -2 V, and can be 'Always On' using the TG with V_{TG} = 4 V. Figures 4a-b show that the TG, which is easily integrated in the device in this work, can enable switching memory device(s) to be 'Always On' (or 'Always Off' if desired) without significantly affecting charge stored in the floating gate (since V_{TG} does not affect stored charge in the FG, and $|V_{pass}|$ can be a low voltage), to improve reliability beyond that which can be achieved with conventional silicon technology.

Figure 5 shows additional advantages of the TG for improving reliability of the digital flash memory. Consider that a read voltage is established at V_{CG} = 0. Figure 5a shows hysteresis loops for various V_{CG} sweeps (with V_{TG} = 0 V); a successful read of Program and Erase states then requires a larger V_{CG} sweep of ±6.5 V (and larger stored charge in the FG) to establish a sufficiently large ΔV_T between the Program and Erase states. However, a larger V_{CG}, i.e. a larger Program voltage, can result in data retention errors from stress-induced leakage current due to electrical degradation of the tunneling dielectric between the channel and FG.[35] Thus, it is desired to reduce the value of V_{CG} to establish the Program state, but still enable the read voltage at V_{CG} = 0 V. Figure 5b shows a case in which a smaller V_{CG} sweep of ±5.5 V is utilized, with V_{TG} then adjusted from 0 V to V_{TG} = -0.8, -1.2 V to shift the hysteresis loop to enable a successful read of Program and Erase States, at a read voltage V_{CG} = 0 V. Figure 5c shows that a successful read of Program and Erase states can be achieved at/near V_{TG} = -0.9 V, for which a sufficiently large On/Off current ratio is achieved to distinguish between the two states. It is more advantageous to utilize V_{TG} to shift a smaller hysteresis curve towards the read voltage, rather than utilize a larger V_{CG} to broaden a hysteresis loop, since V_{TG} does not degrade the tunneling dielectric, unlike V_{CG}, since the field from V_{TG} is screened by the MoS_2 channel layer.

Synaptic application: We lastly demonstrate this device for synaptic applications with multiple conductance states by multiple pulsing of the CG, and with symmetric P/E conductance change by operating the top-gated device in subthreshold. Conventional floating-gate flash memory, utilizing single-gate silicon technology, has shown compatibility to synaptic applications by similar multiple pulsing of the CG, and with symmetric P/E conductance changes by operating the CG-gated device in subthreshold.[36] For this conventional silicon technology, the field in the tunneling dielectric is large during P/E cycles which can lead to wearout of the tunneling dielectric, including formation of traps in the dielectric, that may affect the shape of the subthreshold region (e.g. subthreshold slope) of I_D-V_{CG} over the operating lifetime.

It is expected that reliability (i.e. stability) of the device for synaptic applications will be improved if the device can be operated in subthreshold utilizing a dielectric which does not see a large field during P/E cycles. Such a dielectric is readily achieved with the device in this work for which the field in the top-gate dielectric is always small since it is not subjected to a high field during P/E cycles (since the top-gate dielectric is screened by the MoS_2 channel) and $|V_{TG}|$ is low in the subthreshold region of I_D-V_{TG}. That is, the gate dielectric is decoupled from the tunneling dielectric. Figures 6a-b show example shifts in I_D-V_{TG} from multiple (100 ms) pulsing of the CG (to modulate charge in the FG), either for negative V_{CG} (V_{CG} = -7 V: pulses 1-25; to increase conductance) or positive V_{CG} (V_{CG} = +7 V: pulses 26-50; to decrease conductance), with V_{TG} = 0 V. (A detailed pulsing study (pulse width, different magnitude of positive vs. negative pulses, etc.) was not performed.) Figures 6c-d show the normalized and actual I_D vs. pulse number, for varying V_{TG}, corresponding to biasing the top-gated device from above-

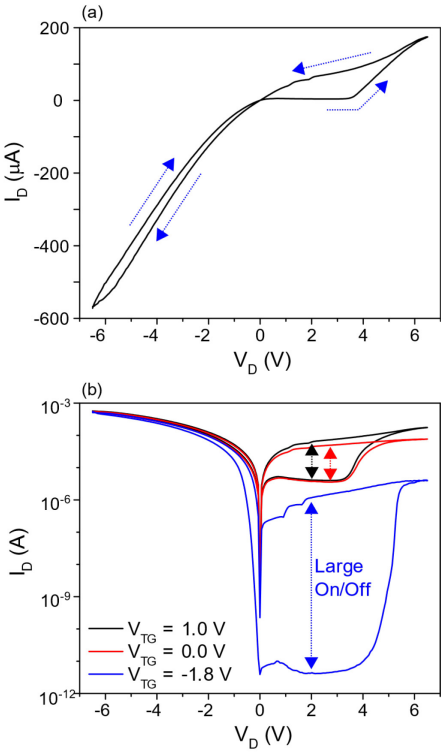

Figure 7. (a) Memristor-like hysteresis sweep of I_D-V_D, with control gate tied to source, V_{TG} = 0V. (b) Sweeps of I_D-V_D for varying V_{TG}, showing large On/Off ratio can be achieved.

threshold (e.g. V_{TG} = -0.57 V) to subthreshold (e.g. V_{TG} = -1.11 V). It is observed in Figure 6c that V_{TG} modulates the concavity of I_D – pulse number (for pulses 1-25) with concave-downward shape of I_D (at V_{TG} = -0.57 V) or concave-upward shape of I_D (at V_{TG} = -1.11 V, in subthreshold).

Figures 6e-h more clearly show the benefit of operating the device as a top-gated device in subthreshold (in addition to the earlier mentioned benefit of small field in the top-gate dielectric). For synaptic applications, it is desirable to have a symmetric conductance change between program and erase.[37] Figures 6e-f show that if the device is operated in above-threshold, then |ΔG| is large when the initial conductance is small for erasing at negative V_{CG} (V_{CG} = -7 V) but |ΔG| is small when the initial conductance is small for programming at positive V_{CG} (V_{CG} = +7 V); that is, there is an asymmetric conductance change between program and erase when the top-gated device is operated in above-threshold. On the other hand, Figures 6g-h show that if the device is operated in subthreshold, then |ΔG| is small when the initial conductance is small for both erasing at negative V_{CG} (V_{CG} = -7 V) and programming at positive V_{CG} (V_{CG} = +7 V). That is, there is a symmetric conductance change between program and erase when the top-gated device is operated in subthreshold.

Overall, the device in this work, when operated as a 4-terminal device, has three benefits: a) the top-gated device operated in subthreshold enables symmetric P/E conductance change; b) the top-gate dielectric does not see a large field during P/E cycles and thus is not subjected to wearout which can affect the shape of the subthreshold region over the operating lifetime; c) the subthreshold slope of the top-gated device can be tailored as desired by adjusting e.g. the thickness of the top-gate dielectric (albeit with tradeoff to operation as a logic FET) without being constrained by the thickness / composition of the tunneling dielectric; this combination of benefits cannot be achieved in conventional silicon technology.

As an additional component of this work on synaptic application, it is noted that the device need not be operated only as a 4-terminal device, for which P/E utilized CG bias and read utilized TG bias. Rather, the device can also be operated as a 3-terminal device, with CG connected to the source (i.e. V_{CG} = V_S), for which P/E is accomplished by source-drain (S/D) bias as in a memristor,[38] and read utilizes the TG (as well as S/D) bias. Figure 7a shows a memristor-like hysteresis sweep of I_D-V_D for a device similar to that used in prior sections, but with the TG metal not overlapping the drain electrode (to avoid wearout of the top-gate dielectric during application of large V_D). Figure 7b shows that the On/Off ratio (between erase and program states) can be significantly increased by negatively biasing V_{TG}, e.g. V_{TG} = -1.8 V, thus showing benefit of the TG for this memristor-like device.

CONCLUSION

In conclusion, we have experimentally demonstrated logic, memory, and synaptic applications of a versatile, double-gate MoS_2 FET with h-BN gate dielectrics and multi-layer graphene floating gate. This versatile device was shown to have capabilities not easily achieved with conventional silicon technology: a) logic FET with adjustable V_T, post-processing, unlike a conventional silicon finFET or without the need for complicated FDSOI technology, b) digital flash memory device with enablement of improved reliability by eliminating the need for a high pass-through voltage, and c) synaptic device with subthreshold operation for symmetric P/E conductance change using an unstressed gate dielectric decoupled from the stressed tunneling dielectric. It was suggested that such a versatile device could readily augment silicon technology.

MATERIALS AND METHODS

Device fabrication: Devices are fabricated using exfoliated flakes of few (2-5) layer MoS_2, h-BN flakes (2-20 nm), and multi-layer graphene (MLGr). The exfoliation process is as follows. A synthetically grown bulk MoS_2 crystal, atmospherically grown h-BN crystals (from 2D Semiconductors), and bulk graphite crystals are exfoliated using the 'scotch tape' method[39] onto separate 285 nm SiO_2 / heavily doped (As) n^{++} Si wafer pieces. SiO_2 thickness enables optimum color contrast between the flake and SiO_2. The n^{++} Si is used as the CG; the SiO_2 is used as the dielectric between the CG and FG. (We note that the n^{++} Si CG and the SiO_2 dielectric are utilized for convenience and could be replaced with a metal gate and non-SiO_2 dielectric). MLGr flakes (5-15 layers) are selected to be used as the FG, then patterned and etched into a 20 um^2 square using EBL (MicroChem PMMA A4 e-beam resist) and a 70 Watt, 30 second O_2 dry plasma etch, followed by PMMA removal in acetone for a few hours. The structure was then annealed at 350 ºC, 6 hours under high vacuum (< 10^{-6} Torr) to remove any remaining PMMA residue. h-BN flakes (2-15 nm) are selected to be used as the tunneling dielectric, then transferred onto the patterned MLGr using the technique in[21–23]: 1) the substrate with h-BN was heated to 40 ºC; 2) a glass with PDMS, hemispherical in shape and coated with PPC, was used to pick up the h-BN flake using a custom micro-manipulator / microscope setup; 3) the h-BN flake was placed and landed on top of the MLGr FG and delaminated from the stamp at 75 ºC. The MLGr / h-BN stack is high vacuum annealed at 350 ºC, 6 hours to remove any stamp residue. Next, Ni / Au (4 nm / 18 nm) S and D electrodes are patterned atop the h-BN using EBL, thermal metal evaporation, and liftoff. Ni is used as an adhesion layer for contacts to stick to the SiO_2; Au is used as a good n-type contact to MoS_2.[7] The device is not annealed after forming S/D

contacts to avoid any agglomeration of the thin Au, but is soaked in acetone for several hours to remove any PMMA/PPC residue. (We note that no hysteresis was observed during forward and reverse gate sweeps (small CG biases) unless charged is tunneled into or out of the MLGr floating gate, indicating clean interfaces.) After S/D metal patterning, an additional h-BN flake (to be used as the top gate dielectric) is then used to pick up a MoS_2 flake; both flakes are placed and landed on top of the S/D metal contacts. As a last step, the top gate and electrode pads (including an 'extension pad' to the FG), comprised of 4 nm / 50 nm Ni / Au, are patterned with the same EBL, thermal deposition, and liftoff process steps as used for S/D formation, thus completing the structure.

Electrical characterization: Electrical measurements were performed with an Agilent 4155C semiconductor parameter analyzer, at room temperature and under vacuum ($< 10^{-4}$ Torr).

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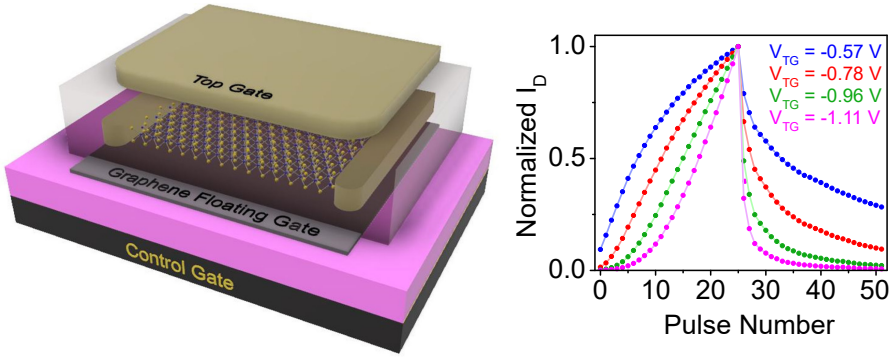
Table of Contents artwork:



Description: 3D schematic of the device from this study, and a data plot (Figure 6c) demonstrating a synaptic application of this device.