Resistance Drift in $Ge_2Sb_2Te_5$ Phase Change Memory Line Cells at Low Temperatures and Its Response to Photoexcitation

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Resistance drift in amorphous $Ge_2Sb_2Te_5$ is experimentally characterized in melt-quenched line-cells from 300 K to 125 K range and is observed to follow the previously reported power-law behavior with drift coefficients in the 0.07 to 0.11 range in dark, linearly decreasing with 1/kT. While these drift coefficients measured in dark are similar to commonly observed drift coefficients (~ 0.1) at and above room temperature, measurements under light show a significantly lower drift coefficient (0.05 under illumination versus 0.09 in dark at 150 K). Periodic on/off switching of light shows sudden decrease/increase of resistance, attributed to photo-excited carriers, followed by a very slow response (~30 minutes at 150 K) attributed to contribution of electron-traps and slow trap-to-trap charge exchanges. A device-level electronic model is used to relate these experimental findings to gradual charging of electron-traps in amorphous $Ge_2Sb_2Te_5$, that gives rise to growth of a potential barrier for holes in time, and hence, resistance drift.

Phase change memory (PCM) is a state of the art non-volatile memory technology that has recently entered the consumer market, filling the gap between DRAM and NAND flash in the memory hierarchy, offering higher speed and endurance compared to NOR and NAND flash memory[1,2]. PCM utilizes the large contrast in conductivity between the crystalline (low-resistance) and amorphous (high-resistance) phase of chalcogenide materials such as $Ge_2Sb_2Te_5$ (GST) to store information[3]. PCM devices can be switched between these two phases using short electrical pulses[4] with endurance levels exceeding 10^{12} cycles[5]. The implementation of multi-bit-per-cell PCM is limited as resistance levels overlap with time due to the drift of the resistance of the amorphous phase with time, following a power-law[6]. Resistance drift has been reported to be a function of annealing and readout temperature[7–13], programmed resistance level[14,15], and read current[16]. There have been several theories explaining the origin of drift[6,17–19], however, the mechanisms giving rise to drift still needs to be fully understood.

Most reports in the literature on resistance drift in PCM cells are on characterization studies at room temperature and above, where multiple processes may be occurring simultaneously. In this work, resistance drift in amorphous GST line cells is monitored in 300 K to 125 K temperature (T) range and the effect of light on the cell resistances is investigated.

The line-cells used in this work were fabricated using 90 nm technology with 250 nm thick bottom metal (Tungsten with Ti/TiN liner) contacts on 700 nm thermally grown SiO_2. GST was deposited using sputtering, patterned using optical lithography and reactive ion etching (RIE) and capped with 10 nm plasma enhanced chemical vapor deposition (PECVD) Si_3N_4 to prevent evaporation of Te during experiments (FIG. 1)[20]. The line cells used in these experiments were 50 nm in thickness (th) with widths (W) varying from ~120 nm to ~150 nm and lengths (L) varying from ~390 nm to 500 nm. A schematic of the measurement setup is shown in FIG. 2. An Agilent 4156C semiconductor parameter analyzer and Tektronix AFG3102 arbitrary function generator were connected to a probe manipulator inside Janis cryogenic probe station through a relay controlled by an Arduino Mega 2560 microcontroller. A series resistor of 1 kΩ on the probe arm was used to limit the current during melting. The relay was not used for T ≤ 150 K as the current going through the PCM cells becomes comparable to the leakage through the relay (~1 pA). Pulse measurements were monitored using Tektronix DPO 4104 digital phosphor oscilloscope as shown in FIG. 2. The chamber was kept under high vacuum (~10^{-5} Torr). Liquid nitrogen was used to cool the chamber and the

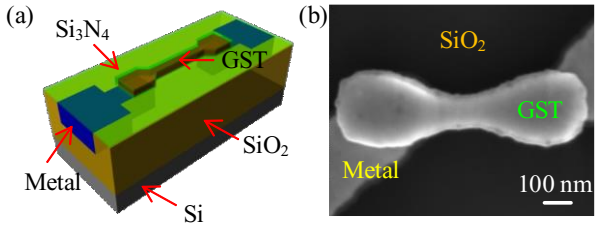

FIG. 1. Schematic (a) and scanning electron microscope (b) image of line cells used in the experiment.

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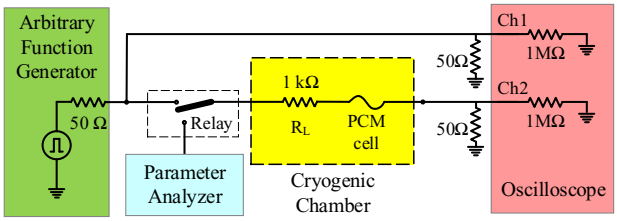

FIG. 2. Schematic of the measurement setup.

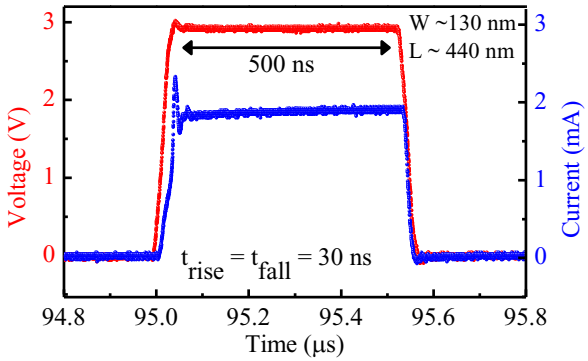

FIG. 3. Voltage used to amorphize the devices (red) and the resulting current (blue) waveforms as measured by the oscilloscope. Current was calculated using the voltage across the 50 Ω termination.

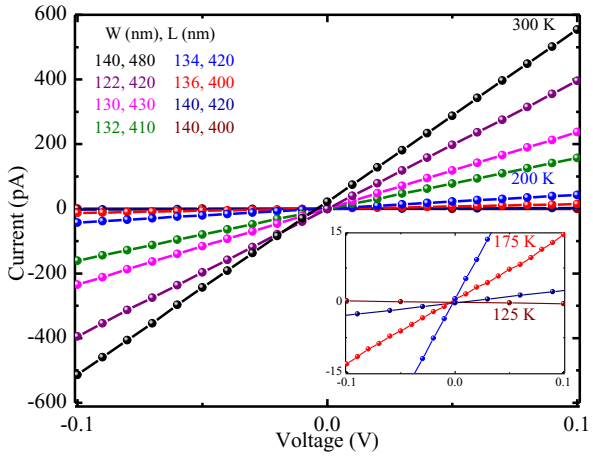

FIG. 4. Current versus voltage graphs for different temperatures in the 125 K to 300 K range. The inset zooms in to show 125 K, 150 K, 175 K and 200 K data.

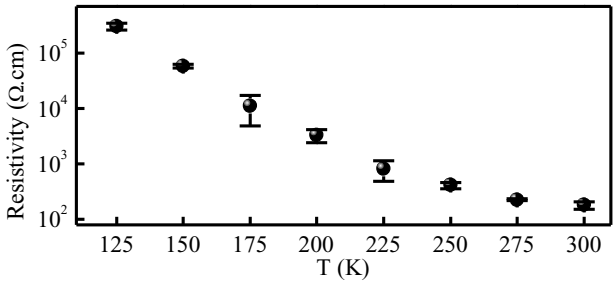

FIG. 5. Initial resistivity of line-cells amorphized at different temperatures, calculated from the I-V characteristics by assuming amorphization of the full length and cross-section of the cells.

chuck, and a Lake Shore 336 temperature controller was used to control the temperature of the chuck.

The line-cells used in the experiment were annealed at 675 K for 20 minutes under high vacuum to ensure that they were all in the crystalline (hcp) phase prior to application of electrical pulses. A 500 ns duration pulse was used to amorphize each line-cell, while the current forced through the cell was monitored (FIG. 3). The long pulse duration ensures melting of the cells. 30 ns rise and fall times were used to minimize waveform distortions due to reflections and

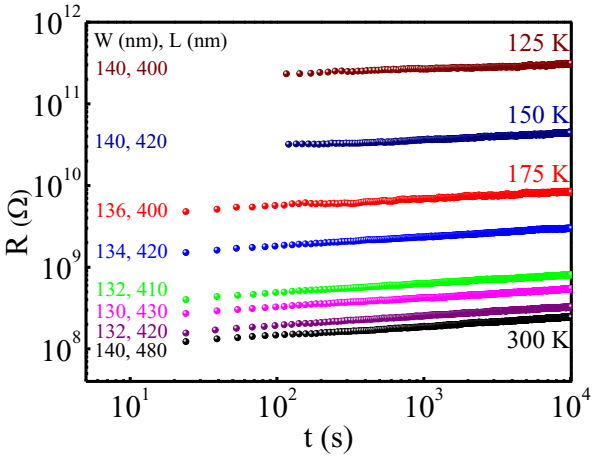

FIG. 6. Resistance (R) versus time (t) plots for line cells amorphized at temperatures from 125 K to 300 K at 25 K intervals. The cell dimensions vary between ~120-140 nm (W) x ~390-500 nm (L) and 50 nm (th). Measurements using a relay enable monitoring of the resistance in the 25 s -100 s period.

parasitic contributions in our setup, while achieving adequate melt-quenching without substantial growth-from-melt from the two solid-liquid interfaces at the ends of the line-cells[21]. The cell resistances were measured using the parameter analyzer with low voltage sweeps to minimize disturbance of the state of the cells (FIG. 4). Multiple line-cells were amorphized at each temperature (FIG. 5) and the resistance of the cells was monitored from ~25 s after the pulse to ~10^4 s (except T = 125 K and 150 K, for which measurement started ~100 s after the pulse due to the delay associated with manual changes in the connections). The cell resistances were monitored at the temperature they were amorphized at.

The amorphized cell resistances were observed to increase with time following the commonly reported power-law[6]:

$$R = R_0 \left(\frac{t}{t_0}\right)^{\gamma}, \quad (1)$$

where R and R_0 are resistances at time t and t_0 respectively and γ is the drift coefficient extracted from the slope of the bi-logarithmic resistance (R) versus time (t) plots (FIG. 6).

We observe a monotonic decrease in drift coefficient from

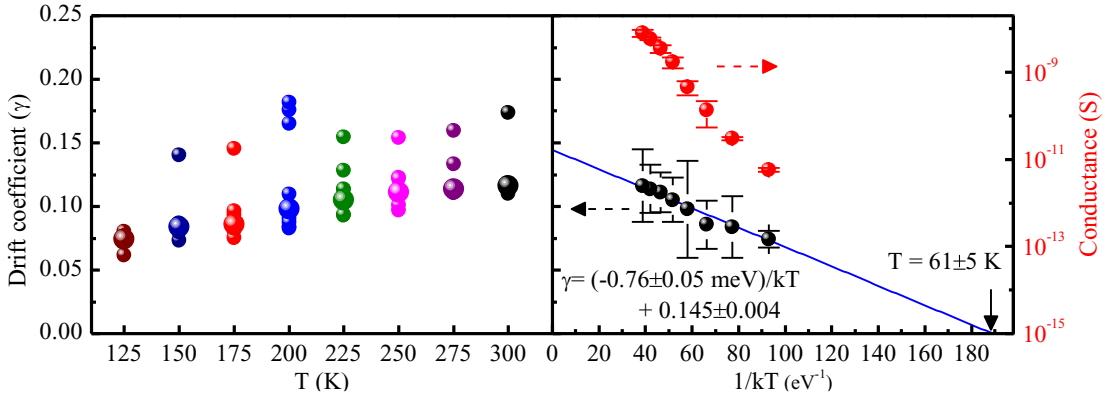

FIG. 7. Drift coefficients at different temperatures extracted from R-t plots (left axis) and corresponding initial conductances (right pane, right axis). Each data point represents the drift coefficient of a different amorphized line cell of similar dimensions (width: ~120-140 nm, length: ~390-500 nm, and thickness: 50 nm), with median values shown with larger markers in the left pane. The median drift coefficients and the associated variations as a function of 1/kT (right pane), show a linearly decreasing trend.

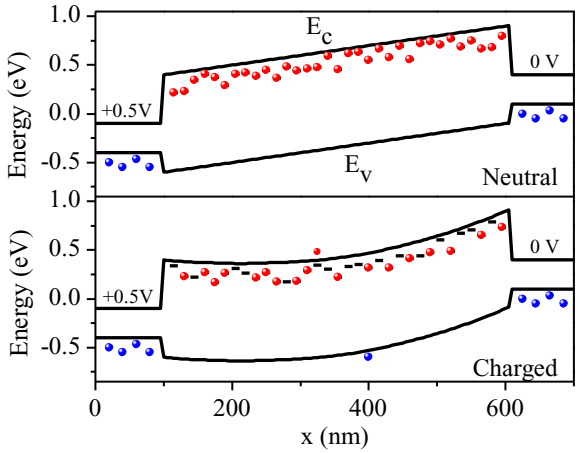

FIG. 8. Energy band diagrams for an amorphized GST wire between hcp-GST regions soon after reset, that is assumed to be charge neutral (top) and with positive fixed charges after activation of the 50% of the electrons (●) from the electron-traps (bottom). Diagrams are shown with 0.5 V bias applied between the two hcp-GST regions serving as contacts. Growth of the crested barrier seen by the holes (●) suppresses the hole current through the amorphous region, observed as resistance drift, while the electrons are better confined within the amorphous region with the evolving potential profile. Band calculations are based on a 1-D model that assumes capacitive coupling only to the two contacts[25–27]. The shown crested barrier is a result of a single positive charge for every ~ 30 nm along the wire.

$\gamma \sim 0.11$ at 300 K to $\gamma \sim 0.07$ at 125 K[22] with device-to-device fluctuations, which we attribute to local variations within the amorphized regions of the cells[23,24] (FIG. 7 left). Median γ values versus 1/kT show a clear linearly decreasing trend, reaching $\gamma = 0$ at $T = 61 \pm 5$ K (FIG. 7 right).

Amorphous phase change materials are known to have a large density of charge traps in their band-gaps[6]. While the hole-traps are assumed to release and trap holes, giving rise to p-type conduction, the electron-traps that release electrons are positively charged and cannot recapture electrons in absence of optical excitation or substantial thermal activation. The ionized electron-traps[19] increase the local electrostatic potential between the two p-type (hcp-GST) contacts[20]. The slow-release of electrons from the electron-traps over time gives rise to gradual growth of a crested barrier[28] for holes (FIG. 8), increasing the observed device resistance. Charging is expected to slow down in time as the shallower traps are more likely to be activated first and the growing electrostatic potential forms an electron-well, increasing the probability of re-trapping of free electrons.

If charging of the electron-traps plays a significant role in the resistance drift of amorphized cells, a response to photoexcitation is to be expected. In order to observe the effect of photo-excitation, a white LED (5 mm round top, driven at rated voltage 3.2 V and current 20 mA, color temperature 6000-9000 K, peak wavelength ~450 nm) was installed inside the cryogenic chamber, controlled by the Arduino microcontroller. A low-power LED was used for low-level photoexcitation, without causing any appreciable thermal disturbance on the measured devices[29]. The thermal relaxation timescales (~10^{-7}-10^{-6} s)[7] and the RC time-constants associated with the electrical setup (~ 10^{-8} s) are

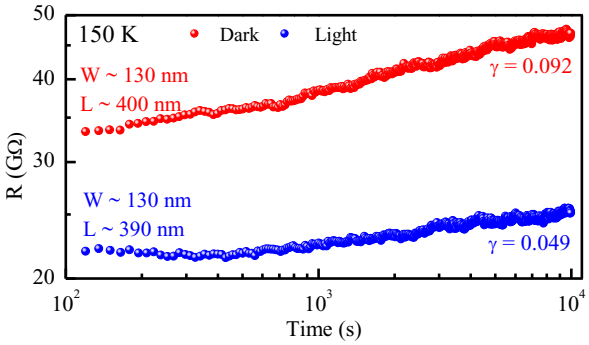

FIG. 9. Resistance versus time for two different line cells amorphized and monitored under dark and light at 150 K.

much smaller than the switching time-scale of the LED (~10^{-1} s) and the measurement time-scale (~15 s). Hence, the observed transient effects are not due to the thermal or electrical response of the measurement setup.

During the LED on versus off experiments, two effects of light were observed: (i) electrical conductivity is higher under light, which is expected as amorphous GST (a-GST) is a semiconductor, (ii) line-cells amorphized and monitored under light showed significantly smaller drift than cells amorphized and monitored under dark (FIG. 9). We did not observe any response to photoexcitation in crystalline cells.

In a second set of experiments, the LED was periodically switched on and off, soon after amorphization at various temperatures (FIG. 10, 11). The relative effect of light is clearly observable for $T \leq 250\ K$ (FIG. 10). The similar R-time behavior each time light is turned on and continuation of the characteristic drift trend each time light is turned off (higher drift coefficient in dark) (FIG. 11e) suggests that light does not induce any permanent changes. Lower resistance at the beginning of each dark interval compared to that at the end of the previous dark interval indicates a partial re-initiation of the resistance drift by light. In the 30 minutes on and off durations measurements performed at 150 K, the resistance is observed to converge to a final value in ~10 minutes when the light is turned on and to a resistance drift trajectory in ~10 minutes when the light is turned off (FIG. 11e). A fast

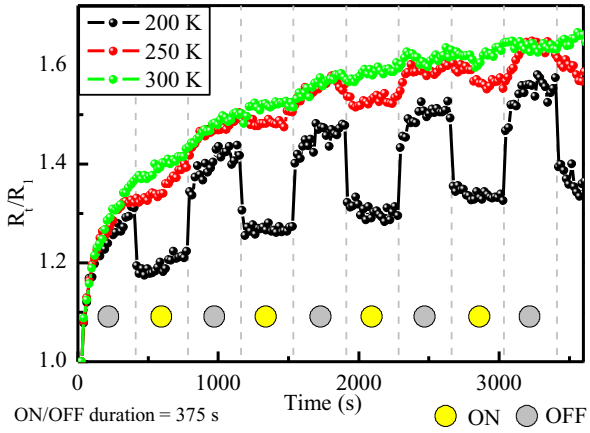

FIG. 10. Effect of light on the ratio of resistance at time t (R_t) to first measured resistance after amorphization (R_1) versus time at different temperatures for three different cells. As the temperature increases, the effect of light reduces. W x L x th = 150 nm x 500 nm x 50 nm.

response (decrease/increase) followed by a gradual change in resistance was observed as the light was turned on and off (decrease/increase). The fast changes in resistance can be attributed to photo-excited charge carriers. The gradual changes that follow point to charging of the amorphous GST, changing the barrier height seen by the holes at the contact regions[30–32] (FIG. 8). This extremely slow response suggests presence of slow trap-to-trap transitions similar to what is expected to give rise to phosphorescence[33] observed in high trap-density material systems. While photoexcitation increases the emission rate of the trapped charges in amorphous GST and band-to-band generation rate, it also

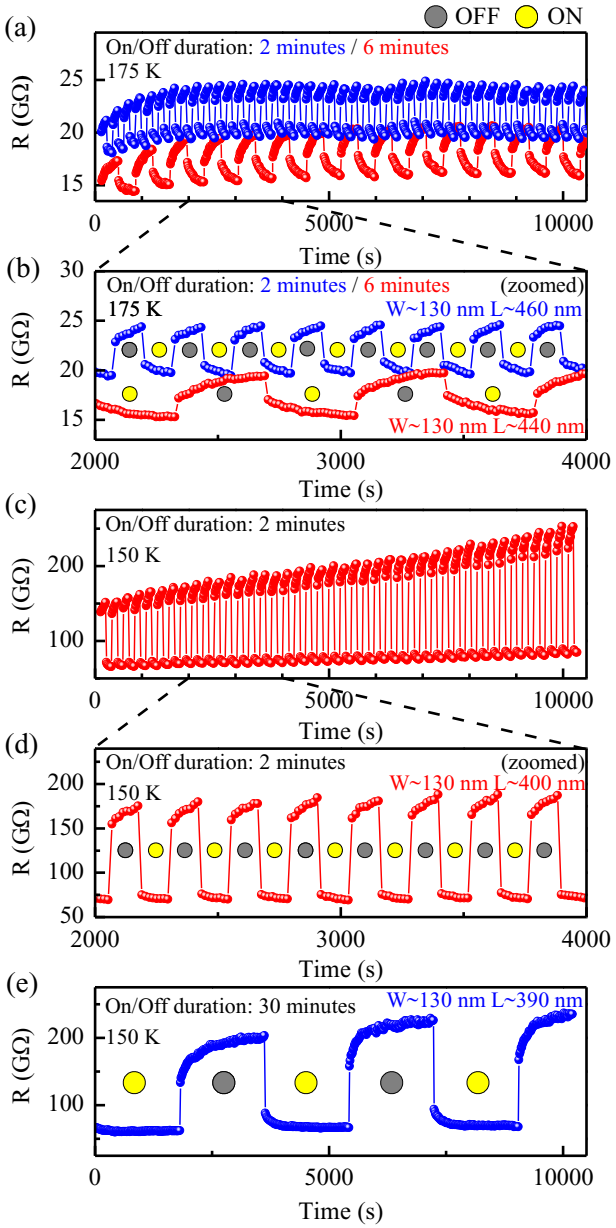

FIG. 11. Resistance versus time plots at 175 K (a, b) and 150 K (c, d, e) for different periods of photo-excitation using LED. The yellow (gray) circle indicates the LED being on (off) during that period. At both temperatures we observe a fast change in resistance followed by a slow response when the LED is switched on/off.

increases the electron and hole injection rates from the degenerately p-type hcp-GST contact regions into the lightly p-type amorphous region[27], establishing a new charge balance. Since the band-gap is expected to increase with reduced temperature, the trap activation energies, as well as the activation energy associated with thermionic emission of carriers over the barriers at the contacts, are also expected to increase. This, combined with reduced kinetic energy at lower temperatures, would give rise to slower charge emission from electron-traps and from the amorphous region to the hcp contact regions, and hence lower drift coefficients. The reduced hole emission rate from the contacts to the amorphous region also leads to increased resistance and further deviation from linear current-voltage (Ohmic) characteristics at higher voltages[22].

The impact of charging on the device resistance may be compounded with the effects of structural relaxation and crystallization[20], especially at higher temperatures. Structural relaxation[34], a thermally activated viscoelastic deformation of the bond network that changes the bond structure and arrangement of the atoms[17,35], is expected to give rise to defect annihilation[17] and increased band-gap[36,37] in amorphous phase change materials, leading to resistance drift. Structural relaxation, and viscosity, are very strong functions of temperature[10,35,38]. However, earlier studies suggest that resistance drift may have no or small temperature sensitivity if the activation energies related to structural relaxation are balanced by the activation energies of holes from hole-traps within the amorphous material[11]. If the linearly decreasing trend we observe in γ versus 1/kT (FIG. 7 right) continues in the lower temperatures, all processes contributing to resistance drift is expected to be quenched at $T = 61 \pm 5$ K.

In summary, amorphized GST line cells continue to display resistance drift between 300 K and 125 K, the full range of temperature used in these experiments, with γ linearly decreasing as a function of 1/kT, suggesting continuation of resistance drift down to $T \sim 61$ K for amorphous GST. The effects of photoexcitation are clearly observable at $T \leq 250\ K$. Experiments with periodic exposure to light show a fast and a slow response. While photo-generated carriers are expected to drive the fast response, electron confinement within the charged amorphous region and very slow trap-to-trap charge exchanges may be giving rise to the slow response (~10 minutes at 150 K). These results support a device-level explanation of resistance drift based on gradual ionization of the electron-traps over time giving rise to an increasing potential barrier seen by the holes at the contacts. It is possible to significantly accelerate resistance drift and stabilize cell resistances with application of large electric fields[22], which can also be explained with the electronic model we discuss in this work. The impact of charging on the device resistance may be compounded with the effects of structural relaxation, annealing of the defects and crystallization. If the electronic mechanisms we discuss here are the dominant contributions for resistance drift up to ~ 100 C, resistance drift in phase-change memory devices can be mitigated by waveform engineering[22], enabling reliable multi-bit-per-cell storage without altering the existing device structures.

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Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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