Low Power and Compact Silicon Thermo-Optic Switch Based on Suspended Phase Arm Without Support Beams

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***Abstract*— A low power and compact thermo-optic switch based on 1 × 1 Mach-Zehnder interferometer structure is demonstrated with the thermal isolation structure fabricated with a new backside etching process. The adjacent SiO_2 and underlying silicon around phase arm are removed to suppress the thermal diffusion. Benefiting from the backside anisotropic etching process and front protecting photoresist used in underlying silicon removal, there are no support SiO_2 beams in air trenches avoiding about 10% of extra thermal diffusion. At 1550 nm for TE mode, a low switching power (P_π) 0.48 mW is obtained with 450 μm thermo-optic interaction length (L_{TO}) representing a $P_\pi \cdot L_{TO}$ product of only 0.22 mW·mm, indicating a high thermal efficiency with a compact footprint. The 10% - 90% response time of the switch is 530 μs, including a rise time of 150 μs, and a fall time of 380 μs. Compared with the switch without isolation structure, the switching power of the proposed switch is reduced more than 17 times, needing only 5.6% of the original value.**

***Index Terms*— Integrated optics, optical switches, thermo-optical materials.**

I. Introduction

THERE are considerable interests in fabricating compact low power optical switches for their wide use in cross-connect and wavelength division multiplexing applications [1], [2]. Silicon-on-insulator (SOI) is a promising platform for its compatibility with complementary-metal-oxide-semiconductor (CMOS) processes, and various optical devices have been fabricated based on the SOI [3], [4]. Silicon is suitable for optical switch fabrication, due to its large thermo-optic coefficient of 1.86×10^{-4}/K [5], which represents the changing of refractive index as a function of temperature. High-density integration and low power consumption have been considered as two key requirements of optical switches.

Various 1 × 1, 1 × 2, and 2 × 2 thermo-optic switches have been demonstrated. Compared with resonant switches [6], [7], nonresonant switches [8], [9] are insensitive to wavelength and could be used in broadband. Several works have been reported on thermo-optic switches based on Mach-Zehnder interferometer (MZI) for its broadband operation and high fabrication tolerance [8]. The high thermal conductivities of silicon (150 W/mK) and SiO_2 (7.6 W/mK) [10] around phase arm cause thermal diffusion, therefore tens of mW power are needed to realize a π phase shift [9], [11]. Replacing the silicon and SiO_2 with air cavities (0.026 W/mK) [12] is an efficient way to suppress the thermal diffusion. In a typical MZI thermo-optic switch, a π phase shift is introduced by heating the phase arm to realize switching. The phase shift ($\Delta\varphi$) of the MZI is calculated as follows:

$$\Delta\varphi = \frac{2\pi}{\lambda}\left(\frac{\partial N_{eff}}{\partial T}\right)\Delta T \cdot L_{TO} \quad (1)$$

N_{eff} is mode effective index in waveguide, ΔT is the temperature change of the phase arm, L_{TO} is the interaction length of light and heater, for the folded phase arm, the L_{TO} is several times as long as heaters. The longer L_{TO} causes the larger footprint. For a highly efficient and compact thermo-optic switch, realizing a low P_π with short L_{TO} is desired. A Figure Of Merit (FOM) is proposed in this work as FOM $= P_\pi \cdot L_{TO}$ (mW·mm). As per our definition, a better FOM is a smaller FOM, which means a smaller power length product. This means that the switch can realize low-power switching with a short interaction length between light and heater.

Several schemes have been proposed to realize low power compact thermo-optic switches. For example, doped silicon heaters [13] can be used to directly heat up the phase arm. Its P_π is 12.7 mW with L_{TO} of 0.01 mm. A spiral-path MZI with folded heaters [14] was designed to utilize the heat diffused laterally. The P_π was down to 6.5 mW. Suspended phase arm [15], [16] was demonstrated as the most effective structure to reduce the power consumption to date. Qing Fang *et al.* suspended the MZI phase arm by removing the adjacent SiO_2 and 120 μm underlying silicon [15], realizing a low P_π of 0.49 mW with L_{TO} of 1 mm. On this basis, Zeqin

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Lu combined folded waveguides and Michelson interferometer (MI) [16] with 6 mm length of L_{TO} to achieve a P_π of only 50 μW, which is the lowest P_π of thermo-optic switches to our knowledge. According to the above, the thermo-optic switches with suspended phase arm can achieve a better FOM for the efficient thermal isolation. Whereas in these applications [15], [16], there are several SiO_2 beams left in air trenches (ATes) to support the suspended phase arms due to the sequentially isotropic dry etching used in underlying silicon removal (USR). These SiO_2 beams would deteriorate the thermal efficiency of switch due to the thermal leakage through them. Therefore, longer phase arm or folded waveguide were designed to achieve lower P_π, causing a bad FOM (larger power-length product). A thermo-optic switch without SiO_2 support beams should be designed to solve this problem.

In this article, we propose and fabricate a low power and compact 1×1 MZI thermo-optic switch with suspended phase arms. The support SiO_2 beams in ATes are no longer needed benefiting from the backside etching process. Different from other works, the adjacent SiO_2 and underlying silicon are removed by an anisotropic etching process separately. The underlying silicon is etched from backside with the chip facing down. In USR, the phase arms are protected by the front protecting photoresist instead of the SiO_2 beams in ATes. Without support SiO_2 beams, the thermal diffusion can be suppressed further. Our thermo-optic switch realizes an ultra-low P_π of 0.48 mW with L_{TO} of 450 μm, representing FOM of only 0.22 mW·mm.

In order to characterize the thermal efficiency and compactness of the proposed switch, the FOM and P_π of different thermo-optic switches are compared in Table 1. The FOM in [19] is as low as 0.054 mW·mm. This value is an order of magnitude better than all other works. This obvious improvement benefits from the thinner BOX of 1 μm used in that work, rather than thermal isolation structure. The buried oxide (BOX) thickness has a great influence on the P_π. The thinner BOX can make smaller cross-section of suspended phase arm, which can maximize the temperature rise leading to smaller P_π. Whereas in common SOI substrate the BOX thickness is 2 - 3 μm to reduce optical coupling to the substrate. In [13], the integrated silicon heater can realize a better FOM (smaller power-length product) by direct heating, whereas the P_π is large due to the thermal diffusion. Compared with other works, the proposed thermo-optic switch can achieve better FOM, benefiting from no SiO_2 support beams in ATes. The heat from the heater can be delivered to the silicon waveguide with lower loss. Lower value of FOM means the proposed switch can realize the same level of P_π in a shorter L_{TO}.

TABLE I

COMPARISONS OF FOM OF DIFFERENT THERMO-OPTIC SWITCHES

Strucutre	FOM = $P_\pi \cdot L_{TO}$ (mW· mm)	P_π (mW)	L_{TO} (mm)	τ (μs)	BOX (μm)
Integrated Si heater [13]	0.127	12.7	0.01	2.4	3
Spiral waveguide [14]	40.95	6.5	6.3	N.A.	2
Suspended MZI [19]	0.054	0.54	0.1	N.A.	**1**
Suspended MZI [15]	0.49	0.49	1	266	2
Suspended MI [20]	2.4	0.4	6	1700	15
Suspended MI [16]	0.3	0.05	6	1280	N.A.
This work	**0**.22	**0**.48	0.45	530	3

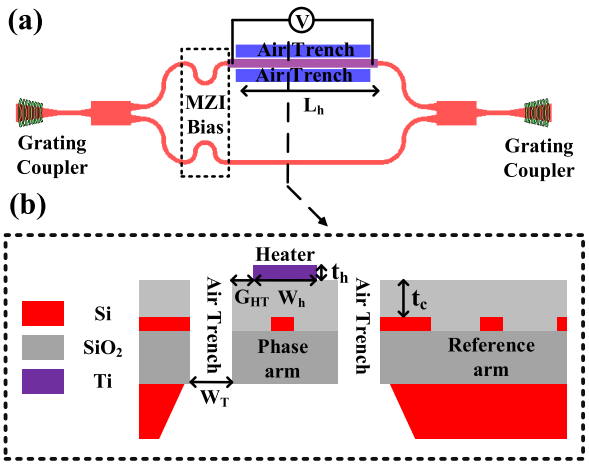

Fig. 1. Schematic of the proposed 1×1 thermo-optic switch: (a) top view, (b) cross-section along cutting line.

II. DEVICE DESIGN AND FABRICATION

The proposed suspended thermo-optic switch is schematically illustrated in Fig.1. Compared with our previous work [17], the USR is introduced to further enhance the thermal efficiency. The switch is designed on an SOI wafer with a 220 nm thick top silicon layer and a 3 μm thick buried oxide layer. In the MZI bias region, 90° phase difference is introduced to insure the MZI working in linear region [18]. The phase arm is isolated by removing the adjacent SiO_2 and underlying silicon. The cross-section of the waveguide is 450 nm × 220 nm. The width (W_h), thickness (t_h), and length (L_h) of the Ti heater are 1.5 μm, 100 nm, and 450 μm, respectively. The width (W_T) and length of ATes are 2 μm and 450 μm, respectively. The gap between heater and ATes (G_{HT}) is 2 μm. The thickness of SiO_2 cladding (t_c) is set to 500 nm to reduce the thermal conduction path from heater to phase arm.

Compared with the works [15], [16], there are no support beams in ATes beside phase arms due to the backside anisotropic etching process used. The widths (W_{Beam}) and intervals (I_{Beam}) of support beams are usually 2 μm to 5 μm and 30 μm to 50 μm, respectively, to prevent the collapse of phase arms. The heat flux through support beams are simulated by 3D HEAT in Lumerial DEVICE Suite. The temperature distribution of phase arm is shown in Fig.2. The W_{Beam}, I_{Beam}, and length of beams (L_{Beam}) are 3 μm, 50 μm, and 3 μm, respectively. It can be seen that the heat in phase arm diffuses through SiO_2 support beams. The inset shows temperature distribution of support beams. When the length of phase arm is 450 μm, the heat flux through support beams is about 11.5% of total heat.

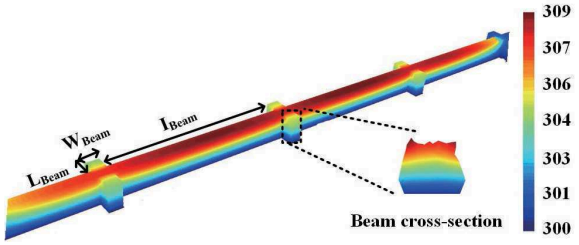

Fig. 2. The temperature distribution of phase arm with SiO_2 support beams in ATes.

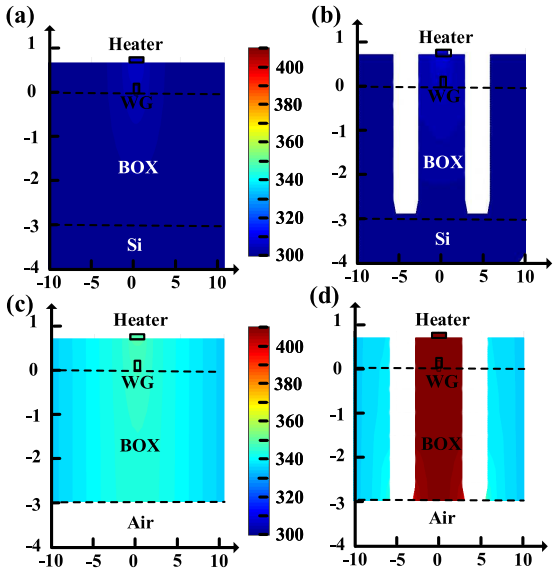

Fig. 3. The temperature distributions of the switches with different thermal isolation structures simulated by Lumerical DEVICE: (a) without thermal isolation structure, (b) with ATes beside phase arm, (c) with USR, and (d) with both ATes and USR.

In order to characterize the thermal efficiency of the proposed switch, the temperature distributions of four switches with different thermal isolation structures were simulated by 2-D Finite-Element simulation in Lumerial DEVICE Suite. The temperature distribution is obtained by solving the heat conduction equation:

$$\rho c_p \frac{\partial T}{\partial t} - \nabla \cdot (k \Delta T) = Q \tag{2}$$

where ρ is mass density, c_p is specific heat, T is temperature, t is time, k is thermal conductivity, and Q is heat energy transfer rate.

Various input powers have been swept, and the results with 5 mW are shown in Figs. 3(a-d). The starting temperature of the SOI substrate is set to 300 K. It can be observed that without thermal isolation structures, the heat diffuses to the whole device and the temperature change of the silicon waveguide is small (about 7 K), whereas with the thermal isolation structure, the heat is confined around the waveguide region creating a high temperature change. Compared Fig. 3(b) with Fig. 3(c), the USR isolates the heat more significantly than the ATes do due to the large thermo-optic coefficient of silicon substrate. Under the same input power, the temperature change of structure in Fig. 3(d) is about 20 times larger than that of structure in Fig. 3(a). Therefore, the switch with thermal isolation structure can work more efficiently.

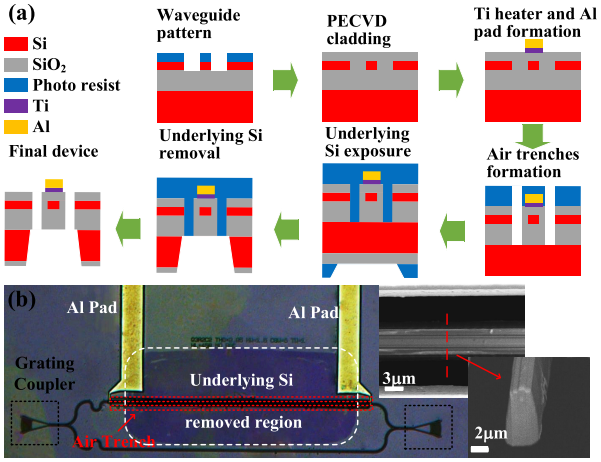

Fig. 4. (a) The main fabrication processes of the proposed thermo-optic switch, (b) images of fabricated thermo-optic switch.

The devices were fabricated at the Center for Advanced Electronic Materials and Devices (AEMD), China. The main fabrication steps are shown in Fig. 4(a). Firstly, the 720 μm SOI wafer was ground to 300 μm from the backside by Disco BG810 to reduce the etching time in USR. Electron-beam lithography (EBL) was used to define the patterns on the CSAR 6200.09 positive resist. Fully-etched (220 nm) waveguides and shallow-etched (70 nm) focusing grating couplers were transferred to the top silicon layer by inductively coupled plasma (ICP) dry etch successively. Then, 500 nm thick SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD) as the upper cladding. 100 nm Ti heater and 700 nm Al pads were sputtered by the multi-target magnetic control sputtering system and defined by lift-off. After that, ATes were patterned by lithography, and etched by dielectric ICP dry etch. Finally, 4 μm thick SiO_2 was deposited on the backside by PECVD as a hard mask at 300°C, and then the front side of the chip was protected by 5 μm thick photoresist. The chip was exposed from the backside by lithography, and underlying silicon was removed by ICP etching using a BOSCH process with the chip facing down. The SiO_2 support beams in ATes were no longer needed due to the phase arms were well supported by the protecting photo resist on the front and the anisotropic etching used in USR. According to the fabrication results, almost all the phase arms are workable, when the length of USR is 420 μm. Fig. 4(b) shows the images of the fabricated thermo-optic switch. The USR region is in a darker color, and its footprint is about 420 μm $\times$ 180 μm. The width of USR region is designed much larger than the width of the phase arm for greater backside etching alignment tolerance. The insets show the SEM images of ATes and suspended phase arm cut by focused ion beam (FIB). The SEM image of suspended phase arm is photographed at 65°. The phase arm is trapezoid. The ATes are about 3 μm wider than the design width caused by the deep etching.

To characterize the devices, an Agilent 81960A tunable laser, and an 81636B power meter were used. TE-polarized light was coupled into/out-of the chip through on-chip focusing polarization-dependent grating couplers. The DC bias was

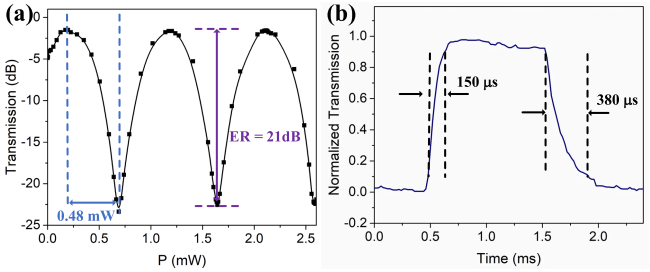

Fig. 5. (a) Transmission for TE mode at 1550 nm as a function of power (the device simulated in Fig. 3d), (b) time-domain response for TE mode at 1550 nm.

applied by a Keithley 2400A dual-channel electronic power source. For the response time (τ) measurement, a GIGOL DF1022U function waveform generator was used to generate a 500 Hz square wave, and a Tektronix CSA7404 was used as the signal analyzer.

III. Result and Discussion

The measured resistance of Ti heater is 6.5 kΩ. Four different thermo-optic MZI switches in simulations have been fabricated. The P_π of the switches without thermal isolation structure, with ATes, with USR, and with both ATes and USR are 8.5 mW, 4.12 mW, 2 mW, and 0.48 mW, respectively. Compared with the thermo-optic switch without isolation structure, the power consumption of the proposed switch with both ATes and USR is reduced more than 17 times, needing only 5.6% of the original value. In accordance with the simulation, USR is more efficient than ATes for thermal isolation.

Fig. 5 shows the measurement results of the proposed thermo-optic switch (the device simulated in Fig. 3d). At 1550 nm with TE polarization input, the transmission as a function of power for the proposed switch is shown in Fig. 5(a). The insertion loss and extinction ratio of the switch are 1.5 dB and 21 dB, respectively. At the origin, the phase difference $\Delta\varphi$ is not equal to 90° due to the fabrication fluctuation of waveguides. The switching power is 0.48 mW. The 10% - 90% response time is 530 μs, which is shown in Fig. 5(b), including a rise time of 150 μs, and a fall time of 380 μs. The thermal isolation structure makes it difficult to dissipate heat, therefore the fall time is much longer than the rise time. The switching power of the proposed switch can be further reduced by using folded waveguide or MI [16] to increase the L_{TO}. Compared with MZI structure, the light looping in MI arms and the length of tunning region is reduced by half.

IV. Conclusion

In conclusion, a low power and compact thermo-optic switch based on an MZI structure is proposed and fabricated with a suspended phase arm. A new backside etching process is applied to remove underlying silicon to release the SiO_2 beams in ATes, which reduces heat loss about 10%. This work defines a new figure of merit FOM to evaluate the design tradeoff in terms of P_π and footprint. The proposed switch can realize a better FOM, benefiting from no support SiO_2 beams in ATes. At 1550 nm, the switching power is 0.48 mW, the 10% - 90% response time is 530 μs, including a rise time of 150 μs, and a fall time of 380 μs, the extinction ratio is 21 dB, and the insertion loss is about 1.5 dB. The power consumption of the proposed switch is reduced more than 17 times, needing only 5.6% of the switch without thermal isolation. The backside etching process can be used in other thermo-optic devices to reduce the switching power.

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