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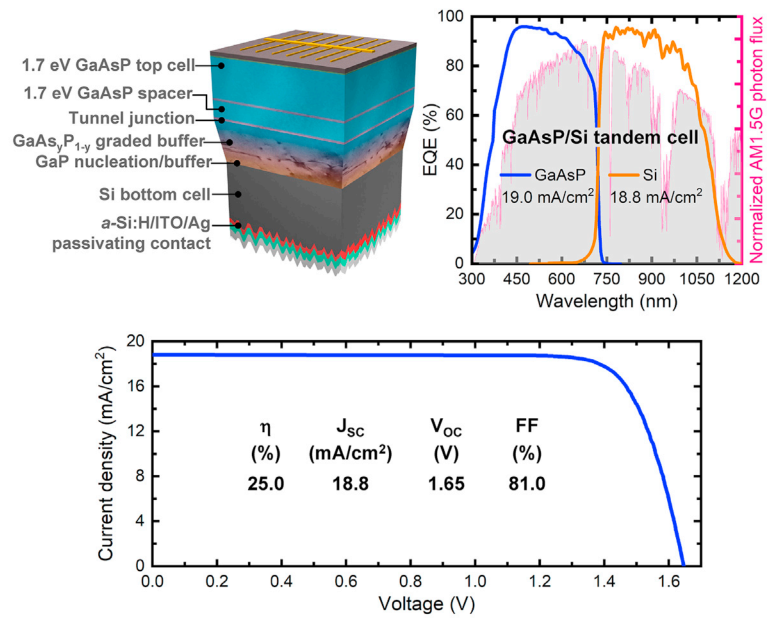

Tandem solar cells consisting of a GaAsP top cell grown on Si can potentially offer an ideal combination of stability and efficiency. However, GaAsP/Si tandem cells are typically hampered by crystalline defects. Improving the quality of interfaces surrounding the GaAsP cell enables Fan et al. to demonstrate a 25% efficient tandem device.

Shizhao Fan, Zhengshan J. Yu, Ryan D. Hool, ..., Yukun Sun, Zachary C. Holman, Minjoo L. Lee

shizhao@illinois.edu (S.F.)
mllee@illinois.edu (M.L.L.)

HIGHLIGHTS

Methods to suppress interfacial defects in GaAsP grown on Si are demonstrated

The reduced defect density enables increased carrier lifetime in the GaAsP

Tandem cell efficiency of 25% validates GaAsP as an efficient and stable partner for Si

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Current-Matched III–V/Si Epitaxial Tandem Solar Cells with 25.0% Efficiency

Shizhao Fan,[1,2,6,*] Zhengshan J. Yu,[3] Ryan D. Hool,[1,2,4] Pankul Dhingra,[1] William Weigand,[3] Mijung Kim,[1,2] Erik D. Ratta,[1,2] Brian D. Li,[1,2] Yukun Sun,[1,2,5] Zachary C. Holman,[3] and Minjoo L. Lee[1,2,*]

SUMMARY

III–V/Si epitaxial tandems with a 1.7-eV GaAsP top cell promise stable power conversion efficiencies above the fundamental limit of Si single-junction cells. However, III–V/Si epitaxial tandems have suffered from limited minority carrier diffusion length in the top cell, leading to reduced short-circuit current densities (J_{SC}) and efficiencies. While conventional wisdom dictates that dislocation density in III–V/Si tandems must be reduced to boost efficiency, here, we show that heterointerface design and growth sequence also play critical roles in reducing recombination losses. Our improved GaAsP cells make use of a wide-band gap AlGaAsP electron-blocking layer that forms a pristine interface with GaAsP, resulting in a 10%–20% (absolute) boost in quantum efficiency over previous work in the critical red wavelength range (600–725 nm), despite similar dislocation density. Combining the improved top cell carrier collection with Si backside texturing, we obtain 25.0% efficient GaAsP/Si tandem cells with a closely matched J_{SC} of 18.8 mA/cm^2.

INTRODUCTION

Pairing wide-band gap (≥1.7 eV) solar cells with market-dominant Si solar cells provides a realistic approach to overcome the 29.4% fundamental efficiency limit of the latter.[1] Boosting the efficiency of photovoltaic modules is a critical lever to reduce overall installed system costs, particularly in area-constrained scenarios.[2] The Lambertian limit of light trapping predicts a theoretical maximal matched short-circuit current density (J_{SC}) of 22.0 mA/cm^2, which is half that of a Si single-junction cell, under AM 1.5 G irradiation conditions for an ideal top-cell band gap energy (E_g) of 1.717 eV.[3,4] However, the reduction of thermalization loss by the wide-band gap top cell promises a 2-terminal tandem open-circuit voltage (V_{OC}) >2 times higher compared to a Si single-junction cell, leading to a theoretical efficiency >40%.[4,5] Stacking 2 junctions above Si to form a triple-junction cell adds complexity but can enable even higher efficiency; hereafter, 2-junction cells will be referred to as tandem cells. State-of-the-art perovskite/Si tandem cells with a top cell E_g of 1.63–1.67 eV have demonstrated J_{SC}s of 19.0–19.5 mA/cm^2, with efficiencies of 25.0%–27.0%[6–13]; the world record efficiency has reached 29.1%.[14] While improving the stability of perovskite top cells is an active area of research,[15] the long-term reliability of III–V cells is well established.[16,17] The combination of GaInP/(Al)GaAs tandem cells and Si solar cells by bonding[18,19] and by mechanical[20,21] stacking has demonstrated higher efficiencies of 34.1% and 35.9%, respectively. The high cost of GaAs wafers and the added processing complexity from bonding/stacking procedures motivate the investigation of direct epitaxial deposition of III–V cells on Si substrates.

[1]Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA

[2]Holonyak Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA

[3]School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ 85287, USA

[4]Department of Materials Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801, USA

[5]Department of Electrical Engineering, Yale University, New Haven, CT 06511, USA

[6]Lead Contact

*Correspondence: shizhao@illinois.edu (S.F.), mllee@illinois.edu (M.L.L.)

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Table 1. LIV Parameters of GaAsP/Si Tandem Cells in This Work and Prior Work

Label	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	η (%)	Type of measurement
This work	18.8 ± 0.41	1.646 ± 0.01	81.0 ± 1.0	25.0 ± 1.0	In-house
Prior work[23]	15.9 ± 0.21	1.629 ± 0.01	77.0 ± 0.3	20.0 ± 0.3	Certified
Prior record[22]	16.7	1.663	78.2	21.8	In-house

J_{SC}, V_{OC}, FF, and η represent short-circuit current density, open-circuit voltage, fill factor, and AM 1.5 G efficiency, respectively. The 25.0% efficient cell in this work was measured in-house under a single-source solar simulator.

Recently heteroepitaxial III–V/Si integration has achieved 21.8% efficiency for 1.7 eV $GaAs_{0.75}P_{0.25}$/Si (hereafter GaAsP/Si) tandem cells[22] and 24.3% for 1.9 eV $Ga_{0.51}In_{0.49}P$/1.4 eV GaAs/Si triple-junction cells.[18] The main strength of the tandem over the triple-junction cell is its relative simplicity and lower lattice mismatch to Si (3.1% for $GaAs_{0.75}P_{0.25}$ versus 4.0% for GaAs). However, the efficiency of the 21.8% efficient champion GaAsP/Si tandem cell was limited by the low J_{SC} of 16.7 mA/cm[2,22] (Table 1, entry 3), which is far from the theoretical maximum of 22.0 mA/cm^2. We previously demonstrated a 20.0%- efficient GaAsP/Si tandem cell with a J_{SC} of 15.9 mA/cm^2 that was limited by the GaAsP top cell.[23] In the same work, we reported a separately fabricated Si bottom cell with a 1.7-eV GaAsP optical filter, showing that backside texturing together with *a*-Si:H passivation can enable a bottom cell J_{SC} of 20.1 mA/cm^2. Given this high value, the critical next step toward current-matched operation and higher tandem efficiency is to raise the J_{SC} of the GaAsP top cell.

The relatively low J_{SC} of GaAsP top cells to date is a direct consequence of poor red response near the band gap energy (600–725 nm wavelengths), resulting from the limited minority electron diffusion length in the thick *p*-GaAsP base layer.[22–26] The external and internal quantum efficiency (EQE and IQE, see Table S2) losses in GaAsP cells are typically attributed to non-radiative recombination at threading dislocations formed from the 3.1% lattice mismatch with the Si substrate. Accordingly, much research in the field has focused on reducing threading dislocation density (TDD) by optimizing the design and growth of the compositionally graded buffer that sits between the Si bottom cell and GaAsP top cell.[25,27] However, even for low-TDD GaAsP cells (TDD = 1–2 × 10^6 cm^{-2}) grown on GaAs substrates with a relatively low lattice mismatch of ~1%,[28,29] the best EQE and IQE values at 650 nm are <80% and <85%, respectively, comparable to GaAsP cells grown on Si with TDD > 5 × 10^6 cm^{-2}.[22–25] The low red response and its insensitivity to TDD suggest that other factors contribute to degraded carrier collection in GaAsP, such as point defects that may arise due to unoptimized growth conditions.[23] Vernon et al.[28] also identified "dark-line defects" in electron beam-induced current (EBIC) mappings of early GaAsP cells grown on GaAs. Considering that EBIC mapping is done under short-circuit conditions, the dark-line defects may also be pertinent to the poor EQE of GaAsP solar cells. Vernon et al.[28] found that the dark-line defect contrast gradually diminished as the graded buffer thickness increased from 1.6 to 14 μm but that growing such a thick layer on Si would lead to severe cracking from thermal mismatch and high growth costs. Methods to reduce local non-radiative recombination at "dark lines" without a drastic increase in III–V layer thickness have not been reported.

In this work, we show that heterointerface design and growth sequence play a major role in recombination losses observed in GaAsP solar cells. We replaced the usual GaInP electron-blocking layer at the back of the cell (i.e., back surface field [BSF] layer) with an AlGaAsP BSF and added a GaAsP spacer layer to put more distance between the cell active region and defects in the graded buffer. Unlike GaInP-GaAsP interfaces, AlGaAsP-GaAsP interfaces are shown to be structurally perfect using transmission electron microscopy (TEM) with a strong reduction in dark-line defects in EBICs. In addition to a 1.8× increase in carrier lifetime, this design change dramatically boosted the red response of the GaAsP cell without reducing TDD. Pairing the improved carrier collection with texturing and *a*-Si:H passivation of the Si back surface, we demonstrated a high-efficiency GaAsP/Si tandem cell with a closely matched J_{SC} of 18.8 mA/cm^2. More generally, our work shows the importance of factors other than TDD in achieving high-efficiency III–V/Si solar cells.

RESULTS AND DISCUSSION

Design of GaAsP Single-Junction Cells and GaAsP/Si Tandem Cells

All of the devices were grown by solid-source molecular beam epitaxy (MBE) on on-axis GaP/Si(001) templates (NAsP$_{III–V}$ GmbH, Marburg, Germany). The substrate temperature (T_{sub}) of the GaAsP top-cell absorber in this work was 625°C,[23] which will be referred to as high temperature (HT). For MBE, a low T_{sub} (e.g., 450°C–500°C) is necessary to attain high doping and to grow (Al)GaInP barrier layers; hereafter, 465°C will be referred to as low temperature (LT), which was used for the GaAsP contact, tunnel junction, GaInP BSF, and AlInP window layer. Due to the 160°C discrepancy in T_{sub}, the use of LT-(Al)GaInP as a barrier layer for HT-GaAsP necessitates a 10- to 12-min growth pause,[30] which can lead to the formation of detrimental interfacial trap states[31]; a 5-nm LT-GaAsP layer is also needed to protect the LT-(Al)GaInP layer during heat-up (see Note S1 and Figure S2). We therefore explored replacing the LT-GaInP BSF with a HT-AlGaAsP BSF while adding a 0.5-μm HT-GaAsP spacer layer beneath the BSF in a growth sequence that avoids T_{sub} changes and growth pauses. GaAsP/AlGaAsP heterojunctions can be grown without interruption while maintaining nearly perfect lattice matching, analogous to GaAs/AlGaAs (further information on GaAsP/AlGaAsP growth and lattice matching can be found in Notes S1 and S2). We conducted X-ray diffraction measurements on GaAsP cells grown on Si with a LT-GaInP BSF and with a HT-AlGaAsP/HT-GaAsP spacer and found that the active regions of both have similar relaxation at room temperature (Figure S3 and Table S1).

Figure 1A shows that the steady-state photoluminescence (PL) intensity of *p*-GaAsP double heterostructures (DHs) with HT-AlGaAsP barriers (DH-1) is 3.0× stronger than its counterpart with LT-GaInP barriers (DH-2), demonstrating the strong effect of heterointerface design and growth sequence on luminescence efficiency. The insets of Figure 1A show that the emission layer in both DHs is 1.2 μm HT *p*-GaAsP doped with a beryllium (Be) concentration of 1×10^{17} cm^{-3} (more details on DH growth can be found in Note S2). Figure 1B likewise shows that the time-resolved PL (TRPL) lifetime increased from 0.86 ns in DH-2 to 1.5 ns in DH-1, despite having nearly identical TDD values of $\sim 7 \times 10^6$ cm^{-2}. The improved TRPL lifetime of *p*-GaAsP (doped at 1×10^{17} cm^{-3}) is comparable to that of *p*-GaAs (doped at 2×10^{17} cm^{-3}) with TDD = 1×10^6 cm^{-2} in the literature.[32]

EQE Improvement in GaAsP Single-Junction Cells Grown on Si

We designed a series of GaAsP single-junction cells on Si to take advantage of the longer TRPL lifetime gained with the HT-AlGaAsP BSF/HT-GaAsP spacer layers. These cells attained a significant increase in red response over earlier cells with a LT-GaInP BSF,[24] boosting J_{SC} by up to 14% (relative to sample A in Figure 2) to 19.3 mA/cm^2. Figures 2A–2D show the layer schematics of samples A–D, all of which possess a nearly identical E_g of 1.69 eV and an absorber thickness of 1.55 μm to

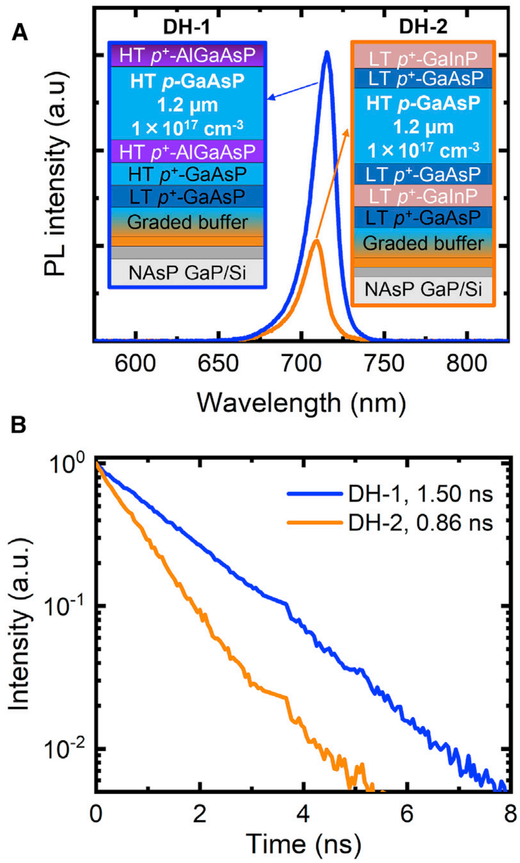

Figure 1. Photoluminescence (PL) Comparison
PL comparison of the Be-doped (1×10^{17} cm^{-3}) p-GaAsP DHs with HT-AlGaAsP (blue) and LT-GaInP (orange) barriers.
(A and B) Steady-state PL spectra (A) and (B) time-resolved PL (TRPL) decays. The insets in (A) show the structural schematics of the 2 DHs, in which the thickness of p-GaAsP emission layers is 1.2 μm.

ensure equal light absorption. Sample A, which has a LT-GaInP BSF, serves as a reference. Sample B includes the HT-AlGaAsP BSF/HT-GaAsP spacer described above, while samples C and D use a 300-nm-thick unintentionally doped GaAsP layer beneath the *n*-GaAsP emitter to further improve carrier collection by increasing the depletion width.[33] In sample D, we replaced the LT-AlInP window layer of samples A–C with a Si-doped *n*-type HT-$Al_xGa_{1-x}AsP$ window layer ($0.34 \leq x \leq 0.8$) with the goal of improving the top interface quality. In comparison with sample A, the $GaAs_yP_{1-y}$ graded buffer thickness in samples B–D is reduced by 1 μm to limit the total thickness of III–V layers to <6 μm, which is sufficient for crack-free GaAsP/Si tandem cells based on our experimental observations.

Comparison of the EBIC maps of samples A and B in Figures 2E and 2F demonstrate that the new cell design leads to a strong reduction in dark-line defects. We observed dark-line defects similar to those shown in Figure 2E in all of our previously reported GaAsP cells grown on GaP/Si templates; the BSF layers of these cells were either p^+-GaAsP grown at identical conditions as the absorber or nominally lattice-matched p^+-LT-GaInP.[25,34,35] We found that the dark-line defect contrast in GaAsP cells diminishes and then disappears as EBIC accelerating voltage decreases from 15 to 5 kV, suggesting that they are related to features at a depth ≥1 μm, and not due to cross-hatch roughness or other surface effects (Figure S4). The dark-line defects

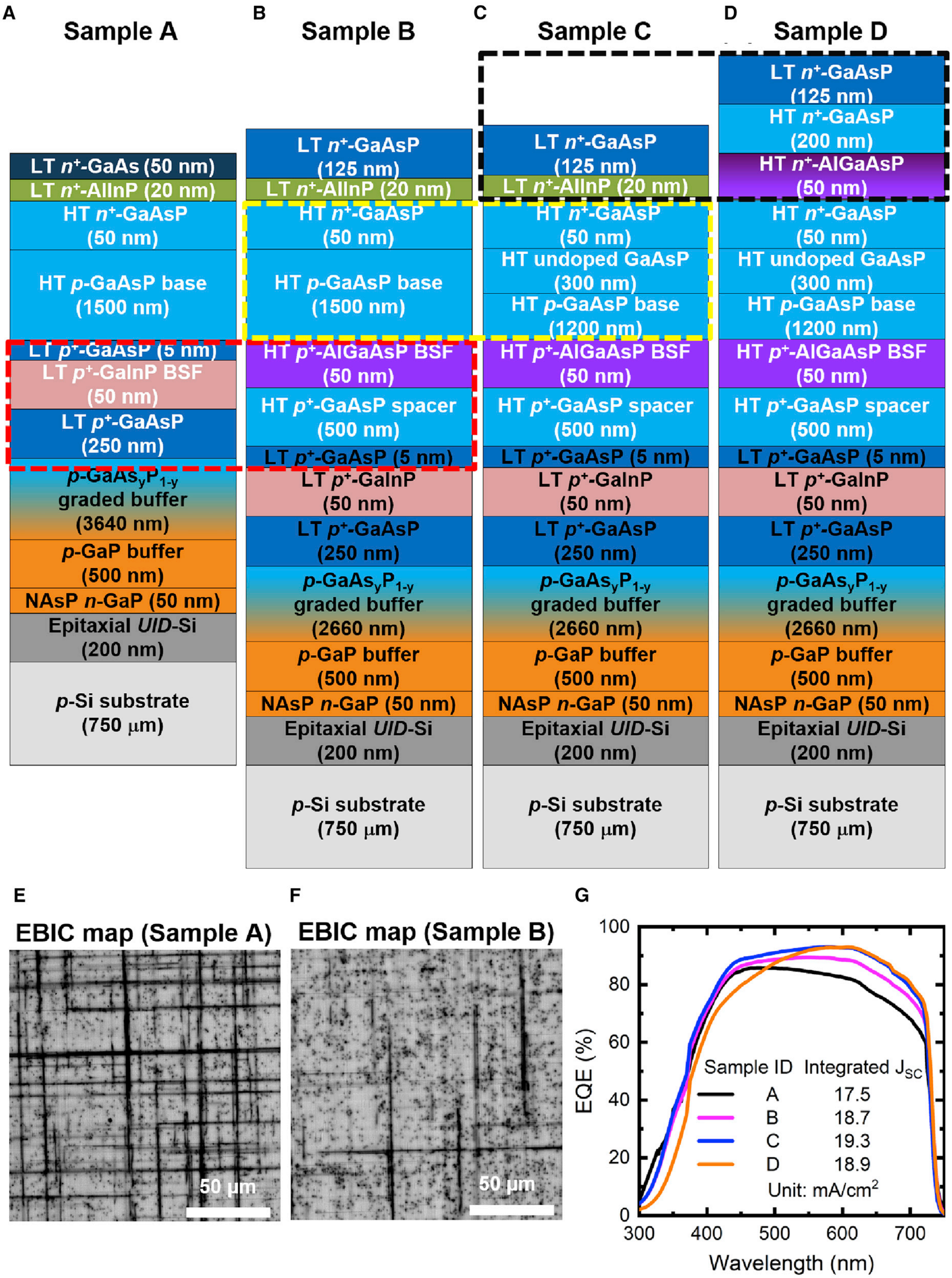
A
Sample A
LT n^+-GaAs (50 nm)
LT n^+-AlInP (20 nm)
HT n^+-GaAsP (50 nm)
HT p-GaAsP base (1500 nm)
LT p^+-GaAsP (5 nm)
LT p^+-GaInP BSF (50 nm)
LT p^+-GaAsP (250 nm)
p-$GaAs_yP_{1-y}$ graded buffer (3640 nm)
p-GaP buffer (500 nm)
NAsP n-GaP (50 nm)
Epitaxial UID-Si (200 nm)
p-Si substrate (750 μm)
B
Sample B
LT n^+-GaAsP (125 nm)
LT n^+-AlInP (20 nm)
HT n^+-GaAsP (50 nm)
HT p-GaAsP base (1500 nm)
HT p^+-AlGaAsP BSF (50 nm)
HT p^+-GaAsP spacer (500 nm)
LT p^+-GaAsP (5 nm)
LT p^+-GaInP (50 nm)
LT p^+-GaAsP (250 nm)
p-$GaAs_yP_{1-y}$ graded buffer (2660 nm)
p-GaP buffer (500 nm)
NAsP n-GaP (50 nm)
Epitaxial UID-Si (200 nm)
p-Si substrate (750 μm)
C
Sample C
LT n^+-GaAsP (125 nm)
LT n^+-AlInP (20 nm)
HT n^+-GaAsP (50 nm)
HT undoped GaAsP (300 nm)
HT p-GaAsP base (1200 nm)
HT p^+-AlGaAsP BSF (50 nm)
HT p^+-GaAsP spacer (500 nm)
LT p^+-GaAsP (5 nm)
LT p^+-GaInP (50 nm)
LT p^+-GaAsP (250 nm)
p-$GaAs_yP_{1-y}$ graded buffer (2660 nm)
p-GaP buffer (500 nm)
NAsP n-GaP (50 nm)
Epitaxial UID-Si (200 nm)
p-Si substrate (750 μm)
D
Sample D
LT n^+-GaAsP (125 nm)
HT n^+-GaAsP (200 nm)
HT n^+-AlGaAsP (50 nm)
HT n^+-GaAsP (50 nm)
HT undoped GaAsP (300 nm)
HT p-GaAsP base (1200 nm)
HT p^+-AlGaAsP BSF (50 nm)
HT p^+-GaAsP spacer (500 nm)
LT p^+-GaAsP (5 nm)
LT p^+-GaInP (50 nm)
LT p^+-GaAsP (250 nm)
p-$GaAs_yP_{1-y}$ graded buffer (2660 nm)
p-GaP buffer (500 nm)
NAsP n-GaP (50 nm)
Epitaxial UID-Si (200 nm)
p-Si substrate (750 μm)
E
EBIC map (Sample A)
50 μm
F
EBIC map (Sample B)
50 μm
G
EQE (%)
Wavelength (nm)
0
20
40
60
80
100
300
400
500
600
700
Sample ID Integrated J_{SC}
A 17.5
B 18.7
C 19.3
D 18.9
Unit: mA/cm^2

Figure 2. Structural Schematics, EBIC Maps, and EQE Comparison of GaAsP Single-Junction Cells on Si

(A) Sample A, our previously reported n^+/p cell with LT-GaInP BSF.[24]

(B) Sample B, n^+/p cell with HT-AlGaAsP BSF/HT-GaAsP spacer.

(C) Sample C, $n^+/i/p$ cell with HT-AlGaAsP BSF/HT-GaAsP spacer.

(D) Sample D, $n^+/i/p$ cell with HT-AlGaAsP BSF/HT-GaAsP spacer and HT-AlGaAsP window layer/HT-GaAsP. The dashed rectangles highlight the structural changes.

(E and F) 12-kV EBIC maps of samples A (E) and B (F), revealing the significant reduction in dark-line defects in sample B. The scale bars have been defined with a known standard specimen in the same field of view.

(G) EQE comparison of samples A–D showing the effect of HT-AlGaAsP BSF/HT-GaAsP spacer and of the $n^+/i/p$ cell structure on carrier collection. The black curve was adapted with permission from Vaisman et al.[24] Copyright (2017) American Chemical Society.

could be related to misfit dislocation bundles[36] from the underlying $GaAs_yP_{1-y}$ graded buffer or misfit dislocations at heterointerfaces between the GaAsP absorber and barrier layers due to unintentional variation in arsenic compositional percentage (%As) and thermal stress effects.[25,34] Samples A and B have dark spot densities (i.e., TDD) of 5.3×10^6 and 7.5×10^6 cm^{-2}, and the slight increase in TDD is consistent with the 1-μm thickness reduction of the $GaAs_yP_{1-y}$ graded buffer in sample B.[25] We believe that both the 0.5-μm-thick HT-GaAsP spacer and the misfit dislocation-free HT-AlGaAsP BSF help to screen defects in the graded buffer and at interfaces and contribute to the ~3× reduction in dark-line defect density (Figure S5). Future studies should aim to better understand and further reduce the formation of dark-line defects and to clarify their effect on minority carrier collection.

The EQE comparison in Figure 2G shows that both the material quality improvement with the HT-AlGaAsP BSF/HT-GaAsP spacer and the $n^+/i/p$ cell structure strongly improve carrier collection. In previous work, we found that increasing T_{sub} for the GaAsP absorber from 585°C to 625°C improved EQE at 450–600 nm by ~5% absolute, potentially due to a reduction in point defects.[23] However, with a conventional LT-GaInP BSF, the EQE at 600–725 nm was insensitive to changes in both the HT-GaAsP absorber thickness and doping profile due to short diffusion lengths.[37] Hovel fittings of EQE in these earlier cells (including sample A) revealed minority electron diffusion lengths (L_n) of 1.1–1.4 μm.[38] In contrast, the EQE at 600–725 nm of sample B (pink) is ~7% (absolute) higher than that of sample A (black), demonstrating the advantage of HT-AlGaAsP/HT-GaAsP over LT-GaInP BSF in minority electron collection. To further improve EQE, we implemented the $n^+/i/p$ cell structure in sample C (blue), leading to another ~5% (absolute) boost at 600–725 nm compared to sample B; Hovel fitting indicated L_n up to 1.85 μm. Samples C and D exhibit identical EQE at 570–750 nm, although the blue response of sample D at 300–570 nm is reduced due to the lower transparency of the AlGaAsP window layer ($E_{g,\ AlGaAsP}$ = 2.18 eV versus $E_{g,\ AlInP}$ = 2.33 eV).[39] We note that the red response in samples B–D was improved over sample A, despite elevated TDD.

Lighted current versus voltage (LIV) parameters in Table 2 show that the HT-AlGaAsP BSF/HT-GaAsP spacer design enables GaAsP single-junction cell efficiencies of 16.6%–17.6%, mainly due to J_{SC} increases of 1.7–2.3 mA/cm^2 compared to the LT-GaInP BSF design. The n^+/p cells (samples A and B) exhibit similar band-gap-voltage offset ($W_{OC} = E_g/q - V_{OC}$) of 0.52–0.53 V. In contrast, the W_{OC} of $n^+/i/p$ cells (samples C and D) is 35 mV higher, indicating higher non-radiative recombination in the wider space charge region due to the 0.3-μm-thick unintentionally doped GaAsP absorber layer. Our single-junction cells are affected by the high sheet resistance of ~400 Ω/*sq* in the p^+-GaAsP rear contact, through which current must flow laterally, leading to diminished fill factor (FF) for larger-area cells (Figure S6). This additional lateral series resistance (R_S) does not apply to two-terminal tandem cells in which current flows vertically through the tunnel junction (Figure S6). We determined R_S in GaAsP single-junction cells from dark current density-voltage characteristics and

Table 2. Comparison of GaAsP Single-Junction Cells on Si in This Work and Prior Work

Sample	J_{SC} (mA/cm^2)	V_{OC} (V)	FF (%)	η (%)	Area (cm^2)	R_S (Ω · cm^2)
A[24]	17.0 ± 0.37	1.157 ± 0.002	77.9 ± 0.4	15.3 ± 0.34	0.039 ± 0.3%	0.45
B	18.7 ± 0.42	1.152 ± 0.003	77.2 ± 0.7	16.7 ± 0.56	0.123 ± 0.2%	1.54
C	19.3 ± 0.42	1.119 ± 0.003	76.6 ± 0.7	16.6 ± 0.56	0.123 ± 0.2%	2.42
D	18.9 ± 0.42	1.127 ± 0.003	82.4 ± 0.7	17.6 ± 0.56	0.044 ± 0.2%	0.37

Note that all of the cells have nearly identical E_g = 1.685 eV. J_{SC}, V_{OC}, FF, η, and R_S represent short-circuit current density, open-circuit voltage, fill factor, AM 1.5 G efficiency, and series resistance, respectively.

observed a correlation between (FF) and R_S in samples A–C (Table 2). To identify the limiting factors of FF, we fitted the suns-V_{OC} characteristics[40] of GaAsP cells on Si using a standard 2-diode model consisting of a parallel combination of a diffusion current-dominated diode (ideality factor n = 1) and a depletion region recombination current-dominated diode (n = 2); the respective saturation current densities are J_{01} and J_{02}.[38] The FF of ~77% is primarily limited by the predominance of the J_{02} component over the J_{01} component.[39] However, we observed a much higher FF in sample D that may be related to a pronounced J_{01} component (not shown here). Further investigation of Al-rich AlGaAsP for better transparency in the window layer and to identify the mechanism for higher FF in HT-AlGaAsP-passivated GaAsP cells could lead to even higher single-junction efficiencies. Regardless, the most important aspect of samples B–D is their high J_{SC} values, capable of closely current matching our previous Si bottom cells.

Improved BSF Interface in GaAsP/Si Tandem Cells

We next performed a cross-sectional TEM (XTEM) study of tandems with top cells following designs A and B to better understand the benefits of the HT-AlGaAsP BSF/HT-GaAsP spacer design. At a length scale of 3–10 μm (the image width in XTEM), it can be seen that switching from a conventional LT-GaInP BSF layer grown directly on the tunnel junction (Figure 3A, sample E) to a HT-AlGaAsP BSF with a HT-GaAsP spacer (Figure 3B, sample F) reduces the density of misfit dislocations at the BSF-absorber interfaces. The XTEM image in Figure 3C, with a layer-to-layer correspondence to the schematic in Figure 3B, illustrates how the HT-GaAsP spacer separates the GaAsP top cell from the underlying dislocation-rich $GaAs_yP_{1-y}$ graded buffer. Figure 3D shows that in sample E, misfit dislocations (indicated by white arrows) formed both above and below the LT-GaInP BSF. The lateral spacing of misfit dislocations was highly heterogeneous, ranging from 0.1 μm to a few microns apart. A possible mechanism for misfit dislocation formation could be that unintentional variation of %As in the LT-GaAsP/AlGaAsP tunnel junction layers causes lattice mismatch with the LT-GaInP layer. In addition, thermal cycling from the graded buffer growth conditions (T_{sub} = 595°C) down to those of the tunnel junction/GaInP BSF (T_{sub} = 465°C) and back up to those of the active region (T_{sub} = 625°C) promotes the motion of threading dislocations, and the different dislocation glide velocities in GaInP and GaAsP could lead to misfit dislocations at the interfaces.[41,42] In contrast, Figure 3E shows that switching to the HT-AlGaAsP BSF/HT-GaAsP spacer reduces the density of interfacial misfit dislocations, which is consistent with both the improved TRPL lifetime (Figure 1B) and the nearly perfect lattice matching between HT-AlGaAsP and HT-GaAsP (Figure S1); the lower-magnification image in Figure 3F further attests to the lack of interfacial defects at a scale of 3 μm. The dark-line defects

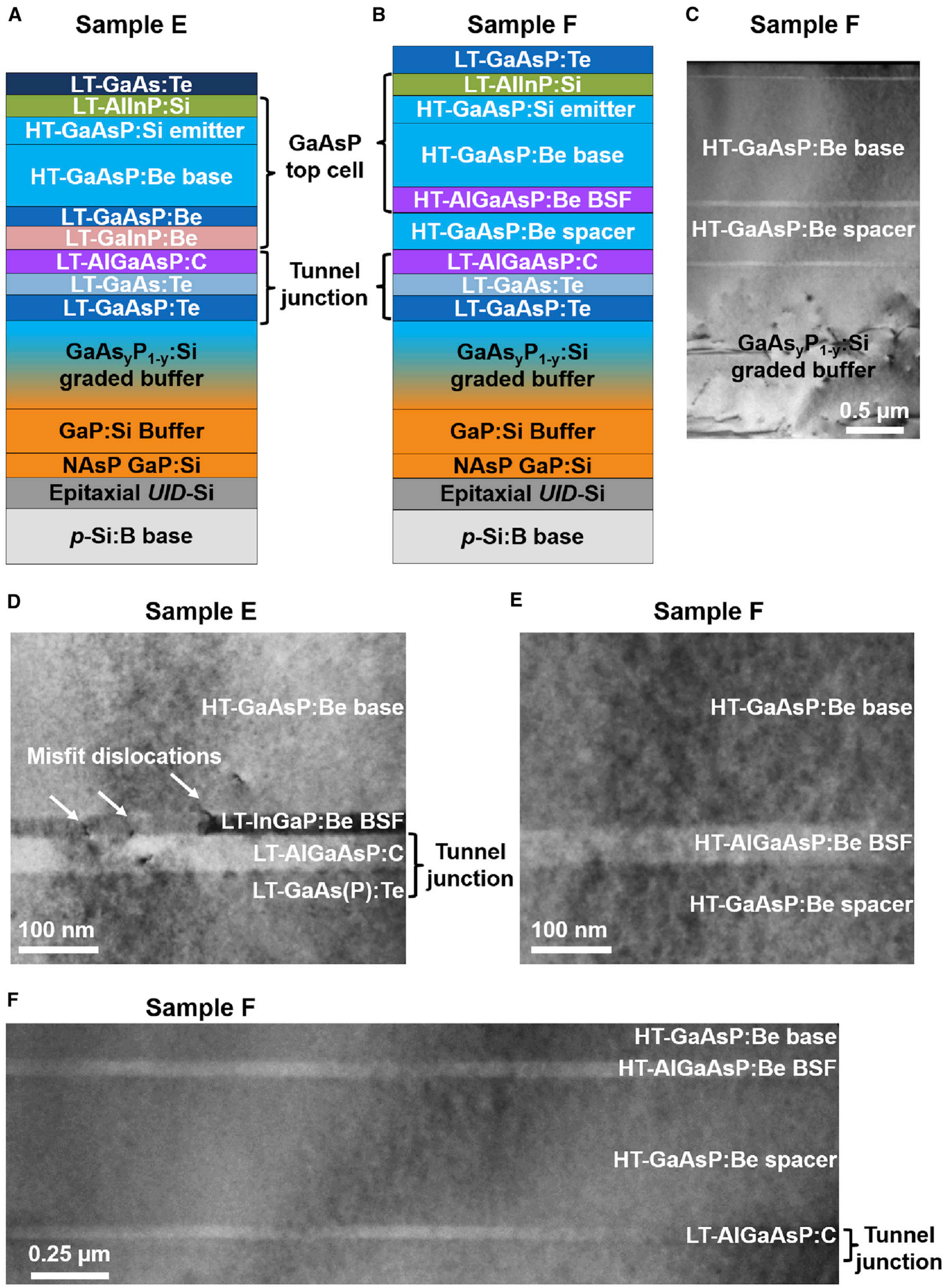

Figure 3. Structural Schematics and XTEM Characterization of GaAsP/Si Tandem Cells

(A and B) The tandem cell with LT-GaInP BSF (sample E) (A) and (B) the tandem cell with HT-AlGaAsP BSF/HT-GaAsP spacer (sample F).
(C) XTEM of sample F shows that the HT-GaAsP spacer separates the GaAsP top cell from dislocations in the GaAs$_y$P$_{1-y}$ graded buffer layers.

(D) High-magnification XTEM of the LT-GaInP BSF region of sample E showing the presence of misfit dislocations (indicated by white arrows).
(E and F) High- (E) and (F) low-magnification XTEM of the HT-AlGaAsP BSF region of sample F showing dislocation-free interfaces.
All of the XTEM images were taken using a g = (004) 2-beam condition. The scale bars have been defined with a known standard specimen in the same field of view.

in our cells may be related to the interfacial misfit dislocations observed in Figure 3D, although their non-uniform distribution and the drastic difference in length scale observed in EBICs versus in XTEM make it difficult to show a definitive correlation.

Understanding the formation of misfit dislocations in III–V devices on Si is an important and ongoing topic of research. Unexpected misfit dislocations in the active regions of GaAs-based lasers on Si were reported at least 5 years ago,[43] and researchers are still working to determine how and why they form, as well as strategies to mitigate them.[44] A recent paper proposed a novel mechanism in which threading dislocations glide in III–V layers on Si during cool-down from growth to room temperature to partially relax thermal mismatch-induced strains.[45] These threading dislocations are speculated to become pinned in In-containing layers due to differences in dislocation glide velocity between different materials (at LT and low residual strain), resulting in the formation of misfit dislocations; similar misfit dislocations were not reported to form at GaAs-AlGaAs interfaces. Future experiments could help to determine whether such a mechanism could account for why misfit dislocations form more readily at GaAsP-GaInP interfaces than at GaAsP-AlGaAsP interfaces in the solar cells investigated in this work. Overall, Selvidge et al.[45] show that misfit dislocations in III–V devices on Si can form through complex and unexpected mechanisms.

25.0% Efficient GaAsP/Si Tandem Cells

We attained 25.0% AM 1.5 G efficiency (in-house measurement under a single-source solar simulator) in a current-matched GaAsP/Si tandem cell by combining the HT-AlGaAsP BSF/HT-GaAsP spacer and improved $n^+/i/p$ top cell design (sample C) with backside texturing, *a*-Si:H passivation, and an indium tin oxide (ITO)/Ag back reflector for the Si bottom cell. Figure 4A shows that the EQE-integrated J_{SC} of the 1.71-eV GaAsP top cell reached 19.0 mA/cm^2, which is slightly higher than that of the Si bottom cell at 18.8 mA/cm^2. Compared to the 20% efficient tandem cell in our prior work,[23] the drastic EQE improvement of 10%–20% (absolute) at 400–700 nm in the GaAsP top cell has transformed the device performance. Although both tandem cells have *a*-Si:H(i)/*a*-Si:H(p)/ITO/Ag passivating back contacts, the tandem cell in this work has the additional benefit of Si backside texturing, leading to an EQE boost of 20%–25% (absolute) at 1,050–1,100 nm, as expected. This gain, together with a slightly lower reflectance at 750–900 nm, increased the EQE-integrated J_{SC} of the Si bottom cell by 1.3 mA/cm^2. As a result, the nearly perfect current matching in the 2 sub-cells boosts the tandem J_{SC} by 2.9 mA/cm^2 compared to our prior work. The LIV results in Figure 4B and Table 1 show that both V_{OC} and FF are improved as well, potentially due to higher minority carrier lifetime in the GaAsP top cell.

We previously identified poor red response of the GaAsP top cell and low V_{OC} of the Si bottom cell ($V_{OC,\ Si}$) as the primary performance bottlenecks in GaAsP/Si tandem cells.[23] While this work has significantly overcome the former limitation, the low $V_{OC,\ Si}$ of ~0.51 V—due to the high GaP/Si interface recombination velocity (>10^5 cm/s)—still impairs the overall efficiency. Almansouri et al.[46] proposed that heavy *n*-type doping of the Si emitter could boost $V_{OC,\ Si}$ by shielding photoexcited carriers from the defective GaP-Si interface (R_{sheet} < 50 Ω/*sq* to obtain $V_{OC,\ Si}$ > 0.6 V; R_{sheet} ~1,600 Ω/*sq* in this work). Feifel et al.[47] demonstrated $V_{OC,\ Si}$ = 0.63 V by the thermal diffusion of P in the *p*-Si wafer (R_{sheet} ~19 Ω/*sq*) before GaP nucleation.

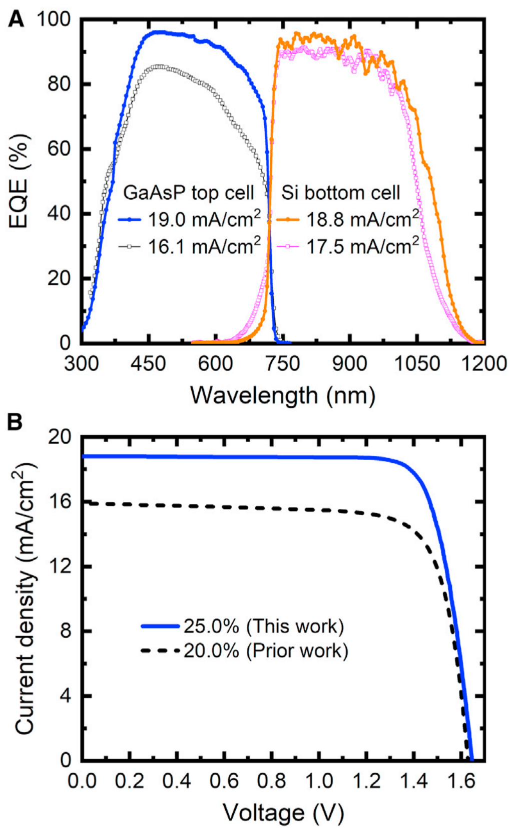

Figure 4. Comparison of Tandem Cell Performance

Comparison of tandem cell performance between the 25.0% efficient GaAsP/Si tandem cell in this work and the 20.0% efficient tandem cell in our prior work.[23]

(A) EQE comparison between this work (blue and orange) and our prior work[23] (gray and pink).

(B) LIV comparison between this work (solid blue) and our prior work (dashed black). Both tandem cells have similar anti-reflection coatings and an identical area of 0.123 cm^2.

The gray and pink curves in (A) and the dashed black curve in (B) were reprinted from Fan et al.[23] Copyright (2019), with permission from Elsevier.

Future implementation of such a high-V_{OC} Si bottom cell into our GaAsP/Si tandem cell could lead to a tandem V_{OC} of 1.77 V and an AM 1.5 G efficiency of 27.0%. While this work has emphasized the importance of factors other than TDD in attaining high efficiency, reductions in TDD will nevertheless play an important role in pushing GaAsP/Si tandems to 30% efficiency and beyond.

We demonstrated that switching the BSF composition and growth sequence led to numerous beneficial effects for MBE-grown 1.7 eV GaAsP solar cells grown on Si. First, the steady-state PL intensity and TRPL lifetime of *p*-GaAsP DHs were increased by 3.0 and 1.8×, respectively. Second, the switch eliminated interfacial misfit dislocations and led to a drastic reduction in dark-line defects in EBIC maps, likely due to improved BSF/absorber lattice matching and increased spacing from the graded buffer. These benefits led to a substantial improvement in the red response of GaAsP top cells. We demonstrated a J_{SC} value of 19.3 mA/cm^2 in a 1.69-eV GaAsP single-junction cell grown on Si together with the $n^+/i/p$ GaAsP cell structure. Finally, we applied the high-J_{SC} GaAsP top cell design into a GaAsP/Si tandem cell with Si backside texturing and passivation, resulting in a closely matched J_{SC} of 18.8 mA/cm^2. Near-term work to reduce recombination losses at the GaP-Si interface could alleviate the voltage bottleneck in our tandem cells and potentially boost the efficiency of GaAsP/Si tandem cells to 27.0%.

EXPERIMENTAL PROCEDURES

Resource Availability

Lead Contact

The Lead Contact is Dr. Shizhao Fan (shizhao@illinois.edu).

Materials Availability

The samples that were grown and processed in this study are being stored at the University of Illinois at Urbana-Champaign for potential future studies.

Data and Code Availability

All data associated with the study are included in the paper and the Supplemental Information. Additional information is available from the Lead Contact upon reasonable request.

GaAsP/Si Tandem Cell Fabrication

Fabrication procedures were identical to our previous publications.[23,39] After III–V growth, the Si substrate was etched to ~200 μm thickness in concentrated (30% by weight) KOH aqueous solution and random pyramid textured in diluted KOH solution (8% by weight) with the addition of a surfactant from GP Solar GmbH. Subsequently, intrinsic (6 nm) and *p*-type (11 nm) amorphous Si (*a*-Si:H) backside passivation and carrier-selective layers were deposited by plasma-enhanced chemical vapor deposition at 250°C for 15 min, and ITO (150 nm)/Ag (200 nm) layers were deposited by sputtering at room temperature, followed by annealing at 200°C for 20 min to cure sputtering damage. Ti (10 nm)/Au (500 nm) front metal grids were deposited after processing the Si back contact. The anti-reflection coatings are either TiO_2 (35 nm)/SiO_2 (70 nm) by sputtering (PVD 75, Kurt J. Lesker Company) or ZnS (30 nm)/MgF_2 (80 nm) by thermal evaporation (NRC Varian 3115 Vacuum Deposition System).

Device Characterization

EBIC maps were collected with a JEOL JSM-6060LV scanning electron microscope using accelerating voltages of 6–12 kV. TDD was estimated by surveying a total area >3×10^4 μm^2. Bright-field TEM was performed using a JEOL 2010 LaB_6. Room temperature steady-state PL was conducted using a 532-nm laser and an Ocean Optics spectrometer. TRPL measurements were conducted using a super-continuum pulsed laser at 633 nm with a time-averaged power of 3 mW, a spot size of 1 mm^2, 6-ps pulses, and a 5.6-MHz laser repetition rate with a single photon detection module (ID Quantique, model no. id100-20). Solar cell measurement procedures can be found in our previous publications.[23,39] EQE was measured using a QE-X7 system from PV Measurements, and LIV measurements were performed in-house with an ABET simulator (single source). Descriptions of the spectral correction procedure for tandem cell measurements as well as error estimations are given in the Supplemental Experimental Procedures, Tables S3 and S4, and Figures S7–S9. LIV measurements from a separate tandem cell of the same sample were verified using a Newport Sol1A solar simulator (model no. 94021A, single -source) with class A spectral match from the Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign; the comparison of verified and in-house measurements is included in Figure S10 and Table S5.

SUPPLEMENTAL INFORMATION

Supplemental Information can be found online at https://doi.org/10.1016/j.xcrp.2020.100208.

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AUTHOR CONTRIBUTIONS

S.F., M.L.L., R.D.H., Z.C.H., and Z.J.Y. designed the experiments. S.F. and M.L.L. designed the MBE growth structures. S.F. and R.D.H. performed MBE growth with assistance from B.D.L. and Y.S. S.F. fabricated the top cells. For the tandem cells, S.F. textured and cleaned the III–V/Si wafers, Z.J.Y. and W.W. fabricated the *a*-Si back contact, and S.F. completed the tandem fabrication. S.F. designed and deposited the anti-reflection coatings. S.F. and M.K. performed the PL and TRPL measurements. S.F. and R.D.H. performed the X-ray diffraction measurements. R.D.H. performed the EBIC characterization. P.D. performed the TEM sample preparation and imaging. S.F. and E.D.R. performed the ellipsometry measurements. S.F. performed the solar cell measurements. S.F. and M.L.L. wrote the paper. S.F., M.L.L., Z.C.H., Z.J.Y., R.D.H., and P.D. discussed the results and revised the manuscript. M.L.L. and Z.C.H. supervised the overall efforts at the University of Illinois and at Arizona State University, respectively.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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