Capacitor Voltage Balancing for Neutral Point Clamped Dual Active Bridge Converters

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***Abstract*—A capacitor voltage balancing method is proposed for a full-bridge neutral point diode clamped (NPC) dual-active bridge (DAB) converter. In existing literature, capacitor voltage balancing is achieved by actively selecting between the small voltage vectors, i.e., connecting either the upper or the lower capacitor on the dc bus to the transformer winding, on the basis of measured voltage mismatch. These balancing methods are dependent on the direction of power flow through the DAB converter. In this work, we propose a voltage balancing controller, which is independent of power flow direction and does not require adjustments of active voltage vectors through the modulator. Irrespective of the direction of transformer current, by dynamically shifting the switching instants of the inner switch pairs in the two NPC legs during the free-wheeling/zero voltage vector time, either of the two capacitors can be selectively charged without introducing any offsets in the voltage-second seen by the transformer. A simple bidirectional phase-shift modulator is designed to facilitate voltage balancing irrespective of power flow direction or mode of operation. The proposed method is highly and universally effective under any converter operating condition and was verified and demonstrated through analysis, simulation, and hardware experiments using a laboratory prototype.**

***Index Terms*—Capacitor voltage balancing, dual active bridge (DAB), neutral point diode clamped (NPC), neutral point balancing.**

I. Introduction

DISTRIBUTED generation, energy storage, and electric vehicle charging applications have reinvigorated the research interest, both in academia and industry, on high power isolated dc–dc converters [1]–[5]. These converters not only provide galvanic isolation, but also enable very high voltage conversion ratios without compromising efficiency. Specifically, dual-active bridge (DAB) converters are a topic of interest due to their versatile features such as bidirectional power flow, inherent soft switching, simplicity of control, and wide voltage ranges [6]–[10]. Bidirectional DAB converters have been used for energy storage and battery charging applications for wide input voltage ranges and large voltage conversion ratios [11]–[17]. In dc microgrids, DABs have been used for interfacing and power flow control among distributed energy resources, energy storage devices, and loads [18]–[20]. For solid-state-transformer applications, DAB converters have been used for galvanic isolation and enhanced efficiency [21]–[23]. For medium voltage applications, especially for modular and/or multilevel topologies, DAB converters are used to achieve multiple isolated dc buses [24]. For instance, for a cascaded H-bridge topology, multiple isolated dc buses can be obtained using DAB converters. By using the neutral point diode clamped (NPC) topology, the DAB can deliver higher dc bus voltage using lower voltage rated power devices [25], [26]. NPC-based DAB converters have been proposed for reaching higher dc bus voltage and enhancing efficiency over a wider range of operating voltages [27]–[32].

Despite the advantage of supplying a dc-bus at near-twice the blocking voltage of its semiconductors, NPC topology requires explicit control strategy for balancing dc bus capacitor voltages [33], [34]. As the power devices are rated to block half of the dc-bus voltage, a growing voltage imbalance between the upper and lower bus capacitors leads to overvoltage stress on power devices despite closed-loop regulation of total dc bus voltage at the rated value and may cause device failure in extreme cases. Furthermore, less severe voltage imbalance for extended period of time causes uneven stress on the bus capacitors and power devices, which may lead to early failure of components. Several capacitor voltage balancing methods have been proposed for NPC-based DAB converters. In [29]–[31], for a three-level NPC-based DAB converter, the authors dynamically adjust the active voltage vectors based on the measured voltage imbalance and the direction of power flow. In [32], a dc blocking capacitor is used, which allows the NPC-based full-bridge to apply asymmetric voltage pulses across the transformer terminal without causing magnetic saturation in the transformer. In the full-bridge NPC topology, each small voltage vector can be generated using either of the upper and lower capacitor of the dc bus. The authors use the two alternative switching combinations for each small voltage vector in successive switching periods to generate neutral point current; consequently, the neutral point voltage fluctuates periodically around the desired value, i.e., half of the dc bus voltage [32].

In this article, we propose a capacitor voltage balancing method that does not require active manipulation of small

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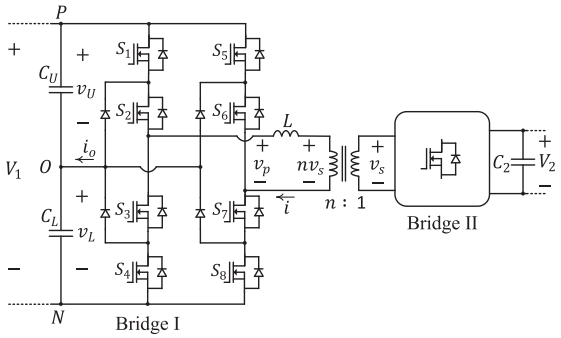

Fig. 1. DAB converter using full-bridge NPC topology.

voltage vectors by the modulator and is insensitive to power flow direction through the DAB converter. Through the conduction path analysis, we show that by adjusting the switching instants of the inner switch pairs of the two NPC legs during the free-wheeling/zero voltage vector time, each of the upper and lower capacitors can be selectively charged irrespective of the power flow direction. Moreover, the proposed method does not produce any offset in the voltage pulses applied across the transformer terminals, which helps avoid magnetic saturation.

The rest of the article is organized as follows. First, the full-bridge NPC-based DAB converter is described. Second, the proposed capacitor voltage balancing method is presented. Third, the balancing charge and balancing power that can be generated by the proposed balancing controller at various operating conditions are quantified through analysis. Through detailed switching model simulation, the balancing power over the entire operating range of voltage ratio and power flow is determined. Fourth, a bidirectional phase-shift modulator (BPSM) with the proposed voltage balancing control is described. Finally, the experimental results are presented to validate the proposed method.

II. System Description

A bidirectional DAB converter is shown in Fig. 1. On the primary side, the full-bridge, denoted as Bridge I, is implemented using the NPC topology. The NPC topology enables reaching a higher dc bus voltage using lower voltage rated semiconductor devices. Bridge II, on the secondary side, may be implemented using a full H-bridge or an NPC-based full-bridge topology. The dc bus voltages of Bridges I and II are denoted as V_1 and V_2, respectively; and v_U and v_L represent the voltages across the upper and lower capacitors C_U and C_L, respectively. The transformer leakage inductance (including any external inductance) is denoted as L and n represents the transformer turns-ratio. Each terminal of the transformer winding, on the primary side, can be connected to the positive point P, negative point N, or the mid-point/neutral point O of the dc bus. Using different switching combinations on the two NPC legs of Bridge I, five-level voltages, such as $v_p \in \{-V_1, -V_1/2, 0, +V_1/2, +V_1\} \equiv$ {NP, NO/OP, NN/OO/PP, ON/PO, PN}, can be generated across the primary winding of the medium frequency transformer (MFT). For simplicity, we consider double phase shift modulation using three-level voltages across the MFT, i.e., $v_p \in \{-V_1, 0, +V_1\}$ and $v_s \in \{-V_2, 0, +V_2\}$. For converter operation using three-level voltage, excluding the small voltage vectors, i.e., $\{-V_1/2, +V_1/2\}$, in Bridge I, ideally the neutral point voltage should be perfectly balanced. However, two different mechanisms can cause voltage imbalance between the bus capacitors in a real converter hardware. First, tolerances in component values causing capacitance mismatch and uneven degradation of components lead to sustained voltage imbalance [34]. Second, perfect synchronization of gate pulses to generate three-level voltage, which prevents any current flow into the neutral point, cannot be guaranteed in a real application. Consequently, neutral current flows due to such gating mismatches caused by asymmetry in gate drive and/or the pulsewidth-modulator in the digital controller. As it is shown in Section V, few nanoseconds of mismatch in gating can unevenly charge/discharge the upper or the lower capacitor leading to imbalance up to hundreds of volts within seconds. Without explicit measures to balance the neutral point voltage, such gating mismatch can lead to growing voltage imbalance and eventually damage the power devices due to overvoltage. Therefore, an explicit control strategy for capacitor voltage balancing is required for safe operation of the NPC topology.

III. Proposed Voltage Balancing Controller

The proposed capacitor voltage balancing controller dynamically generates balancing current i_o based on the error voltage $e_v = v_U - v_L$. For instance, a negative balancing current $i_o < 0$ is required to charge the upper capacitor C_U for $e_v = (v_U - v_L) < 0$. The voltage balancing controller is designed to satisfy four key targets:

1) generates balancing current i_o without introducing any dc offset in v_p;
2) insensitive to the direction of power flow and does not need to change based on the direction of transformer current i;
3) generates small voltage vectors naturally by the power stage during the commanded zero voltage vector time (rather than by the modulator);
4) allows only one switching transition (turn-ON and turn-OFF) of each power device within each switching cycle.

To illustrate the principle of operation, we compare two cases where power is flowing from Bridges II to I and the bus voltages are set as $V_1 = nV_2$. In the first case, the two bus capacitors are perfectly balanced, i.e., $v_U = v_L$. In the second case, $v_U < v_L$ and to compensate for the imbalance, a negative neutral current (i.e., balancing current) $i_o < 0$ is required to charge the upper capacitor of the dc bus. The response of the proposed controller to such an imbalance is shown in Fig. 2. The balanced condition in case 1 is shown by dashed lines. We use complimentary switching pattern for each inner switch pairs $\{S_2,\ S_3\}$ and $\{S_6,\ S_7\}$. In case 1, the simultaneous switching of the inner switch pairs at t_2 on both NPC legs prevents any current flow to the neutral point, i.e., $i_o = 0$. By shifting the switching instant of $\{S_2,\ S_3\}$ to t_1 and $\{S_6,\ S_7\}$ to t_3, a charging current for C_U, i.e., $i_o < 0$ can be generated. A charging current into the neutral point, i.e., $i_o < 0$, is obtained for $t_1 \le t \le t_3$. Similarly,

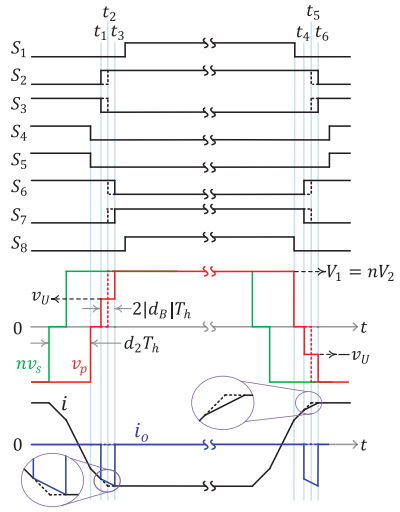

Fig. 2. Charging the upper capacitor C_U, when $v_U < v_L$, by adjusting the switching instants of the inner switch pairs of the two NPC legs (solid lines), whereas the dashed lines represent the nominal operation at voltage-balanced condition, i.e., $v_U = v_L$.

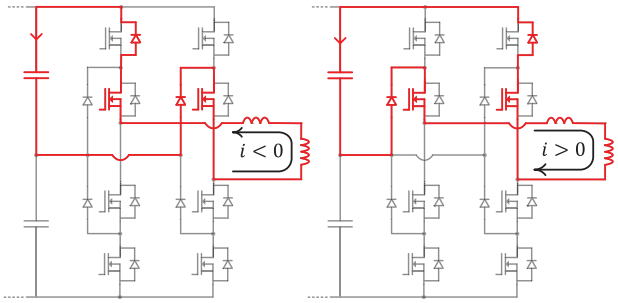

Fig. 3. Current conduction path for charging C_U ($d_B < 0$). (a) For $i < 0$. (b) For $i > 0$.

charging current is generated during $t_4 \le t \le t_6$. The current conduction paths during the two intervals are shown in Fig. 3(a) and (b), respectively.

It is worth noting that no active voltage vector is modified by the modulator, only the zero voltage vector is modified and the small voltage vectors $+V_1/2$ and $-V_1/2$ are generated naturally by the power-stage. We choose $(t_2 - t_1) = (t_3 - t_2) = (t_5 - t_4) = (t_6 - t_5)$ to ensure that no dc offset is generated in the applied voltage v_p across the transformer terminals and to ensure symmetric range for the balancing control input. For $v_U > v_L$, the switching instant of $\{S_2,\ S_3\}$ is moved to t_3 and $\{S_6,\ S_7\}$ to t_1 to generate $i_o > 0$, which charges the lower capacitor C_L. Similarly, charging current $i_o > 0$ can be generated during $t_4 \le t \le t_6$. The corresponding current conduction paths are shown in Fig. 4(a) and (b), respectively.

For simplicity, we choose a full H-bridge topology for Bridge II. The duty-ratios/pulse widths are set to be equal for Bridges I and II. The duration of the zero voltage vector is denoted as d_1 and the phase shift between v_p and nv_s is defined as d_2. Power flow from Bridge II to I requires nv_s leading v_p and

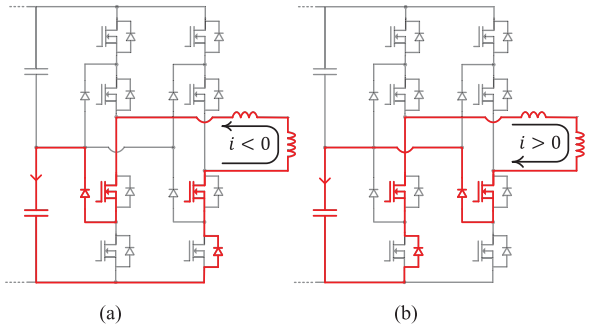

Fig. 4. Current conduction path for charging C_L ($d_B > 0$). (a) For $i < 0$. (b) For $i > 0$.

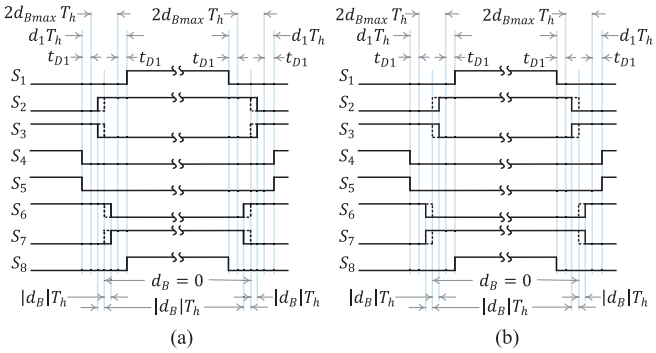

Fig. 5. Switching pattern for $d_B < 0$ and $d_B > 0$. (a) For $d_B < 0$. (b) For $d_B > 0$.

is denoted by $d_2 < 0$ and vice-versa. It is worth noting that both d_1 and d_2 are normalized by $T_h = T_s/2$, where T_s denotes the switching period. Without loss of generality, we set the nominal bus voltage references as $V_1^* = KnV_2^*$ where we denote K as the nominal voltage ratio. We define a balancing control input $d_B = t_B/T_h$. Fig. 5(a) and (b) show the switching patterns for $d_B < 0$ and $d_B > 0$, respectively. A $d_B < 0$ generates an $i_o < 0$ pulse and is used to charge the upper capacitor C_U, whereas $d_B > 0$ generates a $i_o > 0$ pulse that charges the lower capacitor C_L. In the following sections, we denote the minimum deadtimes required for Bridges I and II by $t_{D1} = d_{d1}T_h$ and $t_{D2} = d_{d2}T_h$, respectively. The maximum balancing duty $d_{B\max}$ in the NPC Bridge I is limited by the zero-vector duration d_1 and the minimum deadtime t_{D1} required between each inner and outer switch pair

$$d_1 \ge 2(d_{B,\max} + d_{d1}); \quad d_{d1} = \frac{t_{D1}}{T_h}; \quad |d_B| \le d_{B\max}. \quad (1)$$

Here, the deadtime for each inner and outer switch pair is required to avoid the destructive states of the NPC legs, such as $\{S_1, S_2, S_3, S_4\} \equiv \{1, 0, 0, 0\}$, which result in over-voltage across the inner switches. Deadtime is also required to prevent shoot-through faults, such as $\{S_1, S_2, S_3, S_4\} \equiv \{1, 1, 1, 0\}$. It is worth noting that in NPC Bridge I, the minimum deadtime requirement t_{D1} is fulfilled implicitly by enforcing (1), whereas t_{D2} is implemented explicitly in Bridge II; further details are provided in Section V. In the proposed balancing modulation scheme, balancing current is generated for a duration of $4d_BT_h$

TABLE I
SWITCHING STATES DURING BALANCING INTERVAL

d_B	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$d_B < 0$	0	1	0	0	0	1	0	0
$d_B > 0$	0	0	1	0	0	0	1	0

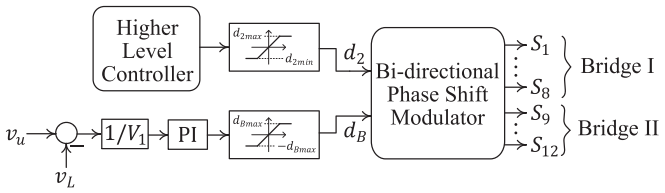

Fig. 6. A proportional-integral (PI) compensator can be used to dynamically generate d_B, whereas a HLC generates the phase-shift d_2 between Bridge I and Bridge II.

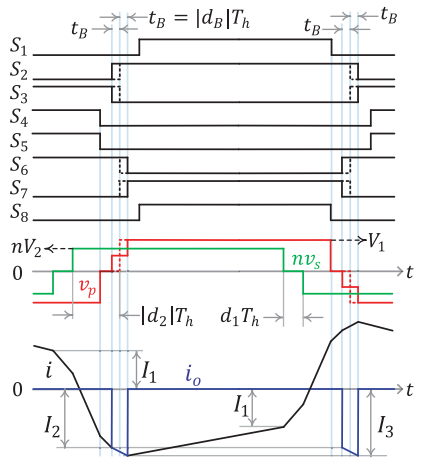

Fig. 7. Voltage and current shapes for $d_2 < 0$, $|d_2| \geq d_1$, $K > 1$, and $d_B < 0$.

in every switching period. The switching states of the NPC bridge during the balancing intervals are listed in Table I.

For $d_B < 0$, turning ON switches S_2 and S_6 while all other power devices are turned-OFF, generates negative balancing current $i_o < 0$ which charges the upper capacitor C_U irrespective of $i < 0$ [Fig. 3(a)] or $i > 0$ [Fig. 3(b)]. Similarly, for $d_B > 0$, turning ON switches S_3 and S_7 while all other power devices are turned-OFF, generates positive balancing current $i_o > 0$ which charges the lower capacitor C_L irrespective of $i < 0$ [Fig. 4(a)] or $i > 0$ [Fig. 4(b)].

Fig. 6 shows the implementation of the capacitor voltage balancing controller using a simple proportional integral (PI) compensator. The higher level controller (HLC) may be a closed-loop power flow controller or a closed-loop controller for output voltage such as V_1 or V_2. The HLC generates the phase-shift d_2, whereas the capacitor voltage balancing PI controller generates the balancing duty ratio d_B. Using d_2 and d_B, the BPSM, described in Section V, generates the gate pulses for the power devices of Bridges I and II. It is worth noting that in the selected modulation scheme, during the zero voltage vector time, the inductor current free-wheels through an inner power device and a clamping diode in each NPC leg. To maximize the power transfer capacity through the DAB converter, very small zero vector duration, such as $d_1 \approx 5\%$, can be used. However, the slightly uneven utilization of the inner and outer power devices may lead to earlier degradation of the inner devices. For $d_B \neq 0$, a balancing pulse is generated within the zero vector time during which an outer device is used instead of the clamping diode in one of the NPC legs. Therefore, the balancing pulses assist in equalizing the current stress among the inner and outer devices in the selected modulation scheme.

IV. BALANCING CURRENT AND POWER ANALYSIS

The implementation of the proposed capacitor voltage balancing method is insensitive to the modes of operation or the direction of power flow as described in the previous section. However, for the analysis of the balancing current and the balancing power, the shape of the balancing current pulse must be considered as a function of power flow direction, the voltage ratio K, and the relative values of d_1 and d_2. For the following analysis, we ignore the effect of deadtime for the power switches of Bridge II. The dc bus voltages of both bridges are assumed constant over a switching period and the effect of magnetizing inductance of the transformer is ignored. Reversing the sign of d_B reverses the polarity of the balancing current pulse, but the absolute values of current and the balancing power remain the same. In the following analysis, $|d_B|$ is used and the results apply identically for $d_B > 0$ and $d_B < 0$. The balancing power is defined as follows:

$$P_B = \frac{V_1 Q_B}{2T_s} = \frac{V_1}{2T_s}\int_{t-T_s}^{t} i_o(\tau)d\tau. \tag{2}$$

Here, Q_B denotes the total balancing charge generated over one switching period and P_B corresponds to the power that can be used to charge either C_U and C_L using the balancing current pulse i_o through the neutral point. The upper and lower capacitor voltages are approximated as $v_U \approx v_L \approx V_1/2$ to simplify the analysis. To illustrate the derivation process, we consider power flow from Bridges II to I, $d_2 < 0$, $|d_2| \geq d_1$, and $K > 1$. The relevant waveforms are shown in Fig. 7. The magnitude of the inductor current at the beginning and at the end of the balancing interval, denoted as I_2 and I_3, respectively, can be derived as follows:

$$I_2 = \frac{T_s}{4L}[(-1+d_1)V_1 + (1-d_1+2d_2+2|d_B|)nV_2]$$
$$I_3 = \frac{T_s}{4L}[(-1+d_1+2|d_B|)V_1 + (1-d_1+2d_2-2|d_B|)nV_2]. \tag{3}$$

The total balancing charge generated over one switching period is given as

$$Q_B = 2\int_0^{2t_B}\left(I_2 + \frac{nV_2 - V_1/2}{L}\right)d\tau = |d_B|T_s(I_2+I_3). \tag{4}$$

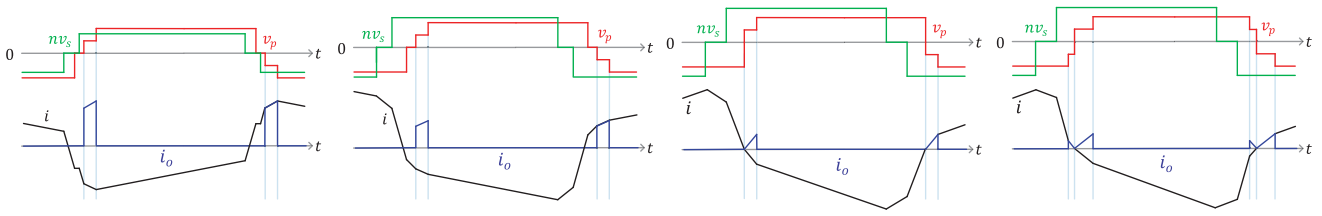

Fig. 8. Different shapes of balancing current pulse in different operating regions for $d_B > 0$.

TABLE II
SYSTEM PARAMETERS

L	Transformer leakage inductance	196μH
n	Transformer turns-ratio	2
L_m	Magnetizing inductance	7.8mH
$C_U,\ C_L$	DC bus capacitor (Bridge I)	250μF
C_2	DC bus capacitor (Bridge II)	1.5mF
f_s	Switching frequency	50kHz
V_2^*	Nominal voltage (Bridge II)	450V
V_1^*	Nominal voltage (Bridge I)	[450V, 1350V]
K	Voltage ratio	$[0.5, 1.5]$
P_{rated}	Rated Power	[5kW, 14kW]
t_{D1}	Dead-time for Bridge I	400ns
t_{D2}	Dead-time for Bridge II	350ns
d_{Bmax}	Maximum balancing duty-ratio	$0.01(\equiv 100\text{ns})$
d_1	Zero vector duty ratio	0.05

Using the balancing charge, the balancing power P_B generated by a balancing duty ratio of d_B can be derived as follows:

$$P_B = \frac{d_B T_s}{2L}[(-1 + d_1 + |d_B|)V_1 + (1 - d_1 - 2d_2)nV_2]. \tag{5}$$

It is easy to verify using similar analysis that (3), (4), and (5) apply identically for $d_B > 0$. The shape of the balancing current pulse changes in different operating regions. Fig. 8 illustrates a number of different shapes of balancing current pulse. For different voltage ratio K, zero vector duty ratio d_1, and phase shift d_2, the proposed balancing method leads to more than 20 different operating regions and corresponding balancing current pulse shapes. Following similar steps, the balancing power in each operating region can be derived. However, the lengthy and cumbersome derivations for all different operating regions can be avoided using high fidelity switching model simulation. The large number of simulations required to determine the balancing power for a wide range of operating conditions can be automated using simulation scripting. In the following section, the simulation setup is described and, subsequently, the simulated results are presented.

A. Simulation Analysis of Balancing Power

The simulation analysis is performed in *PLECS standalone* using nonlinear switching model simulation. We consider the bidirectional DAB converter with parameters listed in Table II. Following (1), the maximum balancing duty ratio is set as $d_{B\max} = 0.01$ ($t_B = 100$ ns). For Bridge II, a full H-bridge, shown in Fig. 9, is used. A detail BPSM is implemented following the guidelines described in Section V. In the entire operating range, the maximum balancing power that can be generated for the chosen maximum balancing duty-ratio $d_{B\max}$ for each combination of values of phase-shift d_2 and voltage ratio K is of particular interest. Therefore, the capacitor voltage balancing PI compensator, in Fig. 6, is bypassed and the balancing duty ratio is set as $d_B = d_{B\max}$. In order to avoid the closed-loop dynamics of the HLC, an ideal dc voltage source is used on the dc bus of Bridge II; and C_U and C_L are substituted by two ideal dc voltage sources. The phase-shift d_2 is explicitly set in an open-loop fashion bypassing the HLC. The balancing current i_o is measured and the balancing power is calculated using (2). A total of 10 201 simulations are performed by varying the voltage ratio in the range of $K \in [0.5, 1.5]$ in steps of 0.01 and the phase shift in the range of $d_2 \in [-0.5, 0.5]$ in steps of 0.01. The simulations are automated using *PLECS Simulation Scripting* [35] and the steady-state values are stored for each set of parameters $\{K, d_2\}$. It is worth noting that the transformer magnetizing inductance L_m is an order of magnitude higher than the leakage inductance and, hence, to speed up the simulation process, the effect of L_m is ignored. Fig. 10 shows the simulated results. It is evident that the proposed method can generate very high balancing powers even with a maximum balancing duty ratio of $d_{B\max} = 1\%$, which corresponds to balancing current pulse width of 200 ns ($\equiv 2d_{B\max}$). However, during the balancing interval, $|i_0| = |i|$ and, therefore, for specific operating conditions when $|i| \approx 0$, the proposed method cannot generate balancing charge. For instance, at the so-called *voltage-matched* condition, i.e., $K = 1$ for $d_2 = 0$, no real or reactive power flows between the primary and the secondary sides leading to $i = 0$ in the simulation. Due to the deadtime of the Bridge II and the zero vector applied by Bridge I, there arises a small region centered around $\{K, d_2\} \equiv \{1, 0\}$ that results in zero or very low real and

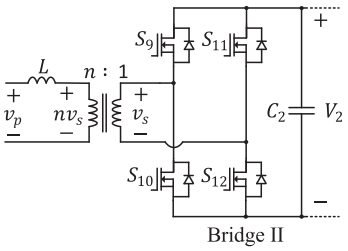

Fig. 9. Full H-bridge is used as Bridge II.

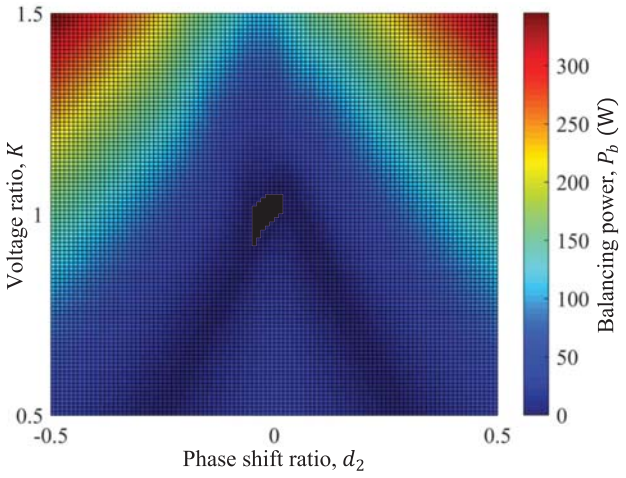

Fig. 10. Simulated balancing power at different operating condition.

reactive power flow through the transformer. In these operating regions, marked in black in Fig. 10, the proposed method fails to generate balancing charge theoretically. However, as it will be shown through experiments in Section VI that the proposed method successfully balances the upper and lower capacitor voltages even at no-load condition for $K = 1$. For any real application, a minimum power flow through the transformer always exists to supply the electrical and magnetic losses in the converter, which enables the proposed voltage balancing controller to generate balancing current at any operating condition.

V. BPSM With Capacitor Voltage Balancing Control

The BPSM is designed to facilitate bidirectional power flow combined with the proposed capacitor voltage balancing method. For a positive phase-shift ratio $d_2 > 0$, the primary side voltage v_p leads the secondary side voltage v_s and vice-versa. Fig. 11 shows the relevant wave-shapes for the modulator. A triangular carrier is used for Bridge I, whereas for Bridge II, a sawtooth carrier is used. Both carriers have periods of $T_s = 1/f_s$, but the sawtooth and triangular carriers have peak values of 1 and 2, respectively. It is worth noting that the outer switch pairs $\{S_1, S_8\}$ and $\{S_4, S_5\}$ have identical gating signals and their switching transitions are triggered by compare-match of the triangular carrier with x_{18} and x_{45}, respectively. For the inner switch pairs $\{S_2, S_3\}$ and $\{S_6, S_7\}$, complimentary gate pulses are used. The *compare-values* for the two inner switch pairs are denoted as x_{23} and x_{67}, respectively. The *compare-values* can be computed as given in Table III.

For Bridge II, phase-shift modulation (PSM) with 50% duty ratio for each leg of the full H-bridge is used [36]. The required active voltage vector/pulse width of v_s is implemented by creating a phase-shift between the two phase-legs. The PSM is implemented for Bridge II using the *compare-values* x_9, x_{10}, x_{11}, and x_{12}, which trigger the turn-OFF transitions of switches S_9, S_{10}, S_{11}, and S_{12}, respectively. The turn-ON transitions of the switches are derived from the turn-OFF transitions of the respective complimentary switches applying the

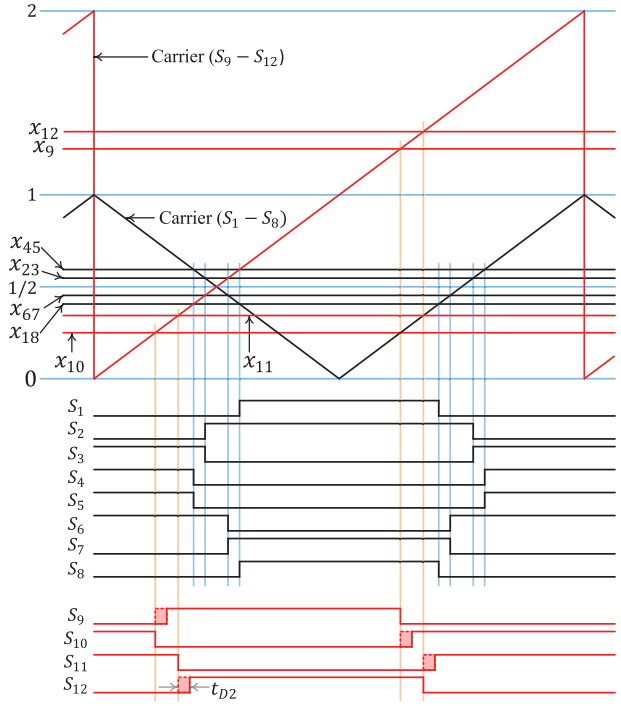

Fig. 11. BPSM for the DAB converter designed for bidirectional power flow and capacitor voltage balancing in Bridge I. The wave-shapes for Bridges I and II are shown in black and red, respectively.

TABLE III
Compare-Values for BPSM

Compare-value signal	Switch	Value
x_{18}	$S_1,\ S_8$	$0.5(1 - d_1)$
x_{45}	$S_4,\ S_5$	$0.5(1 + d_1)$
x_{23}	$S_2,\ S_3$	$0.5 - d_B$
x_{67}	$S_6,\ S_7$	$0.5 + d_B$
x_9	S_9	$0.5(3 - d_1 + 2d_2)$
x_{10}	S_{10}	$0.5(1 - d_1 + 2d_2)$
x_{11}	S_{11}	$0.5(1 + d_1 + 2d_2)$
x_{12}	S_{12}	$0.5(3 + d_1 + 2d_2)$

required deadtime t_{D2}. It is worth noting that the deadtime for Bridge I is implemented implicitly through (1). The BPSM can be implemented with ease using standard microcontrollers or digital signal processors (DSPs).

For $d_B = 0$, ideally the switching of the inner switch pairs $\{S_2,\ S_3\}$ and $\{S_6,\ S_7\}$ in the two NPC legs should be matched exactly. However, owing to process variation, asymmetry in gate-drive, and circuit layout, gating mismatch cannot be avoided in a real application. Without voltage balancing control, such timing mismatch leads to growing voltage imbalance. For instance, in the simulated converter for $K = 1.5$ and $d_2 = -0.21$, a gating mismatch of 5 ns unevenly charges/discharges the two bus capacitors and the voltage imbalance grows to $|v_U - v_L| \approx 384$ V over 10 s without balancing control. The integral part of the voltage balancing controller is required to compensate such offsets in d_B.

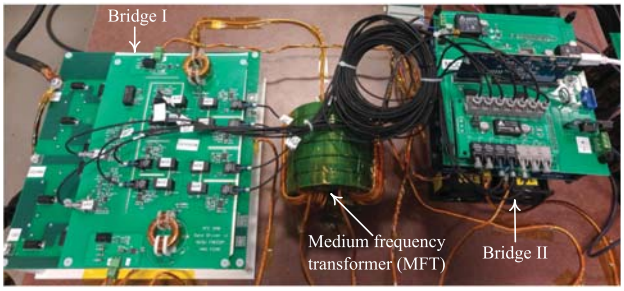

Fig. 12. Experimental setup using a full-bridge NPC topology for Bridge I and a full H-bridge topology for Bridge II; the system parameters are listed in Table II.

VI. Experimental Results

To validate the proposed voltage balancing controller, an experimental setup is built with the system parameters listed in Table II. Fig. 12 shows the experimental setup. A dc voltage supply is connected to the dc bus of Bridge II and the bus voltage is set as $V_2^* = 450$ V. A PI compensator is used as the HLC to regulate the dc bus voltage V_1 of Bridge I. The PI compensator gains are chosen as $K_{P,\text{HLC}} = 0.028$ and $K_{I,\text{HLC}} = 11.37$. The capacitor voltage balancing PI compensator is designed as $K_{P,cvb} = 0.1$ and $K_{I,cvb} = 0.1$. The reference for the closed-loop controller (HLC) is set as $V_1^* = KV_2^*$. The HLC, the capacitor voltage balancing compensator, and the BPSM, described in Section V, are implemented using a C2000 DSP (TMS320F28377D) by Texas Instruments.

All test data are collected using a mixed domain oscilloscope with 350 MHz bandwidth and 2.5 GS/s sampling rate. Voltage waveforms are collected using differential voltage probes with bandwidths of 100 MHz, whereas current waveforms are measured using current probes with dc to 20 MHz bandwidth. First, the voltage ratio is set as $K = 1$ and a load resistance of $R_L = 400\,\Omega$ is connected across the dc bus of Bridge II. The connected load results a power flow of ≈ 2 kW through the DAB converter. Imperfections in the converter prototype cause significant voltage imbalance between the upper and lower capacitors (≈ 31 V) as seen in Fig. 13. Although the exact source of the imbalance cannot be determined, activating the proposed voltage balancing controller eliminates the mismatch (see Fig. 13). Fig. 14 shows the zoomed-in response at voltage-balanced condition. Next, the voltage ratio is changed to $K = 0.9$ and $K = 1.1$ by changing the reference voltage $V_1^*(= K \times 450)$ V and the corresponding wave-shapes are shown in Figs. 15 and 16, respectively. For the load resistance of $R_L = 400\ \Omega$, power flow of ≈ 1.6 and 2.5 kW through the DAB converter is achieved for $K = 0.9$ and $K = 1.1$, respectively. In both cases, the proposed controller obtains voltage balanced operation, i.e., $v_U = v_L$. Fig. 17 shows the step response for $K = 1$ to $K = 1.1$. It is evident that during the transient, voltage balancing is retained by the proposed controller. To evaluate the controller performance at the theoretical worst case, the voltage ratio is set as $K = 1$ and the load is removed from the dc bus of Bridge I. The corresponding result

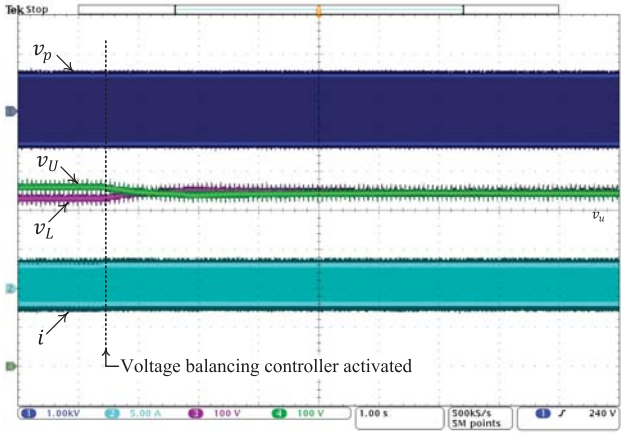

Fig. 13. Without active voltage balancing, ≈ 31 V mismatch is observed between v_U and v_L due to imperfections in the prototype. Activating the proposed voltage balancing controller eliminates the mismatch; scale: voltage (v_p): 1 kV/div, voltage (v_U, v_L): 100 V/div, current: 5 A/div, and time: 1 s/div.

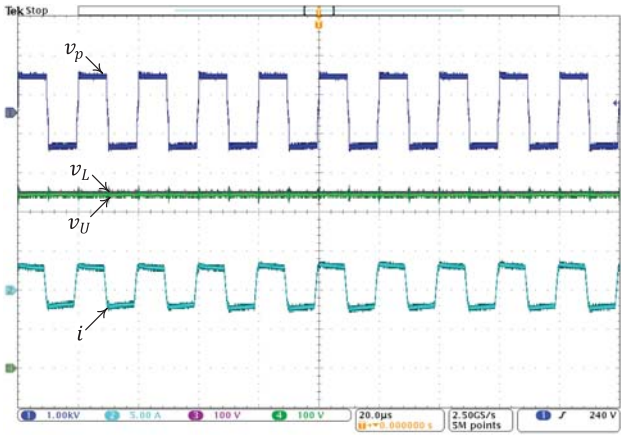

Fig. 14. Capacitor voltage balanced operation at $K = 1$ using proposed controller; scale: voltage (v_p): 1 kV/div, voltage (v_U, v_L): 100 V/div, current: 5 A/div, time: 20 μs/div.

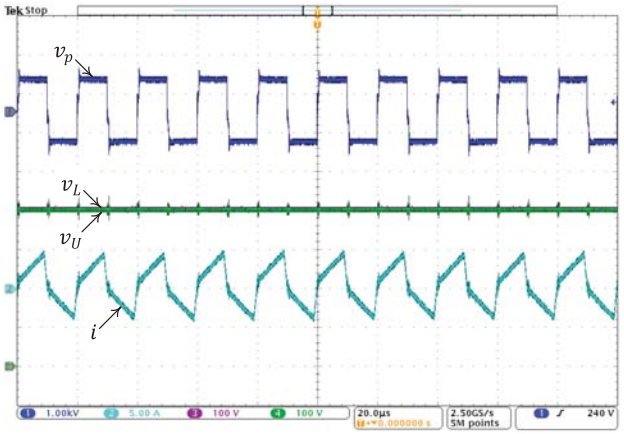

Fig. 15. Capacitor voltage balanced operation at $K = 0.9$ using proposed controller; scale: voltage (v_p): 1 kV/div, voltage (v_U, v_L): 100 V/div, current: 5 A/div, time: 20 μs/div.

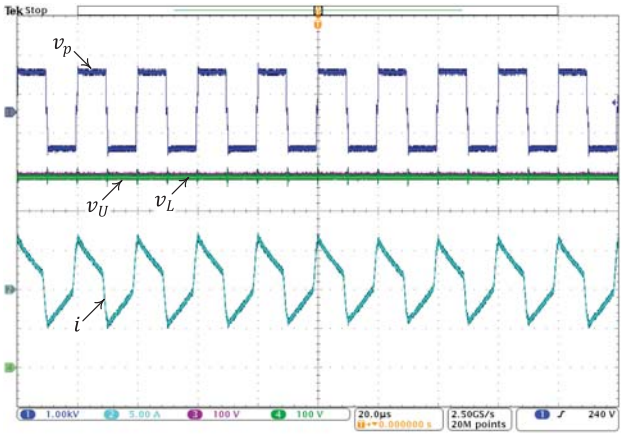

Fig. 16. Capacitor voltage balanced operation at $K = 1.1$ using proposed controller; scale: voltage (v_p): 1 kV/div, voltage (v_U, v_L): 100 V/div, current: 5 A/div, time: 20 μs/div.

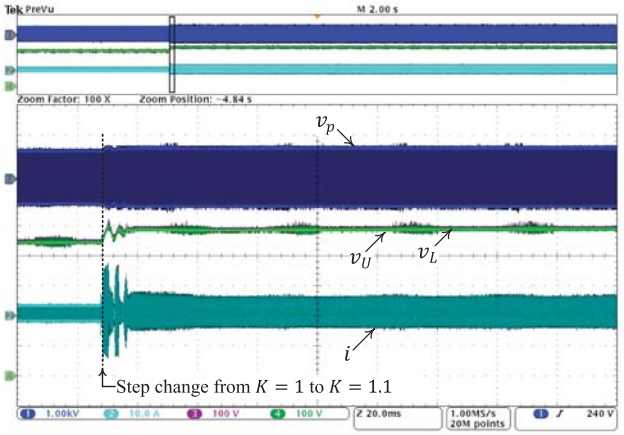

Fig. 17. Balanced capacitor voltage retained during transient for step change in reference voltage V_1^* ($K = 1$ to $K = 1.1$); scale: voltage (v_p): 1 kV/div, voltage (v_U, v_L): 100 V/div, current: 10 A/div, time: 20 ms/div.

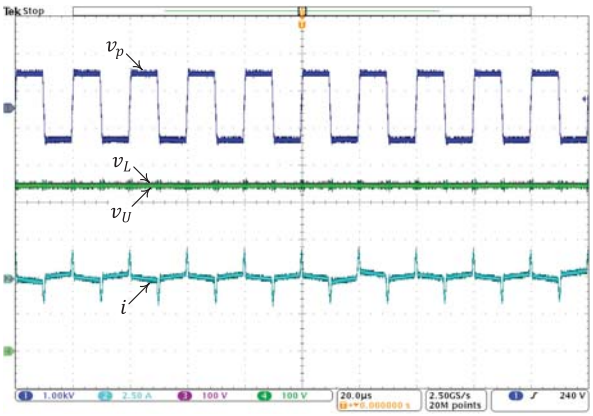

Fig. 18. Balanced capacitor voltage retained at no-load and $K = 1$ using proposed controller; scale: voltage (v_p): 1 kV/div, voltage (v_U, v_L): 100 V/div, current: 2.5 A/div, time: 20 μs/div.

is shown in Fig. 18. It is evident that the capacitor voltages are balanced perfectly even for the minimal current flowing through the transformer. Due to the voltage-matched condition, i.e., $V_1 = nV_2$, no reactive power flows between the two bridges. Only a small real power flows through the transformer to supply the electrical and magnetic losses of the converter.

VII. Conclusion

Capacitor voltage balancing is achieved in a full-bridge NPC topology based DAB converter without active adjustments/selection of small voltage vectors. The proposed method is universal for any direction of power flow through the DAB converter under any operating condition and does not introduce any dc offset in the voltage-second across the transformer terminals. Through analysis and simulations, the balancing power that can be generated for a given balancing duty ratio is derived for the entire operating region. Experimental results validate the effectiveness of the proposed voltage balancing method.

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