A 12.47 kV Medium Voltage Input 350 kW EV Fast Charger using 10 kV SiC MOSFET

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***Abstract*—This paper presents a medium-voltage (MV) (12.47 kV), 350 kW electric vehicle (EV) fast charger using 10 kV SiC MOSFETs. Detailed system design procedure based on the 10 kV SiC MOSFET characterization is presented to provide a guide on the 10 kV SiC MOSFET converter development. Taking the advantage of the 10 kV SiC MOSFET's high voltage blocking capability and efficient switching performance, a single module high power density system is designed with the DC/DC stage operates at 25 kHz and the simulated system efficiency exceeds 98%, input current THD lower than 2%. With all the passive components selected, the designed system power density is 1.6 kW/L.**

***Index Terms*—component, formatting, style, styling, insert**

I. Introduction

With ever increasing electric vehicle (EV) battery capacity, high-power chargers are needed to provide a gas-station like refueling experience for EVs. Fast chargers with a 150 kW-350 kW capacity have recently been introduced to the marketplace as product offerings [1]. The approach to designing chargers is to supply low voltage 3-phase service (480 V in the US) to these chargers. This approach requires a step down transformer and handling of very larger currents on the AC side, especially on site supplies multiple 350kW chargers. Recently [2] researchers have proposed connecting EV fast charger directly to the MV line, through a solid-state transformer, thus improving system efficiency, and reducing system footprint [3].

Though the SST based MV fast charger eliminates the need for a service transformer and provides a significant reduction in system footprint, the direct connection to MV requires high voltage blocking capability of the converters. As a result, many MV fast charger prototypes use high-voltage IGBTs with the overall switching frequency lower than 10 kHz with bulky passive components and relatively low power density [4]–[6]. Researchers in [7] use more efficient silicon MOSFET based dual active bridge (DAB) modular approach which boosts the system switching frequency to 20 kHz. In [2], a higher device utilization multi-cell boost (MCB) based modular topology was selected to build a 50 kW MV fast charger using 1.2 kV silicon carbide (SiC) MOSFETs which achieved 50 kHz switching frequency with smaller number of modules and power density higher than 0.5 kW/L. Though using SiC MOSFETs helps improve the system efficiency due to reduced switching and conduction losses, the limited blocking voltage requires the connection of many modules in series in order to block the MV input. This modular approach increases the system complexity and highly affects the reliability of the MV fast charger, due to the increased component count.

In recent years, Wolfspeed has developed and packaged 10 kV SiC device prototypes and have made these devices available to researchers. These devices have substantially lower switching loss and specific on-resistance compared to the Si IGBT of the same voltage level [8]. With the maturity of the device gate drivers and characterization techniques [9], [10], a number of prototypes that use these devices have been developed and demonstrates including 100 kW rating MV ac SST [11], MV dc SST [12], [13] and impedance measurement unit [14].

Based on the published data, five prospective MV rectifier topologies are selected and some of their basic feasures are summarized and compared in Table I. In this paper, a modification topology of [2] shown in Fig. 1 is selected to build the standard 12.47 kV voltage level input 3 phase 350 kW dc fast charger. The 10 kV device blocking capability enables direct connection to the 7.2 kV line-to-neutral voltage using the topology. In this paper we present a detailed design procedure including the semiconductor selection and characterization, operating frequency and passive component design as well as the system efficiency optimization.

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TABLE I
BASIC METRICS SUMMARY AND COMPARISON FOR CANDIDATE TOPOLOGIES

Metric	CVR	MCB	Active MCB	HB	Single Stage ANPC
10 kV MOSFETs	20	18	24	12	18
1.2 kV MOSFETs	0	0	12	12	12
10 kV Diodes	16	12	6	0	0
1.2 kV Diodes	8	12	0	0	0
SiC Semiconductor Devices Total	44	78	78	72	66
Medium Frequency Transformers	2	3	3	6	3
Hard-Switched MOSFETs	16	12	6	0	0
Control Complexity	High	Medium	Medium	Medium	High

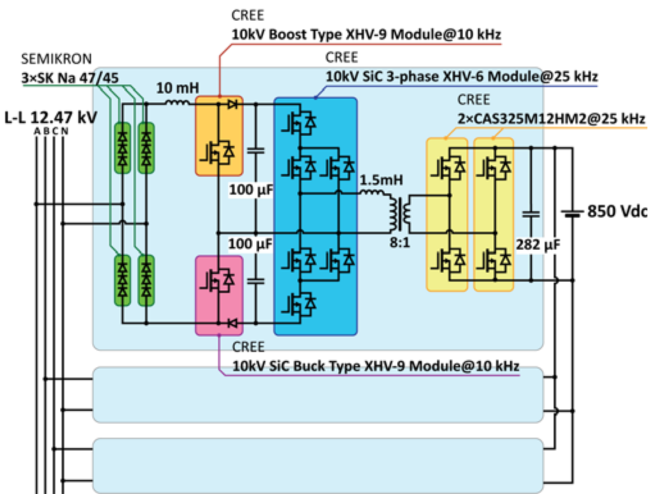

Fig. 1. The topology of MV 350 kW EV fast charger

II. EVALUATION AND CHARACTERIZATION OF 10 KV SIC MOSFETS

The semiconductors selected for the MV fast charger prototype are shown in Fig. 1. Each input rectifier diode consists of three series connected silicon SK Na 47/45 diode from SEMIKRON. A boost type and a buck type connected 10 kV SiC MOSFET and Schottky Diode are packaged in XHV-9 module to form a three level boost (TLB) circuit as the front PFC stage. Three separate half bridge legs are packaged in a XHV-6 module to form the primary side of the active NPC (ANPC) based dual active bridge (DAB) converter. Because of the high voltage conversion ratio, the RMS current on the secondary side of the ANPC DAB is very large, so two CAS325M12HM2 module 1.2 kV SiC MOSFET with $R_{dsON} = 12m\Omega$ are used to form a full bridge on the secondary side.

Devices were characterized using the double pulse tester (DPT) shown in Fig. 2. The DPT was used to measure the device switching losses so that passive component values and operating frequencies could be determined. The DPT uses P6015A high-voltage passive

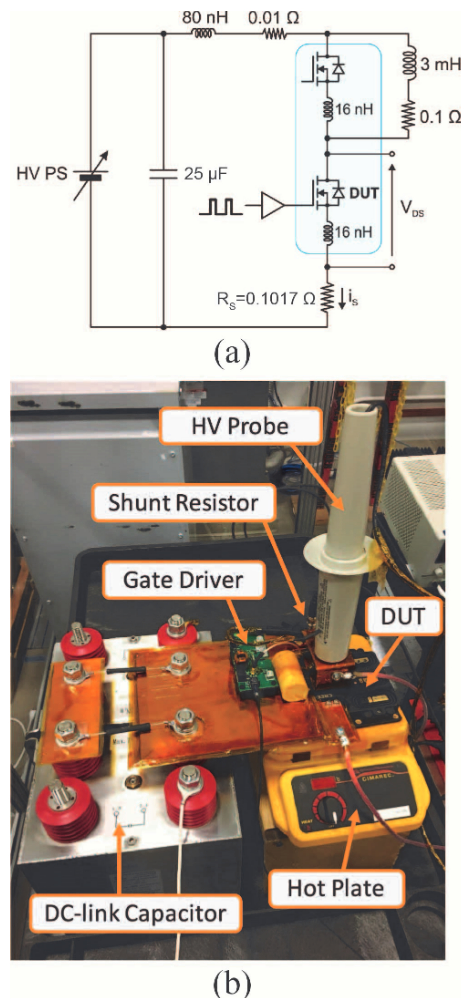

Fig. 2. (a) Circuit for the double pulse test with parasitic component values, (b) DPT setup for the 10 kV SiC MOSFETs characterization

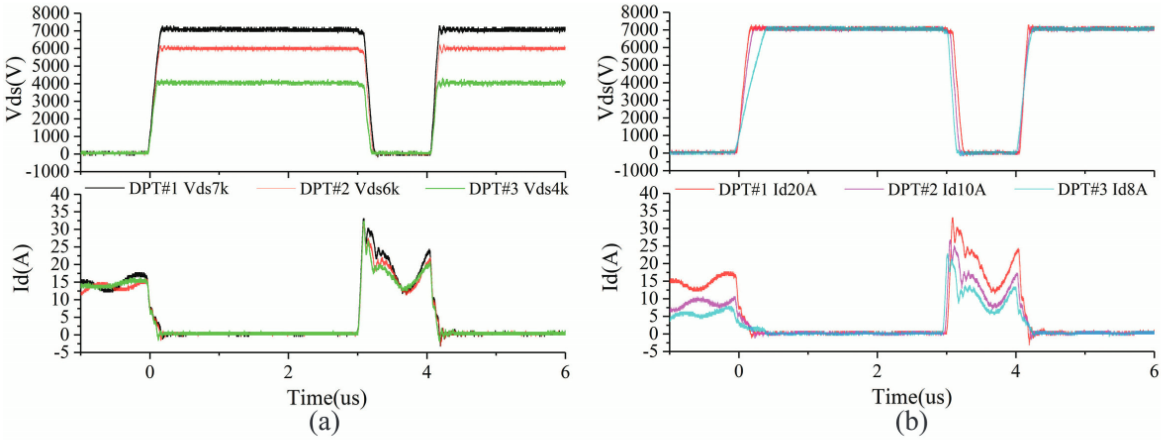

Fig. 3. (a) 10 kV SiC MOSFETs double pulse test waveforms at 15 A conduction current with variable input voltage, (b) 10 kV SiC MOSFETs double pulse test waveforms at 7 kV input voltage with variable conduction current

probe for the voltage sensing. A 0.1017Ω SSDN-414-10 shunt resistor with 2 MHz bandwidth is used for the current sensing after de-skewing with the voltage probe. As shown in Fig. 2(a), since the device under test (DUT) is operating at medium voltage, a large air-core inductor with a large inductance is needed for the freewheeling. The air core inductor parasitic capacitance must be as small as possible so as not to introduce additional discharging current during the turn *OFF* test. Based on [15], the C_{oss} of the DUT is around 160 nF. By separating the multi-layer distance, a 3 mH inductor with 25 nF stray capacitance was designed and built.

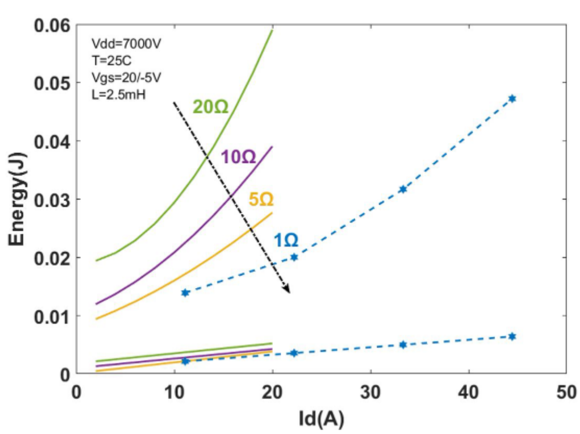

Fig. 4. 10 kV SiC MOSFET switching energy with respect to different gate resistance, and different current tested at 7 kV, $25°C$

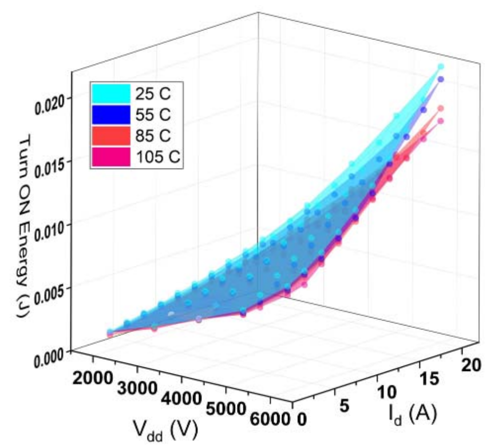

Fig. 5. Switching loss model for the 10 kV SiC MOSFET used in the PLECS simulation

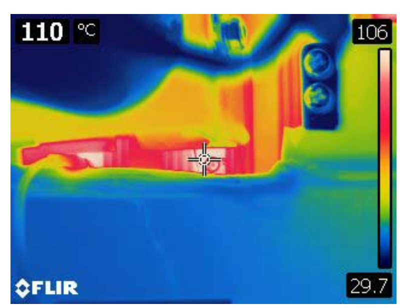

Fig. 6. Die temperature captured by thermal image camera during a $105°C$ double pulse test

Complete device characterization considering gating resistance, input voltage and die temperature was performed using the DPT setup. Fig. 3 shows the experimental waveform for the 7 kV double pulse test with a gate resistor 5Ω at die temperature $25°C$, where the green trace is V_{ds} of the DUT's lower switch, pink trace is the voltage measured on the shunt resistor and the dark blue trace is half of the input voltage source measured on one of the two series connected dc-link capacitor. Figure 4 shows that the switching energy decreases significantly as the gate resistance reduces from $R_g = 20\Omega$ to $R_g = 5\Omega$. Further gate resistance reduction does not lead to major loss reduction, while leading to significant voltage overshoot during the switching transient, which may cause severe EMI issues. As a result, $R_g = 5\Omega$ is chosen as the gate resistance. To develop a loss vs temperature dynamic model of the switching device with given gate resistance, double pulse tests with variable die temperature have been conducted. In order to regulate the die temperature, a die, module and ambient steady state is reached by heating up the entire module with hotplate. The double pulse frequency is set to 1 Hz so that the switching and conduction losses don't provide significant transient temperature change. Thus a device loss look up table model with respect to V_{dd}, I_d and T is created and is shown in Fig. 5. Fig. 6 shows the die temperature of the DUT during the testing captured by a thermal camera.

III. System Parameter Design and Passive Component Selection

Using the thermal model shown in Fig. 5, we developed a complete system simulation in PLECS, which allowed us to select the device switching frequency and the values of the passive components. For the control of the TLB PFC stage, the predictive current control method described in [16] is implemented so that low THD could be achieved with relatively small input inductance. For the DAB stage, a traditional triple phase shift (TPS) control method [17] is implemented to achieve output voltage regulation as well as soft-switching. The system control scheme is shown in Fig. 7.

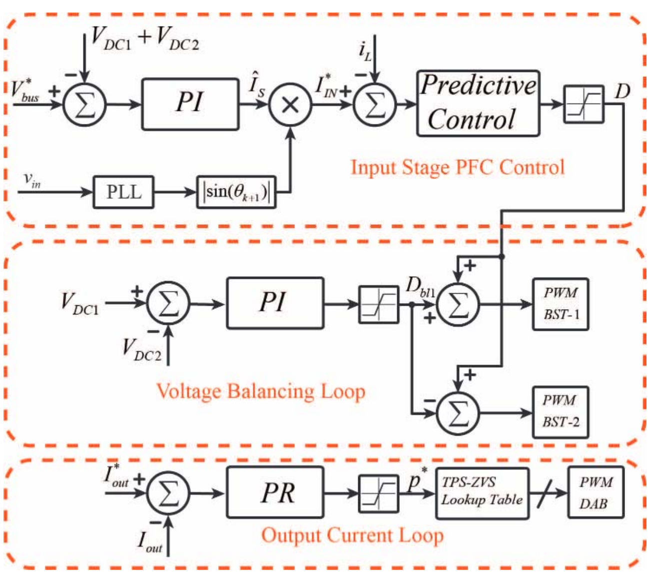

Fig. 7. per phase system control scheme for 10 kV 350 kW EV fast charger

For the correct operation of the boost converter, the DC-link voltage at the output must be larger than the peak value of the input waveform. Therefore, for the rectified 7.2 kV RMS input system, the DC bus voltage must be larger than 10.2 kV. We selected 13.8 kV to provide enough operating margin for the boost converter. Since each 10 kV device in the NPC configuration only needs to block half of the voltage 6.9 kV, each device operates well within its safe operating area. On the secondary side of the DAB, the nominal voltage should be close to primary side nominal voltage, so that RMS current and the reactive power is minimized [18]. With the transformer turn ratio of 8:1, the 850 V secondary side voltage induces 6.8 kV in the primary side of the transformer. The electrolytic capacitor 500MXH390MEFCSN30X60 of 390 μF/500 V were selected as the dc link capacitors. 16 capacitors are connected in series to support the full voltage of 6900 V. Two of the electrolytic capacitors are connected in parallel to enlarge the overall capacitance which gives a 50 μF dc link capacitance. An additional film capacitor bank which consist of 8 parallel 4 series connected PHE450SD6100JR06L2 capacitors rated at 0.1 μF/2 kV gives an overall 1.12 μF decoupling capacitance. The film capacitors 944U470K122AAM of 47 μF/1200V were used for the secondary side output voltage filtering. 6 capacitors are connected in parallel to enlarge the output capacitance.

The input inductor and the high frequency transformer were custom designed for the specific application. The input inductor was made by using 10 stacked MPP toroid cores 0055868A2 with 120 turns of 10 AWG litz wire. The designed inductance at 20 A current was around 4 mH. The high frequency transformer was made by using 10 N87 Ferriet U-shape cores with the transfer ratio of 80:10 turns of high voltage side 10 AWG low voltage side 7 thread twisted 10 AWG litz wire. The transformer parameters were measured using AP Instruments' Model 300 Frequency Response Analyzer with a coupling capacitance 57 pF and leakage inductance 2.5 mH. The transformer loss was determined experimentally using the setup and circuit shown in Fig. 8. The single N87 core with 10:10 turn ratio is tested with the secondary side opened at both 25 kHz and 50 kHz to determine the magnetic core loss. Fig. 9 shows a testing waveform at 50 kHz 300 V input voltage where the dark blue trace is the voltage of the primary side of the transformer, light blue trace is the voltage of the secondary side of the transformer and the purple trace is the current on the primary side. The system hardware and component selection is shown in TABLE. II.

Switching frequency optimization has been done through the loss model based thermal simulations. Since the boost PFC stage is hard switching, a lower switching frequency is preferred. However, the switching frequency can not be too low since the current ripple increases with the decrease of the switching frequency resulting a higher switch off current to provide higher switching

TABLE II
SYSTEM HARDWARE AND COMPONENT SELECTION RESULTS

ITEM	PART NO.	VALUE
Input Diode Heatsink	Fischer Elektronik K 5 M8	R_{th}=5 K/W
10 kV SiC MOSFET Heatsink	Fischer Elektronik SK 497 200	R_{th}=0.55 K/W
1.2 kV SiC MOSFET Heatsink	Fischer Elektronik LA 7/150	R_{th}=0.75 K/W
DC-Link Capacitor	500MXH390MEFCSN30X60	390 μF, 500 V
Decoupling Capacitor	PHE450SD6100JR06L2	0.1 μF, 2000 V
Output Capacitor	944U470K122AAM	47 μF, 1200 V
Input Inductor Core	0055868A2	MPP Toroid 026
Transformer Core	B67385G0000X187	Ferrite U-shape N87

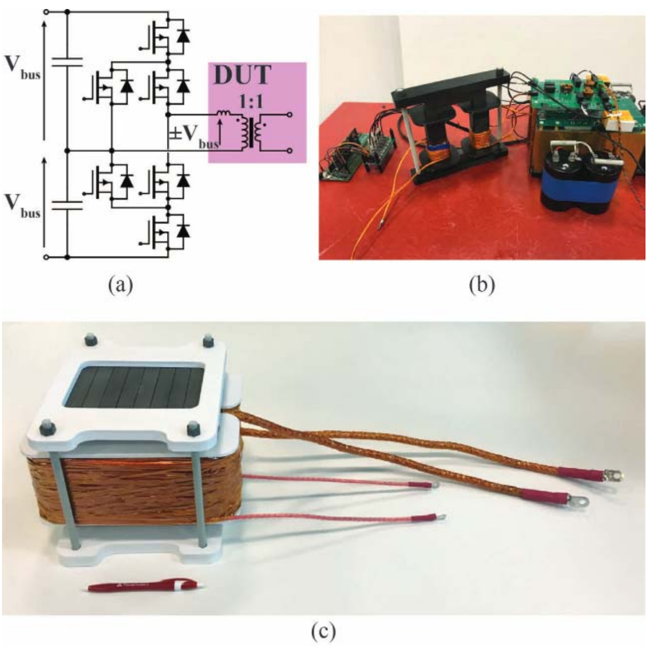

Fig. 8. (a) Circuit for the transformer core loss characterization, (b) Hardware setup for the transformer core loss test, (c) Transformer built based on the system design using N87 U-shape cores

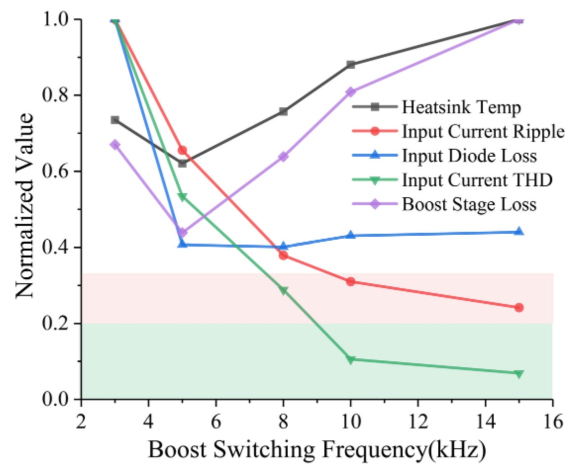

Fig. 10. boost stage switching frequency optimization shown in normalized value where heatsink temp base is 70.36$°C$, input current ripple base is 29 A, input diode loss base is 214 W, input current THD base is 19% and boost stage loss base is 716 W

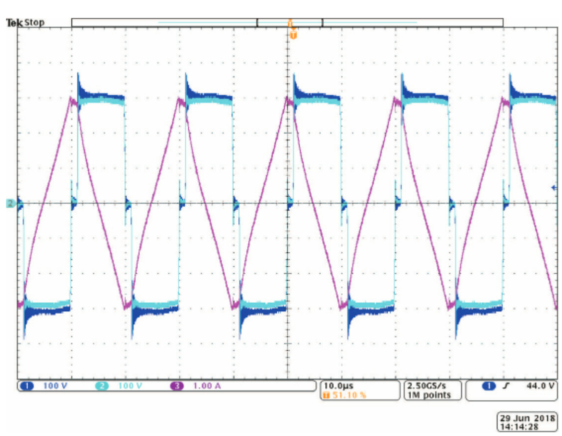

Fig. 9. Transformer core loss test waveform at 50 kHz, 300V

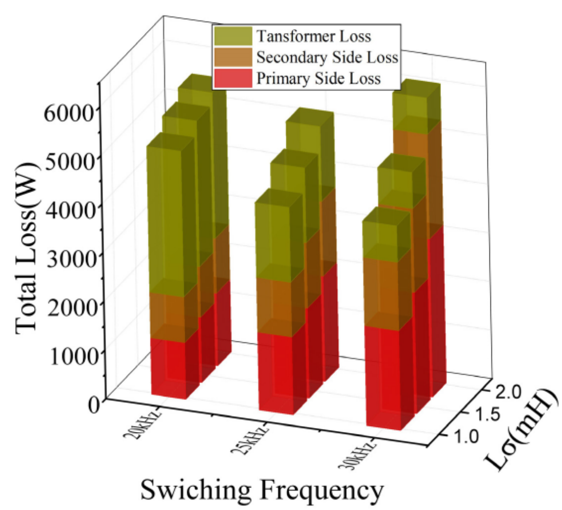

Fig. 11. dual active bridge stage switching frequency and leakage inductance optimization results

360 kW, Ta = 25 C					
Losses [W]					
		10 kHz	25 kHz		
IN D	IN L	BST	ANPC	TR	SEC
253.85	45.00	1697.67	2205.08	1542.00	1507.8
52°C	N/A	60°C	70°C	N/A	75°C

Total losses [W]	7723.79
Output power [W]	359845
Efficiency	98.1%
Output voltage [V]	850.6
Input Current THD	1.5%
Input Power Factor	0.9993

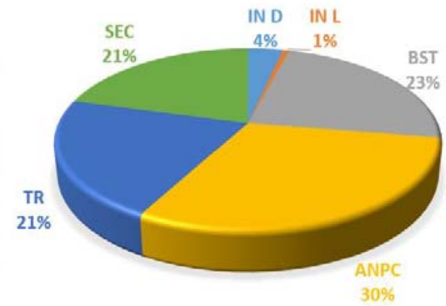

Fig. 12. Detailed system loss breakdown and heatsink temperature of the rated power thermal simulation

losses. Also, low switching frequency results in high THD which deficit PFC function. Based on electrical and thermal simulations, the TLB stage switching frequency was selected to be 10 kHz which is shown in Fig. 10 where a maximum THD and current ripple requirement is set. High switching frequency helps to reduce the passive component value which reflects as a lower magnetic loss in the high frequency transformer. However, higher switching frequency provides higher switching losses as well. At the same time, leakage inductance affects the reactive power which is related to the conduction losses of the system. The DAB optimization is shown in Fig. 11. Considering the feasibility of the leakage inductance in 90 kV level insulation the DAB stage is chosen to operate at 25 kHz to allow sufficient power transfer, given the moderate (1.5 mH) leakage inductance. With this operating frequency a primary to secondary side phase shift of 50°, delivers the target 350 kW. Fig. 12 shows the detailed simulated loss breakdown, where the system shows 98.1% efficiency at rated power.

Fig. 13 shows the three phase input inductor current simulation waveform and DAB stage transformer voltage and current waveform at rated 350 kW power. Fig. 14 shows the 3D rendering with the designed passive components, heatsink and semiconductors where a 1.6 kW/L power density is achieved.

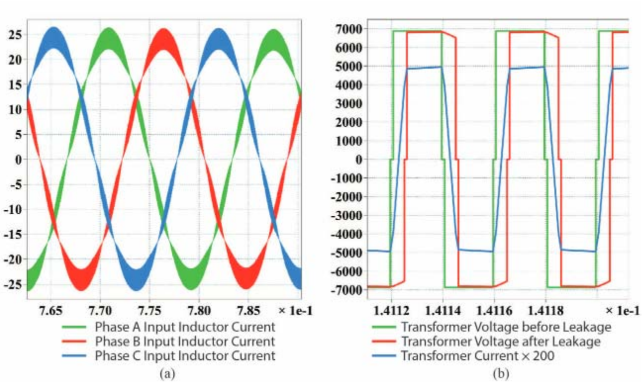

Fig. 13. Simulation waveform at rated 350 kW

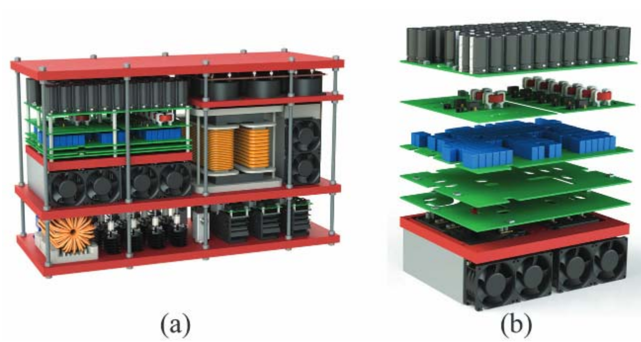

Fig. 14. (a) 3D rendering for one phase of the proposed 350 kW EV fast charger with the proposed design (b) stack design of the high voltage side dc bus bar and capacitor bank to minimize the loop inductance

IV. Conclusion

This paper presents the design procedure of a 12.47 kV Input 350 kW EV fast charger using 10 kV SiC MOSFET. The 10 kV SiC MOSFET switching performance has been characterized through the double pulse test and loss model of the semiconductor has been developed for thermal simulations. A simulation based system optimization helped determine the correct passive components and switching frequencies and a high fidelity thermal simulation based on the experimental validated loss model has shown the system efficiency exceeds 98%.

Acknowledgment

The information, data, or work presented herein was funded in part by the Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy, under Award Number DE-EE0006521 with North Carolina State University, PowerAmerica Institute.

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