

A Distributed Control Architecture for Cascaded H-Bridge Converter with Integrated Battery Energy Storage

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Abstract—Cascaded H-bridge topology has been used in grid-tied converters for battery energy storage system due to its modular structure. To fully utilize the converter's modularity, this paper proposes a hierarchical distributed control architecture that consists of primary control, secondary control and battery state of charge (SOC) balancing control. Primary control ensures accurate current tracking while a distributed secondary control based on consensus algorithm is presented to regulate power sharing among modules and is proved to be stable theoretically. A distributed SOC balancing control is further introduced to improve energy efficiency of battery energy storage system. Finally, the hierarchical distributed control strategy is implemented using hardware controllers and a software platform. Besides, a carrier phase shift control is also implemented to achieve multilevel output voltage and harmonic reduction. The experimental results demonstrate the performance of the proposed control scheme effectively.

Index Terms—Battery SOC balancing, cascaded H-bridge, consensus algorithm, distributed control.

I. INTRODUCTION

THE increasing penetration of intermittent renewable energy sources, such as wind and solar, leads to numerous challenges for power grid operation. Dispatchable battery energy storage system (BESS) can address many of these issues by balancing out power fluctuation, shaving peak and filling valley in power requirement, increasing the reserve capacity of power grid, etc. As one of the most popular multilevel topologies, cascaded H-bridge (CHB) topology can effectively integrate BESS into the grid in medium voltage and high power applications, since it can use switching devices with lower voltage ratings and achieve low electromagnetic interference, low total harmonic distortion and fault-tolerance capability [1], [2]. Moreover, the modular structure of CHB topology makes it possible to achieve high conversion efficiency.

CHB converter usually utilizes a central controller since it is easy to realize system control and synchronized modulation [3], [4]. The central controller communicates with every H-bridge module via high-speed communication links. It executes all the calculations and sends switching commands to each module at every switching cycle, which increases the computational burden of the central controller and makes modularization difficult. Besides, the switching noise of high-

power converters can degrade the quality of communication, which could potentially degrade the converter's performance.

To circumvent the need for a central controller and high bandwidth communication, distributed control approaches are preferred. In distributed control strategies, the control and modulation are implemented in the local controllers of each module. Information is collected locally and exchanged through a sparse communication network. However, for CHB converter, it is challenging to achieve accurate output current regulation and power sharing control among modules without globally coordinating the switching actions of all the semiconductor devices. Existing distributed control strategies for the CHB converter is summarized in Table I. One approach is to directly regulate the current through one (or multiple) modules, while the remaining modules only operating in the open-loop and provide grid voltage support; such a method leads to a control architecture without communication [5]–[8]. In [9], a current controller hybrid automata is proposed to choose one module to regulate current at a time. However, the power output in each module cannot be regulated with the above methods and only a single module (or part of the modules) is used to compensate for all the transients or power variations, which may limit the converter operating range. To achieve both simultaneous regulations of both output current and power sharing through all the modules together, a method proposed in [10] is to optimize current regulation in module controllers by mitigating current measurement errors and DC voltage mismatches. But module controllers with the same control objective could be conflicting, as errors and mismatches could not be eliminated completely. Another commonly used control strategy is to add an output LC filter to each module so that each module can control its output voltage independently as an AC signal instead of a pulse signal [11]–[14]. Extra LC filters eliminate the need of coordinating all the modules at the switching level, which in turn eliminates the need for high speed communication link. The control strategy in [11] utilizes the local voltage controller along with a virtual droop resistance in each module, but it requires a resistive impedance to connect to the grid. Authors in [12] proposed a decentralized control strategy, where by emulating a virtual resistive output impedance in each module, the active and reactive power output of each module is regulated by dynamically updating the amplitude and phase of its output voltage, respectively. However, the controller coefficient needs to be properly designed to ensure sufficient damping for the overall stability of the entire system. In [13], [14], a power factor-frequency inverse droop control strategy is proposed to

TABLE I: Distributed Control Methods for CHB Converter

Methods	Advantages	Disadvantages
Directly regulate the current through one (or multiple) modules, while the remaining modules only provide grid voltage support in open-loop control [5]–[8].	No need for communication. Simplified system architecture with high reliability and low cost.	The power output in each module cannot be regulated. A single module (or part of the modules) compensates all power variations.
Apply a hybrid current controller for each module and choose one module to regulate current at a time [9].	Applicable to any applications using CHB, MMC, or any modular converter.	The power output in each module cannot be regulated.
Optimize current regulation in module controllers by mitigating current measurement errors and DC voltage mismatches [10].	Achieve regulations of both output current and power sharing among modules simultaneously.	The module current controllers with the same control objective could be conflicting.
Add an output LC filter to each module. Emulate a virtual resistive output impedance in each module [11], [12].	Easy to accomplish. Achieve regulations of both output current and power sharing among modules simultaneously.	It requires a resistive impedance to connect to the grid. Controller coefficients need to be properly designed to ensure sufficient damping for stability.
Add an output LC filter to each module. Power factor-frequency inverse droop control strategy [13], [14].	No need for communication. Simplified control architecture.	It only works for standalone inverter and cannot be applied to grid-tied applications.

generate the desired voltage reference, which does not need any communication. Power sharing among modules is realized when all the modules have the same phase angle. However, This method only works for standalone inverter and cannot be applied to grid-tied applications.

For the CHB converter with integrated BESS, it is necessary to inject a current with good quality into the grid while maintaining a desired output power ratio among modules. As the battery state of charge (SOC) of different modules may diverge from each other due to different operation demands, self-discharging rates, operating temperatures, etc, the ability of distributing different output power ratios among modules is important to balancing the SOC of modules. This can improve the energy utilization and extend the operating life of the BESS. Existing strategies of power and battery SOC control for CHB-BESS generally require that each module communicates with all the other modules to exchange information [15]–[17].

In this paper, we extend the work in [18] and present an improved distributed architecture consists of three levels, namely primary control, secondary control, and battery SOC balancing control, respectively. The hierarchical distributed control architecture realizes all desirable features for the grid-tied CHB converter mentioned in the literature review. We use decentralized primary control to guarantee good current tracking performance. The secondary control based on consensus algorithm is improved to achieve the desired output voltage and power sharing regulation among modules. Our control algorithm has no need for an output LC filter and reduces the requirement on the communication network among modules compared with centralized control strategies. A sparse communication network with low bandwidth communication frequency is sufficient. Moreover, system stability analysis for power control level is performed to ensure the stability of the proposed distributed control. Considering the application of BESS, the secondary power control is further utilized to balance battery SOC. Additionally, a novel software platform, Resilient Information Architecture Platform for Smart Systems (RIAPS), is used to implement the proposed distributed control scheme and achieve the carrier phase shift (CPS) control between modules.

Three main technical contributions are presented in this paper. First, we apply the consensus algorithm for CHB

converter to realize proportional power sharing regulation of each module. The proposed algorithm only needs sparse communication among neighboring modules. Although consensus algorithm has been widely used in microgrid control [19], to our best knowledge, it has not been applied for CHB converter control. Second, we provide the stability proof of the proposed control scheme. Third, we extend the secondary power control to realize the battery SOC balancing. Experiment results are provided to validate the proposed control scheme.

The rest of the paper is organized as follows: Section II-IV introduce primary control, secondary control and battery SOC balancing control, respectively. Experimental implementation and results are presented in Section V and VI respectively. Section VII concludes the work.

II. PRIMARY CONTROL SCHEME

A single-phase CHB converter with integrated batteries and its control block diagram are shown in Fig. 1. It has N H-bridge modules connected in series with a filter inductor L_f . As the fundamental level of the proposed distributed control architecture, primary control maintains a stable and accurate current tracking. The corresponding control scheme is depicted in the primary control part of Fig. 1.

In primary control, one single module, i.e. module 1 in Fig. 1, is named as current control module (CCM) and controls the converter output current i_g . A digital phase lock loop (PLL) produces a grid synchronized reference sine signal $\sin \hat{\theta}$. The output current reference i_{ref} is generated by multiplying the current amplitude reference, I^* with the sine signal $\sin \hat{\theta}$. The output current i_g is then regulated by a PR controller. The current control block diagram is shown in Fig. 2. In s domain, the duty cycle of CCM can be written as:

$$d_1(s) = \left(k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega^2} \right) (i_{\text{ref}}(s) - i_g(s)) \quad (1)$$

where k_p, k_r, ω_c , are parameters of the PR controller.

Due to the series connection, all modules share the same current, and simultaneous regulation of the current by two or more modules could destabilize the system. Therefore, only one CCM is allowed, while the other modules, i.e. module i ($i = 2, 3, \dots, N$) in Fig. 1, are controlled in an open-loop manner. These modules are called voltage control

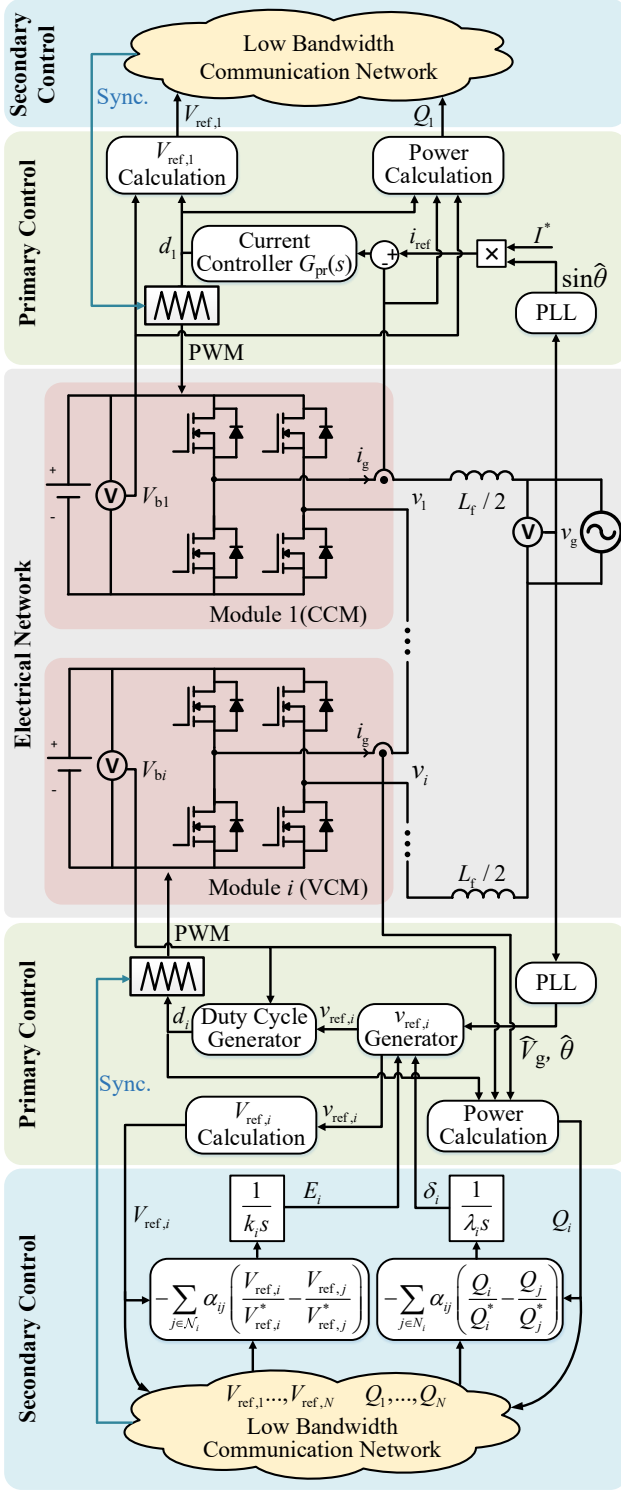


Fig. 1: The topology and distributed control architecture of single phase CHB converter

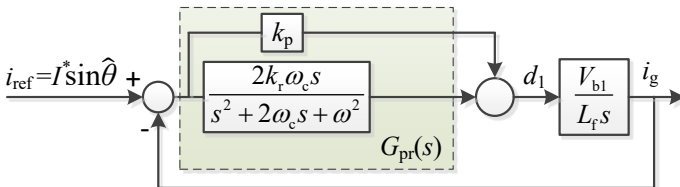


Fig. 2: The current control block diagram in the primary control

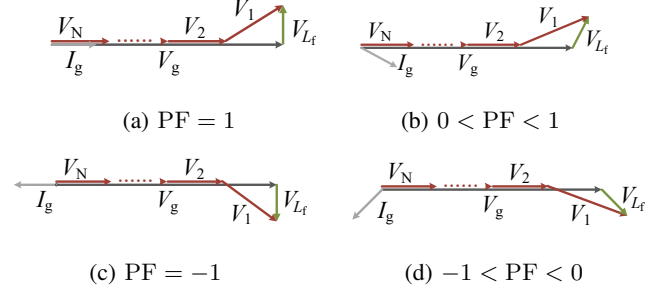


Fig. 3: The voltage vector diagram of different modules with only primary control under different conditions

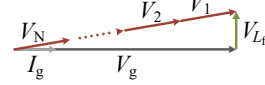


Fig. 4: The voltage vector diagram under balanced condition

module (VCM). The reference output voltage for each VCM is designed as,

$$v_{\text{ref},i} = \frac{1}{N} v_g = \frac{\hat{V}_g}{N} \sin \hat{\theta} \quad (2)$$

where $\hat{V}_g$ and $\hat{\theta}$ are grid voltage amplitude and phase tracked by PLL, respectively.

In steady state, all the VCMs' output voltage build up a total fundamental AC voltage $v_g(N-1)/N$. The remained voltage mismatch v_g/N and the voltage drop across filter inductance v_{L_f} are compensated by the CCM. The desired fundamental component of CCM output voltage in steady state is,

$$v_1 = \frac{1}{N} v_g + v_{L_f} = \frac{1}{N} v_g + j\omega L_f i_g \quad (3)$$

Fig. 3 shows the voltage vector diagram of different modules with only primary control under different conditions. Fig. 3a shows the nominal operation condition at unity power factor (PF). VCMs have the same output voltage in the same phase of grid voltage, and the output voltage of CCM differs due to the filter inductor. If PF changes, the amplitude and phase of the output voltage for CCM change accordingly while the VCMs' output voltage remains unchanged, as shown in Fig. 3b-d. The output voltages of VCMs are aligned with grid voltage while the CCM compensates for voltage transients and voltage drop on the filter inductor. Therefore, CCM injects/absorbs different active and reactive power to/from the grid compared with VCMs. With only primary control, the output voltage, and thus the output power among modules will be unbalanced, which can result in unbalanced battery SOC. Moreover, the CCM is more prone to overload or overshoot than VCMs, which affects the dynamic performance of the control and results in a reduced utilization of the converter.

III. SECONDARY CONTROL SCHEME FOR POWER REGULATION

To regulate the active and reactive power output of each module as desired, a secondary control layer is proposed. The amplitude and phase of the output voltage for each module

should be controlled as desired, e.g. balance operation as shown in Fig. 4. Next, we first introduce the graph theory and distributed consensus algorithm. Then, the consensus-based secondary control scheme is described and the realization of proportional power sharing among modules is interpreted. Finally, the stability analysis is presented.

A. Graph Theory and Consensus Algorithm Preliminaries

A communication network can be modeled by an undirected graph $G = (\mathcal{V}, \mathcal{E})$, with $\mathcal{V} = \{n_1, n_2, \dots, n_N\}$ being the set of nodes, $\mathcal{E} \subseteq \{(n_i, n_j) \in \mathcal{V} \times \mathcal{V}\}$ being the set of edges. Define $\mathcal{A}$ as a corresponding $N \times N$ adjacency matrix with $\alpha_{ij} = \alpha_{ji} > 0$ if and only if the i th and j th node can communicate directly with each other, i.e., $(n_i, n_j) \subseteq \mathcal{E}$, otherwise $\alpha_{ij} = \alpha_{ji} = 0$. The indices of the nodes that are interconnected to node n_i directly form its neighboring set, denoted by $\mathcal{N}_i = \{j \mid (n_i, n_j) \subseteq \mathcal{E}\}$. If a path exists between any two nodes, it is called a connected graph.

Each node n_i ($i = 1, 2, \dots, N$) of the graph represents an agent that holds a state x_i . To achieve consensus of a multi-agent system (MAS), consensus algorithms can be used [20],

$$\dot{x}_i = - \sum_{j \in \mathcal{N}_i} \alpha_{ij} (x_i - x_j) \quad (4)$$

For a connected graph $G = (\mathcal{V}, \mathcal{E})$, when consensus is achieved, all state variables x_i converge to a common value, i.e., $x_i = x_j$ for any i and j [21].

If one leading agent is controlled by an external controller without obeying (4), while other agents still obey (4), it sets up a “leader-follower” relationship in consensus algorithm [22]. In this case, the states of the agents can be controlled by regulating the motion of the leader agent [23].

B. Secondary Control and Proportional Power Sharing

We use an undirected and connected graph $G = (\mathcal{V}, \mathcal{E})$ to model the communication network of the CHB converter. Every agent represents a module, and the edge depicts the communication channel among modules.

The proposed secondary control scheme is depicted in the secondary control part of Fig. 1 and it exploits the “leader-follower” relationship in the consensus algorithm. The CCM acts as the leader and controls the converter output current, whereas VCMs act as followers and regulate the output voltage by:

$$v_{\text{ref},i} = \left(\frac{\hat{V}_g}{N} + E_i \right) \sin(\hat{\theta} + \delta_i) \quad (5a)$$

$$k_i \frac{dE_i}{dt} = - \sum_{j \in \mathcal{N}_i} \alpha_{ij} \left(\frac{V_{\text{ref},i}}{V_{\text{ref},i}^*} - \frac{V_{\text{ref},j}}{V_{\text{ref},j}^*} \right) \quad (5b)$$

$$\lambda_i \frac{d\delta_i}{dt} = - \sum_{j \in \mathcal{N}_i} \alpha_{ij} \left(\frac{Q_i}{Q_i^*} - \frac{Q_j}{Q_j^*} \right) \quad (5c)$$

where for module i ($i = 2, 3, \dots, N$) that acts as VCM, E_i, δ_i are secondary control variables, k_i, λ_i are positive gains; for any module i ($i = 1, 2, \dots, N$), $V_{\text{ref},i}$ is the amplitude of $v_{\text{ref},i}$, Q_i is the reactive power output, $V_{\text{ref},i}^*$

is voltage ratio variable, Q_i^* is reactive power ratio variable. $V_{\text{ref},1}^* : V_{\text{ref},2}^* : \dots : V_{\text{ref},N}^*$ is the desired output voltage ratio between modules. $Q_1^* : Q_2^* : \dots : Q_N^*$ is the desired reactive power ratio between modules. The $N \times N$ matrix $\mathcal{A} = [\alpha_{ij}]$ is the adjacency matrix of the communication network. $\mathcal{N}_i$ represents the neighboring set of the module i .

For the followers, i.e. VCMs, the output voltage is regulated by the secondary controller (5a)-(5c). The open-loop-control voltage reference for VCMs is generated using (5a) with secondary control variables E_i and δ_i . The control gains k_i and λ_i correspond for the secondary control convergence speed. For the leader, i.e. the CCM, its output voltage is determined by the current controller (1). The secondary controller requires the i th VCM to obtain $V_{\text{ref},j}$ and Q_j from all its neighbors. Thus, the CCM should calculate and share its information to the communication network.

Considering the steady state of the secondary controller, the derivatives should be zero, which is satisfied when

$$\frac{V_{\text{ref},1}}{V_{\text{ref},1}^*} = \frac{V_{\text{ref},2}}{V_{\text{ref},2}^*} = \dots = \frac{V_{\text{ref},N}}{V_{\text{ref},N}^*} \quad (6a)$$

$$\frac{Q_1}{Q_1^*} = \frac{Q_2}{Q_2^*} = \dots = \frac{Q_N}{Q_N^*} \quad (6b)$$

The primary control includes an inner current loop in CCM and open-loop voltage generation in VCMs. The primary control has a much higher control bandwidth, i.e. at least a decade higher than the fundamental frequency. Therefore, for the analysis of secondary control, i.e. power regulation loops, the dynamics of primary control are ignored. Perfect voltage and current reference tracking is assumed, i.e., $V_i = V_{\text{ref},i}$ and $I_g = I^*$, where V_i is the amplitude of fundamental component of module i 's output voltage in steady state and I_g is the amplitude of fundamental component of converter output current. The output active and reactive power of the i th module can be presented as:

$$P_i = \frac{1}{2} V_i I_g \cos \delta_i = \frac{1}{2} V_{\text{ref},i} I^* \cos \delta_i \quad (7a)$$

$$Q_i = \frac{1}{2} V_i I_g \sin \delta_i = \frac{1}{2} V_{\text{ref},i} I^* \sin \delta_i \quad (7b)$$

Based on equation (6), (7) and the fact δ_i is very small such that $\sin \delta_i \approx \delta_i$ and $\cos \delta_i \approx 1$, it can be further derived that,

$$\frac{P_1}{V_{\text{ref},1}^*} = \frac{P_2}{V_{\text{ref},2}^*} = \dots = \frac{P_N}{V_{\text{ref},N}^*} \quad (8)$$

The proportional power sharing regulation is thus realized by the secondary controller in steady state. As a special case, equal power sharing, as shown in Fig. 4, can be realized if identical $V_{\text{ref},i}^*$ and Q_i^* are given for each module.

C. System Stability Analysis

To verify the stability of the proposed control strategy and derive sufficient conditions for stable operation, the system small signal model and stability analysis are presented.

Referring to the secondary controller (5a)-(5c), there are $2(N-1)$ state variables, E_i and δ_i ($i = 2, 3, \dots, N$), respectively. Since E_1 and δ_1 in CCM are not state variables, CCM is separated from system modeling to facilitate the

stability analysis. A parameter r_i is defined to characterize the communication between CCM and other modules. When i th module communicates directly with CCM, $r_i = 1$, otherwise $r_i = 0$. The converter under the proposed control scheme can be modeled as:

$$k_i \dot{E}_i = - \sum_{j \in \mathcal{N}_i} \alpha_{ij} \left(\frac{V_{\text{ref},i}}{V_{\text{ref},i}^*} - \frac{V_{\text{ref},j}}{V_{\text{ref},j}^*} \right) - r_i \left(\frac{V_{\text{ref},i}}{V_{\text{ref},i}^*} - \frac{V_{\text{ref},1}}{V_{\text{ref},1}^*} \right) \quad (9a)$$

$$\lambda_i \dot{\delta}_i = - \sum_{j \in \mathcal{N}_i} \alpha_{ij} \left(\frac{Q_i}{Q_i^*} - \frac{Q_j}{Q_j^*} \right) - r_i \left(\frac{Q_i}{Q_i^*} - \frac{Q_1}{Q_1^*} \right) \quad (9b)$$

From (5a), $V_{\text{ref},i}$ can be expressed as:

$$V_{\text{ref},i} = \frac{\hat{V}_g}{N} + E_i \quad (10)$$

The small-signal model of (9a) is derived by substituting (10) into (9a):

$$k_i \dot{E}_i = - \sum_{j \in \mathcal{N}_i} \alpha_{ij} (E'_i - E'_j) - r_i (E'_i - E'_1) + \Delta_E \quad (11)$$

where $E'_m = E_m / V_{\text{ref},m}^*$ ($m = i, j, 1$); $\Delta_E = - \sum_{j \in \mathcal{N}_i} \alpha_{ij} \left(\frac{\hat{V}_g/N}{V_{\text{ref},i}^*} - \frac{\hat{V}_g/N}{V_{\text{ref},j}^*} \right) - r_i \left(\frac{\hat{V}_g/N}{V_{\text{ref},i}^*} - \frac{\hat{V}_g/N}{V_{\text{ref},1}^*} \right)$ is a constant and is irrelevant to system states.

If taking the approximation that $\sin \delta_i \approx \delta_i$ and $V_1 + V_2 + \dots + V_N = V_g$, i.e., $E_1 + E_2 + \dots + E_N = 0$, E_1 in CCM can be expressed as:

$$E_1 = - \sum_{i=2}^N E_i \quad (12)$$

If the speed of controller (5c) is designed as much faster than that of controller (5b), it can be assumed that $E_1 = E_2 = \dots = E_N = 0$ for angle stability analysis. According to (7b),

$$Q_i = \frac{\hat{V}_g I^*}{2N} \delta_i \quad (13)$$

Substituting (13) into (9b):

$$\lambda_i \dot{\delta}_i = \frac{\hat{V}_g I^*}{2N} \left[- \sum_{j \in \mathcal{N}_i} \alpha_{ij} \left(\frac{\delta_i}{Q_i^*} - \frac{\delta_j}{Q_j^*} \right) - r_i \left(\frac{\delta_i}{Q_i^*} - \frac{\delta_1}{Q_1^*} \right) \right] \quad (14)$$

From the system voltage vector diagram, it can be obtained that

$$V_g + j\omega L_f I^* = \sum_{i=1}^N \frac{\hat{V}_g}{N} (\cos \delta_i + j \sin \delta_i) \quad (15)$$

Due to the same imaginary part and small power factor angle, δ_1 in CCM can be presented as:

$$\delta_1 = \frac{N\omega L_f I^*}{\hat{V}_g} - \sum_{i=2}^N \delta_i \quad (16)$$

From (11), (12), (14) and (16), the model of converter system with the proposed controller can be summarized as

$$\begin{cases} k_i \dot{E}_i = - \sum_{j \in \mathcal{N}_i} \alpha_{ij} \left(\frac{E_i}{V_{\text{ref},i}^*} - \frac{E_j}{V_{\text{ref},j}^*} \right) - r_i f(E_i) + \Delta_E \\ \lambda_i \dot{\delta}_i = \frac{\hat{V}_g I^*}{2N} \left[- \sum_{j \in \mathcal{N}_i} \alpha_{ij} \left(\frac{\delta_i}{Q_i^*} - \frac{\delta_j}{Q_j^*} \right) - r_i f(\delta_i) \right] + \Delta_\delta \end{cases} \quad (17)$$

where $f(E_i) = \frac{E_i}{V_{\text{ref},i}^*} + \frac{\sum_{i=2}^N E_i}{V_{\text{ref},1}^*}$ is a function of E_i , $f(\delta_i) = \frac{\delta_i}{Q_i^*} + \frac{\sum_{i=2}^N \delta_i}{Q_1^*}$ is a function of δ_i , $\Delta_\delta = r_i \frac{\omega L_f I^{*2}}{2Q_1^*}$ is a constant that is irrelevant to system states.

The system model in (17) could be written in matrix form:

$$\dot{\mathbf{x}} = \mathbf{W}\mathbf{x} + \mathbf{u} \quad (18)$$

where $\mathbf{x} = [\mathbf{E} \ \delta]^T$ represents system state variables under analysis and the system matrix $\mathbf{W}$ is

$$\mathbf{W} = \begin{bmatrix} -k_i^{-1} \mathbf{W}_E & \mathbf{0}_{N-1} \\ \mathbf{0}_{N-1} & -\lambda_i^{-1} \frac{\hat{V}_g I^*}{2N} \mathbf{W}_\delta \end{bmatrix} \quad (19)$$

where $\mathbf{0}_{N-1}$ represents a $(N-1)$ -by- $(N-1)$ zero matrix;

$$\mathbf{W}_E = (\mathbf{L} + 2\mathbf{R}) \left[\frac{\mathbf{1}}{\mathbf{V}_{\text{ref},i}^*} \right] + \frac{1}{V_{\text{ref},1}^*} \mathbf{R}[\mathbf{1}]_{N-1} \quad (20a)$$

$$\mathbf{W}_\delta = (\mathbf{L} + 2\mathbf{R}) \left[\frac{\mathbf{1}}{\mathbf{Q}_i^*} \right] + \frac{1}{Q_1^*} \mathbf{R}[\mathbf{1}]_{N-1} \quad (20b)$$

where $\left[\frac{\mathbf{1}}{\mathbf{V}_{\text{ref},i}^*} \right] = \text{diag} \left(\frac{1}{V_{\text{ref},i}^*} \right)$ and $\left[\frac{\mathbf{1}}{\mathbf{Q}_i^*} \right] = \text{diag} \left(\frac{1}{Q_i^*} \right)$ are diagonal matrices; $\mathbf{L}$ is the Laplacian matrix of an undirected communication graph with $(N-1)$ vertices, which represents the communication network structure among modules; $\mathbf{R} = \text{diag}(r_i)$ reflects the communication structure between CCM and VCMs; $[\mathbf{1}]_{N-1}$ represents a $(N-1) \times (N-1)$ all ones matrix; $V_{\text{ref},1}^*$ and Q_1^* are constants.

The system is exponentially stable if and only if all the eigenvalues of $\mathbf{W}$ have strictly negative real parts. From (19), the sufficient condition for system stability is that the matrix $\mathbf{W}_E$ and $\mathbf{W}_\delta$ are positive definite, i.e. the quadratic form of $\mathbf{W}_E$ and $\mathbf{W}_\delta$ is always greater than 0.

If $\mathbf{L}$ is a laplacian matrix of an undirected and connected graph, it satisfies the property, $X^T \mathbf{L} X = \frac{1}{2} \sum_{i,j \in G} \alpha_{ij} (x_i - x_j)^2$ for any non-zero real vector X [21]. Thus, the quadratic form of the matrix $(\mathbf{L} + 2\mathbf{R})$ can be written as:

$$X^T (\mathbf{L} + 2\mathbf{R}) X = \frac{1}{2} \sum_{i,j=1}^{N-1} \alpha_{ij} (x_i - x_j)^2 + \sum_{i=1}^{N-1} r_i x_i^2 \quad (21)$$

The equation (21) consists of two added components, both of which are always greater than or equal to 0. If and only if all elements of vector X are the same, i.e., $x_i = x_j (\forall i, j)$, the first component of (21) will be equal to zero. If and only if $x_i = 0$ for all $r_i \neq 0$, the second component will be equal to zero. It

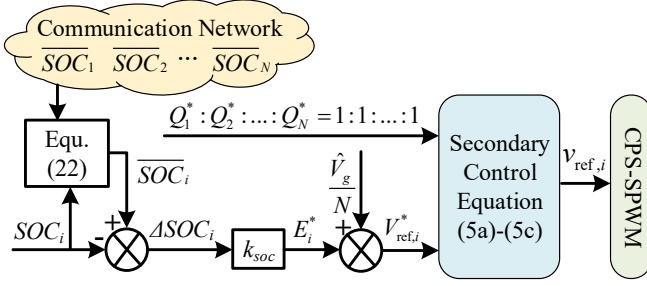


Fig. 5: The block diagram of SOC balancing control

can be concluded that the two components cannot be equal to zero at the same time for a connected communication graph, where there exists $r_i \neq 0$. In other words, $X^T(\mathbf{L} + 2\mathbf{R})X > 0$ is always satisfied with the connected communication network. Thus, the matrix $(\mathbf{L} + 2\mathbf{R})$ is a positive definite matrix. Based on similar matrix theorem, the matrix $(\mathbf{L} + 2\mathbf{R}) \begin{bmatrix} 1 \\ \mathbf{V}_{\text{ref},i}^* \end{bmatrix}$ is also positive definite. Moreover, it can be easy to find that $\frac{1}{V_{\text{ref},1}^*} \mathbf{R}[1]_{N-1}$ is a positive semidefinite matrix. From these points, it can be concluded that $\mathbf{W}_E$ in (20a) is positive definite since $\mathbf{W}_E$ is the summation of a positive definite matrix and a positive semidefinite matrix.

Similarly, $\mathbf{W}_\delta$ can be derived to be a positive definite matrix by the same approach. Therefore, the proposed control scheme is stable if a connected communication structure is satisfied.

Based on the above stability analysis, it is noteworthy that the proposed secondary control does not require a fully connected communication network, under which each module can communicate with any other modules. Power sharing regulation among modules can be achieved with a sparse communication network. A typical example is that each module only communicates with its neighbor modules [24].

IV. BATTERY SOC BALANCING CONTROL

For a BESS, the SOC values of different battery modules may diverge from each other due to different operation demands, self-discharging rates, operating temperature, etc. The battery SOC imbalance can result in degraded utilization and overdischarge/overcharge for some batteries. To avoid this issue, the proposed distributed control is utilized to achieve the battery SOC balancing. The control block diagram of SOC balancing is shown in Fig. 5.

The average SOC of all battery modules, $\overline{SOC}_i$, is estimated in each module using dynamic average consensus algorithm [25], which is able to track the average of a set of time-varying states in a distributed manner,

$$\dot{\overline{SOC}}_i(t) = \dot{SOC}_i(t) - \sum_{i,j \in \mathcal{N}_i} \alpha_{ij} [\overline{SOC}_i(t) - \overline{SOC}_j(t)] \quad (22)$$

In steady state, it can be satisfied that

$$\overline{SOC}_i(t) = \frac{1}{N} \sum_{j=1}^N SOC_j(t) \quad (23)$$

With the estimated average SOC, the difference between estimated average and the actual SOC value of each battery module can be obtained as ΔSOC_i . Then, ΔSOC_i is used in (24) to obtain the voltage ratio variable, $V_{\text{ref},i}^*$.

$$V_{\text{ref},i}^* = k_{\text{soc}} \Delta SOC_i + \frac{\hat{V}_g}{N} = k_{\text{soc}} (\overline{SOC}_i - SOC_i) + \frac{\hat{V}_g}{N} \quad (24)$$

Then, $V_{\text{ref},i}^*$ is used in the active power secondary controller (5b) to generate the secondary control variable E_i . The reactive power ratio is set to be $Q_1^* : Q_2^* : \dots : Q_N^* = 1 : 1 : \dots : 1$ to share the reactive power equally among modules.

If all components are assumed to be lossless, for each module, the battery power is equal to its output power,

$$V_{bi} I_{bi} = P_i = \frac{P_i^*}{\sum_{i=1}^N P_i^*} \left(\frac{1}{2} V_g I^* \right) \quad (25)$$

The current flowing through the battery module i is also related to the battery SOC by

$$I_{bi} = C \left(\frac{dSOC_i}{dt} \right) \quad (26)$$

where C is the nominal capacity of the battery modules. By substituting (26) into (25), the following equation can be derived,

$$\frac{dSOC_i}{dt} = \frac{P_i^*}{\sum_{i=1}^N P_i^*} \left(\frac{V_g I^*}{2CV_{bi}} \right) \quad (27)$$

Combining (8) with (27), it can be concluded that the battery SOC can be regulated by dynamically controlling the value of $V_{\text{ref},i}^*$ under the same Q_i^* : Larger value of $V_{\text{ref},i}^*$ will result in faster battery SOC change rate, and vice versa. It is desirable that, in the discharging operation mode, the module with higher SOC provides more power and, in the charging operation mode, the module with lower SOC absorbs more power than the others. Thus, the SOC balancing control coefficient k_{soc} should be set to be negative in the discharging mode, and positive in the charging mode.

For tuning the controller parameters, clear time-scale separations between each control layer should be guaranteed to allow the proper operation of the hierarchical control structure. For the secondary control, the corresponding gains, k_i and λ_i , are tuned so that the convergence speed is at least 10 times slower than the dynamics of the primary control but hundreds of times faster than the SOC balancing control. For SOC balance, the corresponding gain, k_{soc} , should be tuned so that its dynamics is the slowest of the hierarchical architecture. This is because the charge/discharge of the battery packs generally takes several hours.

V. CHB HARDWARE IMPLEMENTATION

To verify the performance of the proposed distributed control method, a CHB converter with one CCM and two VCMs is constructed, as shown in Fig. 6.

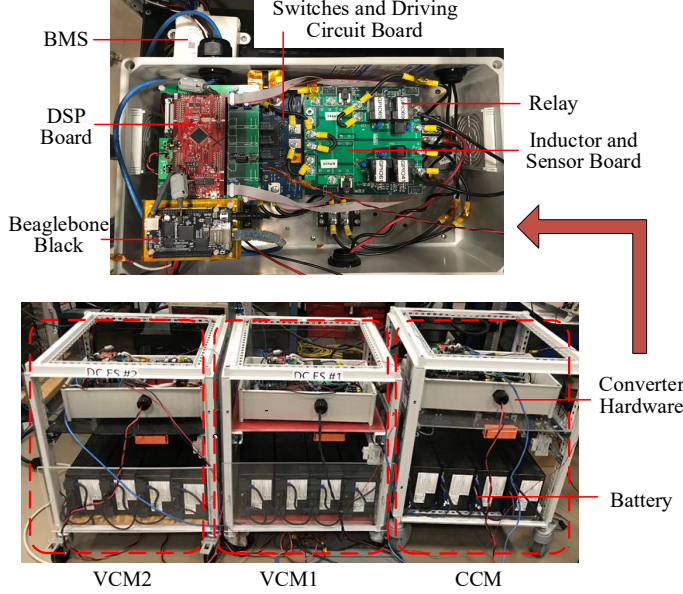


Fig. 6: Hardware with one CCM and two VCMs

TABLE II: Experimental Parameters

Electrical Parameters	
Grid Frequency f	60Hz
Grid Nominal Voltage V_g	120 V _{rms}
Battery Nominal Voltage V_b	138 V
Battery Nominal Capacity C	20 Ah
Filter Inductance L_f	550×3 μ H
Switching Frequency f_s	37.5 kHz
Sync. Pulse Signal Frequency	750 Hz
Secondary Controller Data Frequency	5 Hz
SOC Balancing Control Data Frequency	5 Hz
Controller Parameters	
Current PR controller Proportional gain k_p	0.07
Current PR controller Resonant gain k_r	5
Secondary Controller Coeff. k_i	0.2
Secondary Controller Coeff. λ_i	100
SOC Control Coeff. k_{soc}	0.7

A. Hardware Setup and Controller Implementation

The DC side of each module is connected to a *SCiBTM* battery pack from Toshiba. Each battery pack is equipped with a battery management system (BMS) to monitor the battery's status and estimate SOC. The converter output is connected to the 120V_{rms}/60Hz grid via an inductor. The electrical and controller parameters are listed in Table II. The switching frequency f_s was set to 37.5 kHz. SiC MOSFET CCS050M12CM2 from Wolfspeed is used.

The primary control is implemented in digital signal processors (DSPs) TMS320F28377S from Texas Instrument. A PR current controller is used in the CCM to achieve current regulation with high bandwidth and large phase margin. The data used for the secondary control and SOC balancing control are calculated in the DSPs and sent to the communication network at a frequency of 5 Hz.

The secondary control and SOC balancing control are implemented using the RIAPS platform. The RIAPS platform is a distributed control platform that allows real-time messaging and high precision synchronization. More information about the RIAPS platform and its synchronization capability can

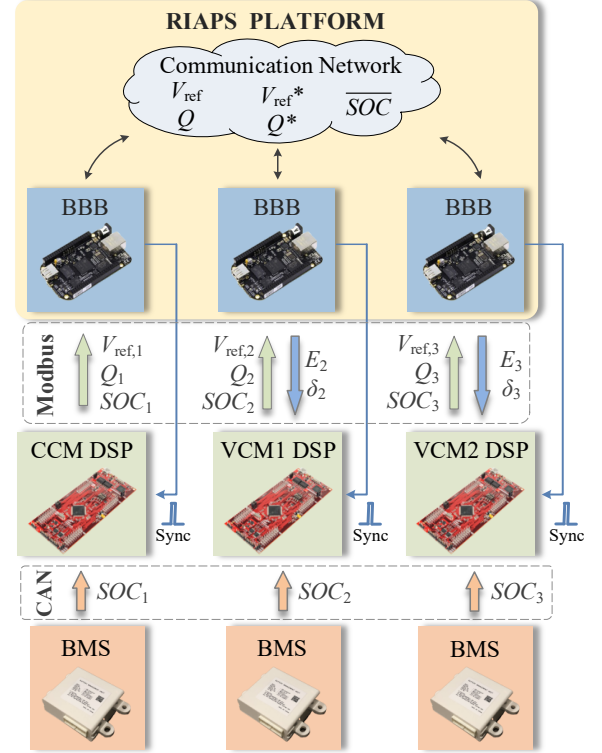


Fig. 7: The implementation of distributed control system

be found in [26]. The hardware for the RIAPS node is Beaglebone Black (BBB) single-board computer. Each BBB can communicate with its DSP using Modbus protocol.

Fig. 7 shows the implementation of the proposed control system and its communication channels. At every time step, the BBB sends a Modbus message to pull $V_{ref,i}$ and Q_i calculated by the DSP and battery SOC. Then, based on (5a) - (5c) and (24), each BBB calculates E_i , δ_i and sends them back to the DSP to modify VCMs' voltage reference. At the same time, $V_{ref,i}$, $V_{ref,i}^*$, Q_i and Q_i^* are published to the RIAPS network to be shared with other RIAPS nodes. The relevant data, such as battery SOC, secondary control variables, etc, are acquired and stored in real-time by the RIAPS platform.

B. Carrier Phase Shift Control

In order to achieve multilevel output voltage and harmonic reduction, CPS modulation is widely used for CHB converter. The carrier of each module has a phase shift, $2\pi/N$, from its adjacent module. CPS modulation is easy to implement if all the modules are controlled by a central controller. However, for distributed control, each module implements the modulation independently without a central controller. The internal clocks in different module controllers cannot be accurately synchronized due to crystal frequency drift and difference in operating conditions. As a result, the applied carrier frequency would differ from module to module and the phase shift between modules is time-varying.

To deal with this issue, a CPS control shown in Fig. 8 is used to achieve carrier frequency synchronization and desired CPS among modules. A global synchronization pulse signal

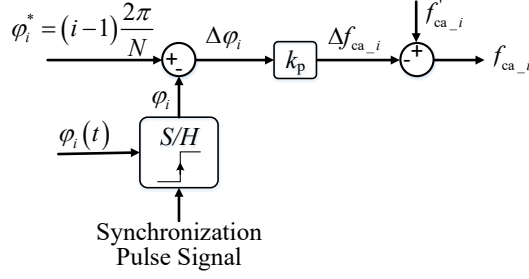


Fig. 8: The block diagram of CPS control

for all modules occurring simultaneously is used to realize the CPS control. Once receiving the synchronization pulse signal, the module controller samples and holds the carrier phase φ_i at that moment, which is then compared with the desired CPS, $\varphi_i^* = (i-1) \frac{2\pi}{N}$. The obtained error, $\Delta\varphi_i$ is multiplied by a positive coefficient k_p . The output, Δf_{ca_i} is used to fine-tune the carrier frequency. The applied carrier frequency can be expressed as $f_{ca_i} = f'_{ca_i} - \Delta f_{ca_i}$, where f'_{ca_i} is the unadjusted carrier frequency. In steady state, the applied carrier frequency f_{ca_i} will be the same for all modules and the CPS φ_i will be controlled to the desired value.

The RIAPS platform uses a fault-tolerant method to generate synchronized pulses at different BBBs with a time error less than $1 \mu s$ [27]. If one RIAPS node fails to generate a synchronization signal, all the healthy nodes will still work with their phase shift. The whole phase shift control will work at a sub-optimal point rather than having zero interleaving effect. This is an embedded feature of distributed control algorithms. The RIAPS platform guarantees an accurate synchronization signal used to implement the CPS control. The synchronization pulse signal is sent from the RIAPS platform to DSPs at $f_s/50$ frequency, which is experimentally found to be enough for DSP synchronization.

VI. EXPERIMENT RESULTS

A. CPS Control Performance

Only primary control is enabled to validate the performance of the CPS control. The current reference amplitude I^* is set to 10 A. In the first case, no CPS control is implemented. The phase difference between different modules becomes time-varying. The worst case happens when all the modules have the same carrier phase, as shown in Fig. 9. When the CPS control described in Section V-B is activated, the output voltage of the three modules have a fixed phase shift $2\pi/3$ as shown in Fig. 10. In both cases, the output current is well controlled, which indicates that the presented primary control has a good current tracking performance. The implemented CPS control can achieve a multilevel voltage output and a lower current ripple.

B. Distributed Control Performance

We validated the proposed distributed control using both a full and a sparse communication network. In the full communication network, CCM, VCM1 and VCM2 exchange

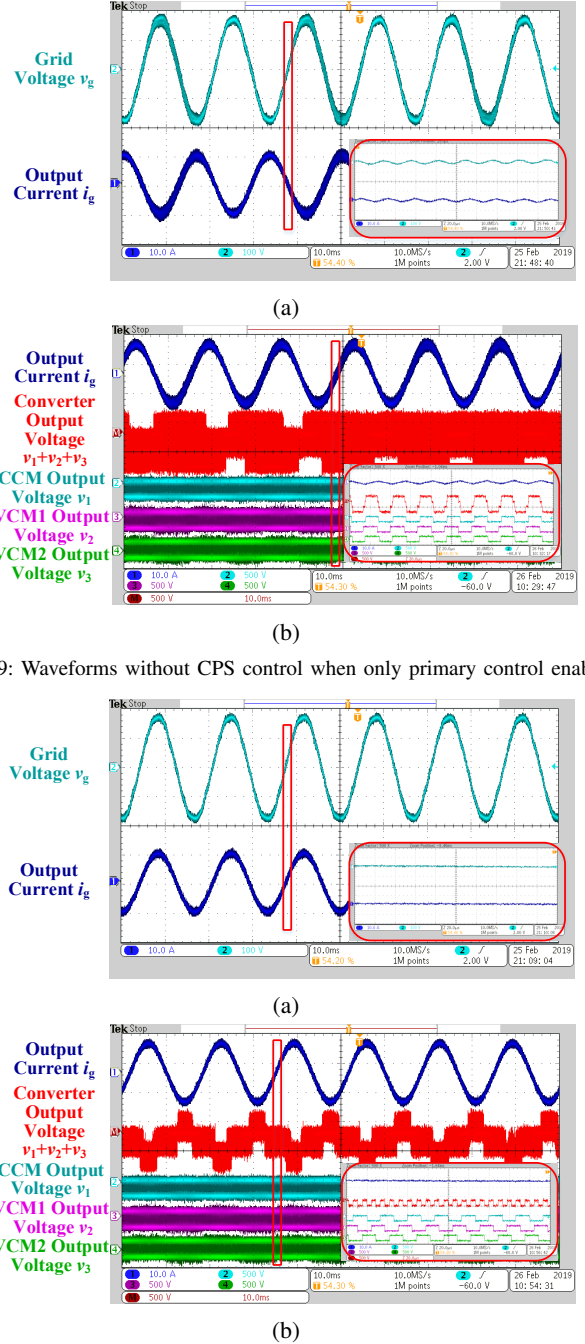


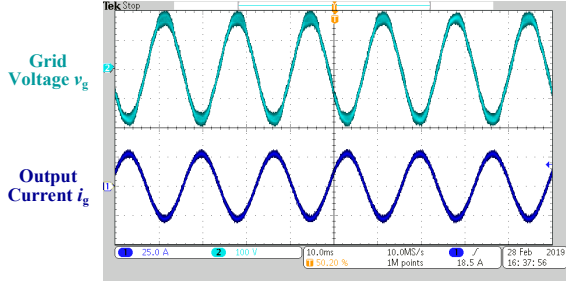
Fig. 9: Waveforms without CPS control when only primary control enabled

Fig. 10: Waveforms with CPS control when only primary control enabled

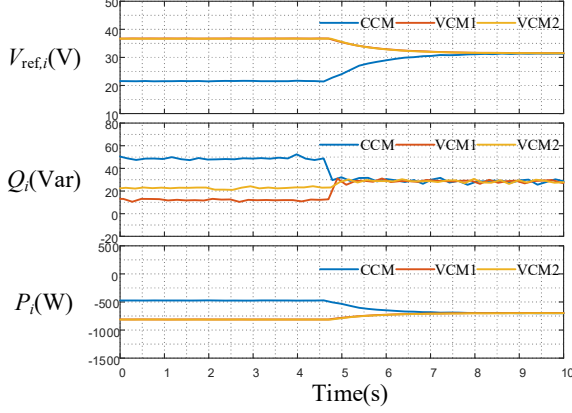
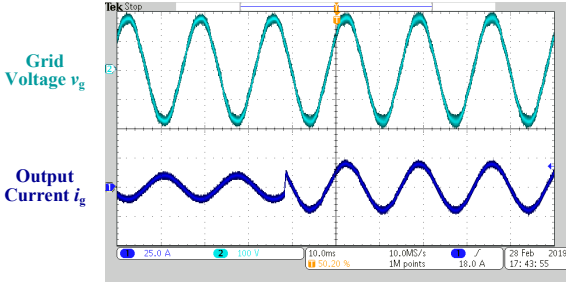
information with each other. In the sparse communication network, CCM only exchanges data with VCM1, and VCM2 only communicates with VCM1.

a) Full communication network

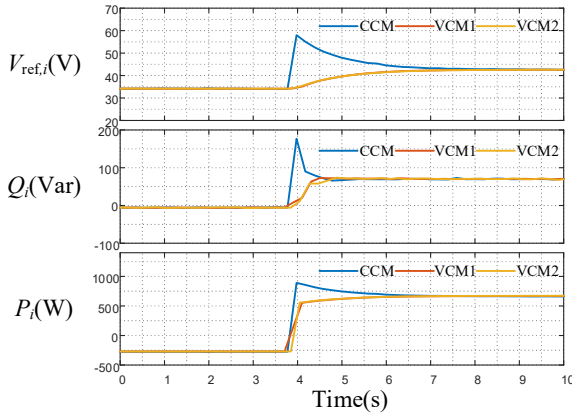
First, the secondary control is activated with primary control and CPS control enabled. The ratios of V_{ref}^* and Q^* are set to be $1 : 1 : 1$ to realize equal power sharing among modules. The experiment results are shown in Fig. 11. Comparing Fig. 11a with Fig. 10, it can be found that the current tracking performance is still good after activating the secondary control. Data transmitted in the communication network are recorded and plotted in Fig. 11b. It can be observed that the variables used in the secondary controller, V_{ref} and Q , have accurately



(a) Waveforms with CPS and secondary control activated

(b) V_{ref} , Q , P calculated by DSPsFig. 11: Experiment results when secondary control activated under the full communication network with $I^* = -28A$ 

(a) Waveforms with CPS and secondary control enabled

(b) V_{ref} , Q , P calculated by DSPsFig. 12: Experimental results when I^* steps from -10A to 20A under the full communication network

converged to the same value. For demonstration purpose, the active power output of each module is also calculated. Fig. 11b shows that the active and reactive power of different modules

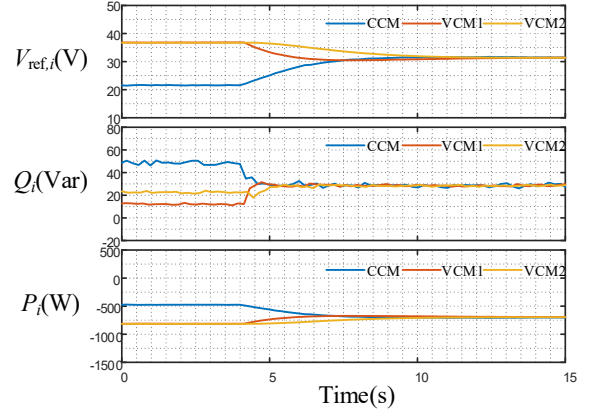
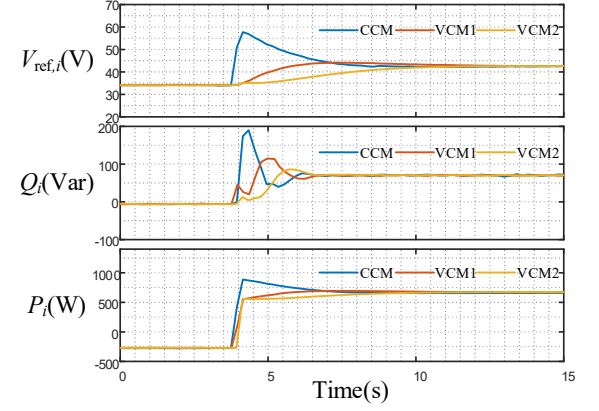
(a) When secondary control activated with $I^* = -28A$ (b) When I^* steps from -10A to 20A

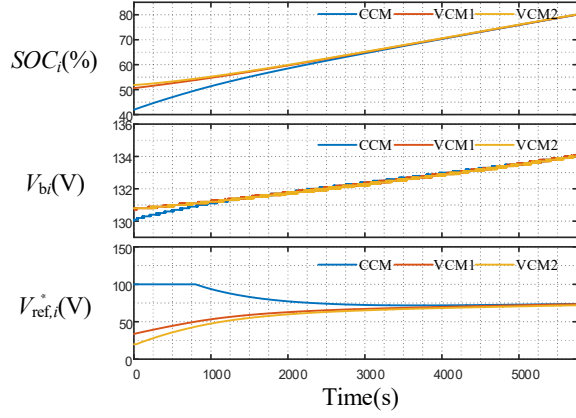
Fig. 13: Experimental results under the sparse communication network

are equalized by the proposed secondary control in steady state.

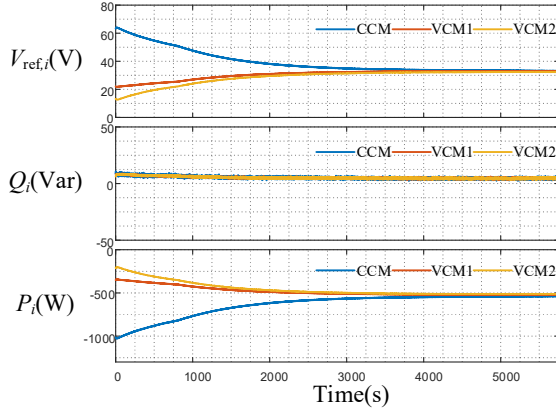
Besides, the dynamic performance of the proposed control scheme is tested by stepping the current reference amplitude I^* from -10 A to 20 A. The transient responses of the output current and output voltage are shown in Fig. 12a and the secondary control responses are shown in Fig. 12b. The output current can follow the reference step change in about 800 μs . Equal active and reactive power sharing among modules is achieved shortly after the transients.

b) Sparse communication network

Similarly, we activated the secondary control with the synchronized CPS control enabled. The ratios of V_{ref}^* and Q^* are set to be 1 : 1 : 1. The results are shown in Fig. 13a. It can be observed that V_{ref} , Q , and P converge to the same values, respectively, in 6 s. In steady state, the active and reactive power of different modules are equalized under the sparse communication network. However, comparing with Fig. 11b, the converge speed is slower and the transients are different. The reason is analyzed as follows. Under the full communication network, all modules exchange information directly with CCM so that all VCMs can get the CCMs information, i.e., V_{ref} and Q , at the same time. Thus, VCMs have identical transients since they can respond and regulate their output at the same time. Under the sparse communication network, only VCM1 communicates with CCM. Referring to



(a) SOC V_{bi} measured in BMS, V_{ref}^* calculated by BBBs



(b) V_{ref} , Q , P calculated by DSPs

Fig. 14: Experimental results of battery SOC balancing during charging operation with $I^* = -20A$

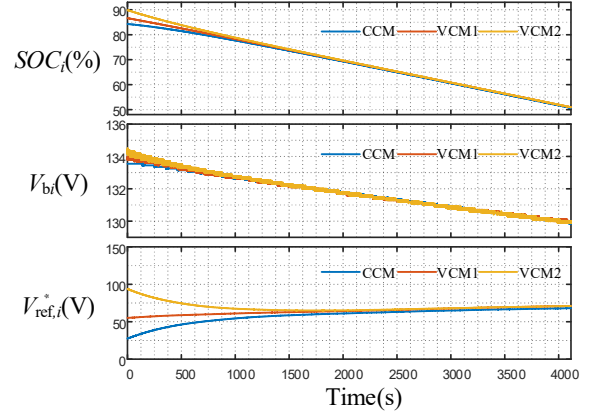
equation (5a)-(5c), VCM1 is aware of the unbalanced output power among modules earlier than VCM2. Therefore, VCM1 can regulate its output power faster than VCM2.

Next, we stepped the current reference amplitude I^* to validate the dynamic performance under the sparse communication network. The current tracking performance is similar to Fig. 12a and thus it is not shown here. The secondary control responses are shown in Fig. 13b. It can be found that power sharing among modules can be achieved in about 7 s after the step change. However, comparing with Fig. 12b, convergence time is slower under the sparse communication network.

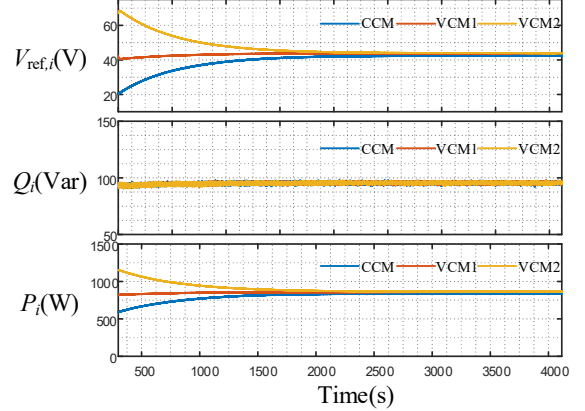
In conclusion, current tracking and power sharing among modules can be achieved with a full or sparse communication network. The communication channels can be reduced substantially if the number of modules is large.

C. Battery SOC Balancing Control Performance

The performance of the proposed battery SOC balancing control scheme is tested and evaluated during battery charging operation with $I^* = -20A$. The initial SOC values of the battery packs are intentionally made different by 8%. The SOC value of CCM is $SOC_1 = 43.3\%$, and SOC values of VCMs are $SOC_2 = 50.74\%$ and $SOC_3 = 51.94\%$, respectively. The experimental results are shown in Fig. 14. In the beginning, the SOC balancing controller can detect that the SOC value



(a) SOC V_{bi} measured in BMS, V_{ref}^* calculated by BBBs



(b) V_{ref} , Q , P calculated by DSPs

Fig. 15: Experimental results of battery SOC balancing during discharging operation with $I^* = 25A$

of CCM is lower than that of other modules. Therefore, the voltage ratio variable V_{ref}^* for CCM is larger than others, as shown in Fig. 14a. Also, $V_{ref,1}^*$ reaches the preset maximum value, i.e., $V_{ref,1}^* = 100$ to avoid overmodulation. As a result, k_{soc} can not be set to a large value. In our experiments, with $k_{soc} = 0.7$ as shown in Table II, battery SOC for the three modules can be balanced in about 4500 s. From Fig. 14b, the output voltage amplitude of CCM, $V_{ref,1}$, is larger than the output voltage amplitudes of other modules so that CCM can absorb more power and charge the battery pack of CCM at a faster rate until SOC balancing is achieved. With the proposed control, the SOC values of the three battery packs get closer to each other gradually. After SOC balance is achieved, the voltage ratio variables $V_{ref,i}^*$ for three modules are kept close to each other to maintain the balance. The intermediate variables, V_{ref}^* , V_{ref} and Q_i , also follow the trend of SOC, and gradually reach an agreement.

The performance of SOC balancing control is also tested during battery charging with $I^* = 25A$. The initial SOC values of the battery packs are intentionally made different by 5% with $SOC_1 = 84.2\%$, $SOC_2 = 86.5\%$ and $SOC_3 = 89.5\%$. The experimental results are shown in Fig. 15. In the beginning, the SOC value of CCM is lower than that of other modules. The SOC balancing controller set the voltage ratio variable, V_{ref}^* of CCM to be smaller than others, as shown

in Fig. 15a. On the contrary, the voltage ratio variable V_{ref} for VCM2 is larger than others due to its large initial SOC. In Fig. 15b, the output voltage amplitude of CCM, $V_{\text{ref},1}$ is smaller than the output voltage amplitudes of other modules so that CCM outputs less power and discharge the battery pack of CCM at a slower rate until SOC balancing is achieved. The experiment results validate that the desired SOC balancing is achieved and maintained during the discharging process.

VII. CONCLUSION

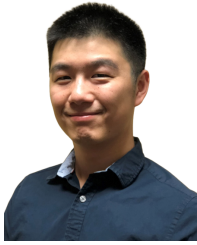
In this paper, we propose a hierarchical distributed control architecture for CHB converter, which consisting of three levels - primary control, secondary control and battery SOC balancing control. The primary control is in charge of ensuring output current tracking and maintaining the stability of the grid-connected operation of BESS. The secondary control based on consensus algorithm achieves power sharing regulation among modules and is proved to be stable. Battery SOC balancing is further realized based on the secondary control and dynamic average consensus algorithm in a distributed manner. Moreover, the proposed control strategies, along with the CPS control, are implemented in a CHB converter testbed and validated through experiment.

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