Analytic Device Model of Organic Field-Effect Transistors with Doped Channels

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Abstract

Doping has been shown to not only provide additional degrees of freedom in the design of organic field-effect transistors (OFETs), but to increase their performance and stability as well. An analytic model based on the assumption of a square doping profile inside the channel is presented here that describes the effect of doping on the transfer characteristic of OFETs. The model is validated experimentally by a series of OFETs with varying doping conditions. The precise doping profile in the transistor channel is determined by fitting the capacitance/voltage response of doped Metal-Insulator-Semiconductor junctions using a AC small signal drift-diffusion simulation. It is shown that the real doping profile deviates from the simplifying assumptions of the analytic model, i.e. it is found that the effective doping concentration at the dielectric/semiconductor interface is reduced. However, it is shown that the analytic model is not sensitive to this deviation as only the total density charges per unit area determine the changes in the transistor behavior. Overall, the presented theory provides new design rules that can be used to guide the development of doped OFETs with high performance.

Keywords

Organic Field-Effect Transistors; Doping; Stability; threshold voltage; pinch-off voltage; Small-Signal AC Model

1 Introduction

Organic field-effect transistors have experienced a significant improvement in performance during the last decade.[1–3] Although some of the reported record values for the charge carrier mobility might not be reliable,[1] charge carrier mobilities approach or - in case of p-type transistors - even exceed $10 cm^2 V^{-1} s^{-1}$. At this level, it was shown that the transit frequency of OFETs can be significantly increased, possibly into the GHz regime,[4] if contact resistances at the source and drain are minimized.[5,6]

Doping organic semiconductors[7–9] was shown to be essential for obtaining high mobility.[10] However, the benefits of doping are not limited to an increase in performance.[11–14] Doping was as well shown to precisely control the threshold voltage of OFETs;[7,8,12,15] to fill traps and stabilize OFETs;[16,17] and to define the majority and minority charge carrier type in OFETs.[18–20] Overall, doping is a key technology to realize the full potential of OFETs, to increase OFET stability, and to precisely tune their key parameters.

Doping the channel of OFETs has a profound influence on their electric characteristic. Not only does it shift the threshold voltage, but increases the pinch-off voltage as well, i.e. a larger voltage has to be applied to the gate to turn the transistor off. Balancing these two trends, i.e. reaching a sufficient shift in the threshold voltage without degrading the off-current is essential to obtain high performance doped OFETs. Recently, we were able to show that keeping the doped layer as thin as possible but keeping the total number of dopants per unit area constant approaches an optimum result.[15,16,18]

Despite the increasing importance of doping for high performance OFETs, an analytic device model describing doped OFETs is missing. Most reports on doped OFETs discuss the

influence of doping in terms of a shift in threshold voltage. It was experimentally found that this shift is proportional to the total number of free charges introduced into the channel by doping.[7,8,18,21,22] However, neither is the influence of doping on the pinch-off voltage included, nor is a thorough theoretical validation for the observed trends given.

Horowitz et al.[23] presented an analysis on the influence of residual bulk charges, e.g. caused by impurities in the organic semiconductor, and proposed a better physical interpretation of the threshold voltage. Here, an analytical model of doped OFETs is developed based on the result of Horowitz et al.[16,23] and the predictions of the model are thoroughly validated by systematic experiments. It is shown that the transistor operates in an intermediate state between accumulation (close to the source electrode) and depletion mode (close to the drain). In order to verify this result, the influence of doping on the threshold and pinch-off voltage in pentacene-based OFETs and metal insulator semiconductor (MIS) junctions is studied. The model is derived by the simplifying assumption of a homogeneous and abrupt doping profile inside the transistor channel. To test this assumption, the actual doping profile is determined with the help of a numerical drift-diffusion simulation,[24] which shows that the effective doping concentration is reduced at the insulator/semiconductor interface. However, it is shown that this decrease in doping concentration at the gate interface does not significantly affect the performance of the analytic model. Overall, the model presented here provides a framework to discuss and design highly performing doped OFETs.

2 Theory of Doped p-Type Organic Field-Effect Transistors

Doping introduces additional charges into the transistor channel that have to be accounted for. Assuming that the transistor channel extends from $x = 0$ to $x = L$, with L: the channel length (cf. Figure 1) and that $V(x) - (V_{GS} - V_{FB}) > 0$, one finds the following density of

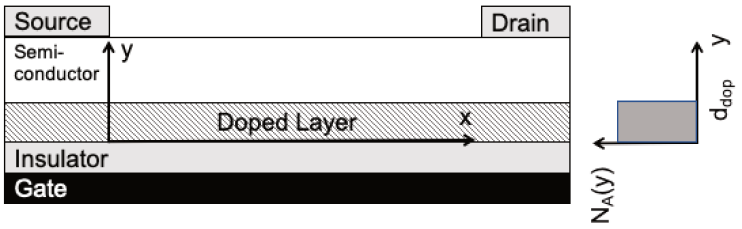


Figure 1: Geometry of doped organic transistors assumed in the model.

free holes[16]

$$p(x,y) = \frac{1}{e} C_i \left[V(x) - (V_{GS} - V_{FB}) \right] \delta(y) + N_A(y). \tag{1}$$

In Equation 1, the y axis is perpendicular to the transistor channel, e is the elementary charge, $C_i = \frac{\epsilon_i}{d_i}$ is the specific gate capacitance (ϵ_i: permittivity of gate insulator, d_i: thickness of gate insulator), $V(x)$ is the electric potential along the transistor channel, V_{GS} is the gate voltage, V_{FB} is the flatband voltage of the gate capacitance, $\delta(y)$ is the Dirac delta function, and $N_A(y)$ is the doping profile, which is assumed to be uniform along the x-direction.

The doping profile $N_A(y)$ can be complex and will be determined in more detail in Section 3.2. In order to derive an analytic solution, a rectangular doping profile can be assumed (cf. Figure 1)

$$N_A(y) = \begin{cases} N_A, & \text{for } 0 \leq y \leq d_{dop} \\ 0, & \text{for } y > d_{dop} \end{cases} \tag{2}$$

where d_{dop} is the thickness of the doped layer.

The drain current I_D is obtained from Ohm's law $I_D = -ew \int_0^\infty p(x,y) \mu_p E_x(x) dy$ ($E_x = -\frac{dV}{dx}$: electric field along the x-axis, w: width of the transistor).

In the linear regime, i.e. for $V_{DS} > V_{GS} - V_{FB}$ (V_{DS}: drain potential) holes are accumulated along the whole transistor channel and the doped layer is not depleted (cf. Figure 2a).

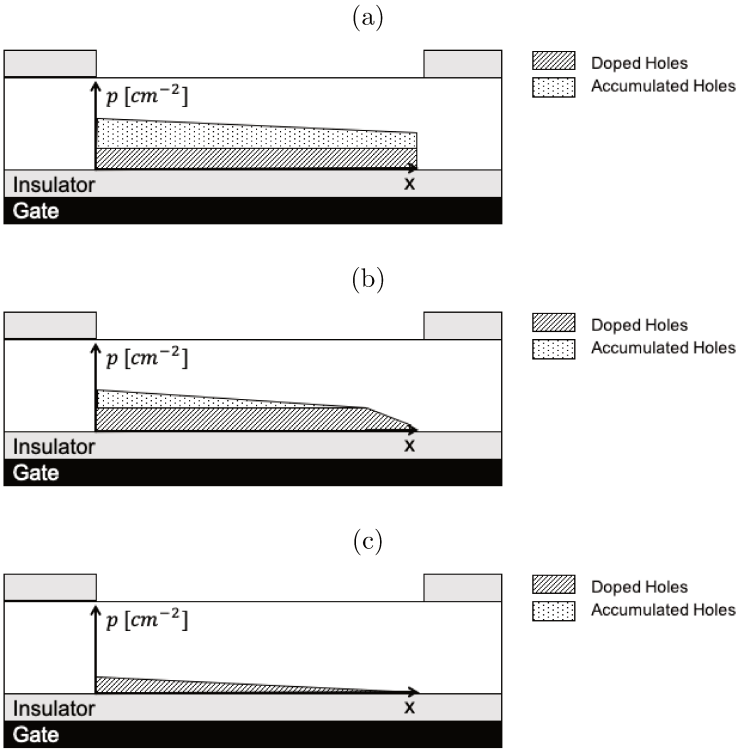


Figure 2: Sketch of the hole concentration $p(x) = \int_0^\infty p(x, y)dy$ inside the transistor channel in the (a) linear regime ($V_{DS} > V_{GS} - V_{FB}$); (b) saturation regime ($V_{DS} < V_{GS} - V_{FB}$); and (c) depletion regime ($V_{GS} > V_{FB}$). Holes due to doping are represented by the hatched area, whereas accumulated holes are shown by the dotted area.

One obtains

$$\int_0^L I_D dx = \mu_p w C_i \int_0^{V_{DS}} \left\{ [V(x) - (V_{GS} - V_{FB})] + \frac{d_{dop} e N_A}{C_i} \right\} dV, \tag{3}$$

which leads to the well-known equation

$$I_D = \frac{\mu_p w C_i}{L} \left\{ \frac{V_{DS}^2}{2} - (V_{GS} - V_{th}) V_{DS} \right\} \tag{4}$$

Equation 4 resembles the characteristic of intrinsic transistors, but with a modified threshold voltage of

$$V_{th} = V_{FB} + \frac{e d_{dop} N_A}{C_i}. \tag{5}$$

As seen in Equation 5, the threshold voltage equals the flatband voltage of the gate capacitance, but with an additional term added that accounts for the additional charge $N_A d_{dop}$ introduced into the channel by doping.

For larger voltages, i.e. for $V_{DS} < V_{GS} - V_{FB}$, the difference between the gate potential and the potential at the drain electrode $V_{GS} - V(x = L)$ becomes large enough to deplete the doped layer, i.e. to remove free charges introduced by the doping profile defined by Equation 2. For increasing drain voltages, this depletion not only grows toward the source electrode, but the thickness of the depletion layer d_{dep} increases as well. At the pinch-off point, the doped channel is completely depleted at the drain, i.e. $d_{dep} = d_{dop}|_{x=L}$, and the drain current saturates (cf. Figure 2b).

To account for this behavior, Equation 3 has to be appended by a second term describing transport through the depleted doped layer[23]

$$I_D = \frac{\mu_p w C_i}{L} \int_0^{V_{GS}-V_{FB}} [V(x) - (V_{GS} - V_{th})]\, dV + \frac{\mu_p w e N_A}{L} \int_{V_{GS}-V_{FB}}^{V_{DS}} (d_{dop} - d_{dep}(V))\, dV \tag{6}$$

Assuming an abrupt junction, i.e. an infinitely sharp boundary between the depleted and

the non-depleted part of the doped layer, one finds for the thickness of the depletion layer[25]

$$d_{dep}(V) = \frac{\epsilon_s}{C_i}\left\{\sqrt{1+\frac{2C_i^2(V_{GS}-V(x)-V_{FB})}{eN_A\epsilon_s}}-1\right\}, \tag{7}$$

where ϵ_s is the permittivity of the semiconductor.

Using this equation, one can re-write the second integral of Equation 6 as an integral over the depletion layer thickness d_{dep}. Furthermore, assuming that the transistor is in the saturation regime, one obtains

$$\begin{aligned} I_{D,sat} &= \frac{\mu_p w}{L} C_i \int_0^{V_{GS}-V_{FB}} \left[V(x)-(V_{GS}-V_{th})\right] dV & (8)\\ &+ \frac{\mu_p w}{L} eN_A \int_0^{d_{dop}} (d_{dop}-d_{dep})\left\{-\frac{eN_A}{\epsilon_s}\left[d_{dep}+\frac{\epsilon_s}{C_i}\right]\right\} d(d_{dep}) & (9)\end{aligned}$$

Solving this equation leads to the characteristic of a doped OFET in the saturation regime

$$-I_{D,sat} = \frac{\mu w}{2L} C_i \left\{(V_{GS}-V_{th})^2 + \frac{2}{3}\frac{d_{dop}eN_A}{C_i}(V_{PO}-V_{th})\right\} \tag{10}$$

Here, the pinch-off voltage V_{PO} is defined as the voltage that has to be applied to the drain to completely remove all doped charge carriers from the channel and to switch the transistor off. One obtains for V_{PO} from Equation 7 by setting $d_{dep} = d_{dop}|_{x=0}$ and considering that $V(0) = 0$

$$\begin{aligned} V_{PO} &= \frac{eN_A d_{dop}^2}{2\epsilon_s}\left[1+2\frac{C_s}{C_i}\right] + V_{FB} & (11)\\ &= V_{th} + \frac{d_{dop}^2 eN_A}{2\epsilon_s}, & (12)\end{aligned}$$

where $C_s = \frac{\epsilon_s}{d_{dop}}$.

Equation 10 shows that doped OFETs operate in between the accumulation and depletion regime. Whereas free charges are accumulated close to the source, the doped layer is depleted close to the drain. For increasing gate voltages, the depletion region of the device grows,

until the transistor finally switches off.

Consequently, the drain current consists of two components. The first term in Equation 10 resembles the IV characteristic of intrinsic transistors, i.e. it is due to accumulation of free holes at the gate/semiconductor interface. The second component is given by the second term in Equation 10, which is caused by conduction through the doped layer. Furthermore, the shift of the threshold voltage with the doping concentration as described by Equation 5 is identical for the linear and saturation regime.

Finally, for $V_{GS} > V_{FB}$, no charge carriers are accumulated in the transistor channel and the doped layer is depleted along the whole channel length (cf. Figure 2c). The saturation current becomes

$$I_{D,sat} = -\frac{\mu_p w e^2 N_A^2}{L\epsilon_s} \int_{d_{dep}(0)}^{d_{dop}} (d_{dop} - d_{dep}) \left\{ d_{dep} + \frac{\epsilon_s}{C_i} \right\} d(d_{dep}) \tag{13}$$

$$= \frac{\mu_p w e^2 N_A^2}{L\epsilon_s} \left[\frac{C_s}{C_i} d_{dop}^2 d_{dep}(0) - \frac{1}{2} \left(\frac{C_s}{C_i} - 1 \right) d_{dop} d_{dep}^2(0) - \frac{1}{3} d_{dep}^3(0) - \frac{d_{dop}^3}{6} \left(1 + \frac{3C_s}{C_i} \right) \right] \tag{14}$$

where $d_{dep}(0)$ is the thickness of the depletion layer at the source, given by Equation 7 at $x = 0$. As can be easily verified, Equation 13 results in $I_{D,sat} = 0$ for $d_{dep}(0) = d_{dop}$, i.e. the transistor is switched off once the doped layer is fully depleted along the whole channel.

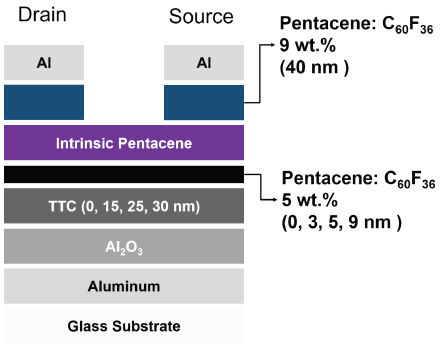


Figure 3: Schematic structure of doped OFETs with varying thickness of the doped channel. The doped channel consisting of p-doped Pentacene (5 $wt.\%$ Pentacene:$C_{60}F_{36}$) is inserted between the passivation layer (TTC) and a layer of intrinsic Pentacene.

3 Experimental Verification of the Model

To verify this model, doped staggered, bottom gate OFETs as shown in Figure 3 are discussed in the following. However, the model assumptions are independent of the particular geometry of the OFET and should be applicable for other designs. The devices consist of an Al_2O_3 gate dielectric ($104nm$), covered by a thin layer of tetratetracontane (TTC) as passivation layer. Adding a TTC layer is known to yield highly stable organic transistors[26] and to enable ambipolar conduction in a variety of organic semiconductors.[27]

On top of the TTC layer, a thin film of a doped organic semiconductor is deposited by co-evaporation of Pentacene and $C_{60}F_{36}$.[28] $C_{60}F_{36}$ is a comparably large molecular dopant, which shows a large morphological stability at room temperature compared to smaller dopants such as F_4TCNQ.[29] This layer is followed by an intrinsic Pentacene layer (45 nm), and a doped contact layer of 9 $wt.\%$ of Pentacene:$C_{60}F_{36}$ (40 nm) structured by a drain/source shadow mask to optimize injection at the drain and source. Finally, 60 nm of Aluminum are deposited on top to ensure a high lateral conductivity of the electrodes.

Process details are given in the experimental information section. The stability of undoped devices and the influence of the TTC layer on the transfer characteristic is discussed in the supplementary information.

3.1 Influence of Doping on the Threshold and Pinch-Off Voltage of OFETs

According to Equation 5, the increase in free charge carriers in the transistor channel due to doping is expected to shift the threshold voltage of OFETs. Assuming that the flatband voltage V_{FB} is only weakly influenced by the doped layer, the shift in threshold voltage $\Delta V_{th} = \frac{ed_{dop}N_A}{C_i}$ will be directly proportional to the thickness of the doped layer d_{dop}.

Indeed, as shown in Figure 4 (a), there is a clear shift in the on-set voltage towards positive gate-source voltages. Furthermore, the ambipolar characteristic of intrinsic transistors (d_{dop}

$= 0\ nm$) returns to an unipolar one upon doping.

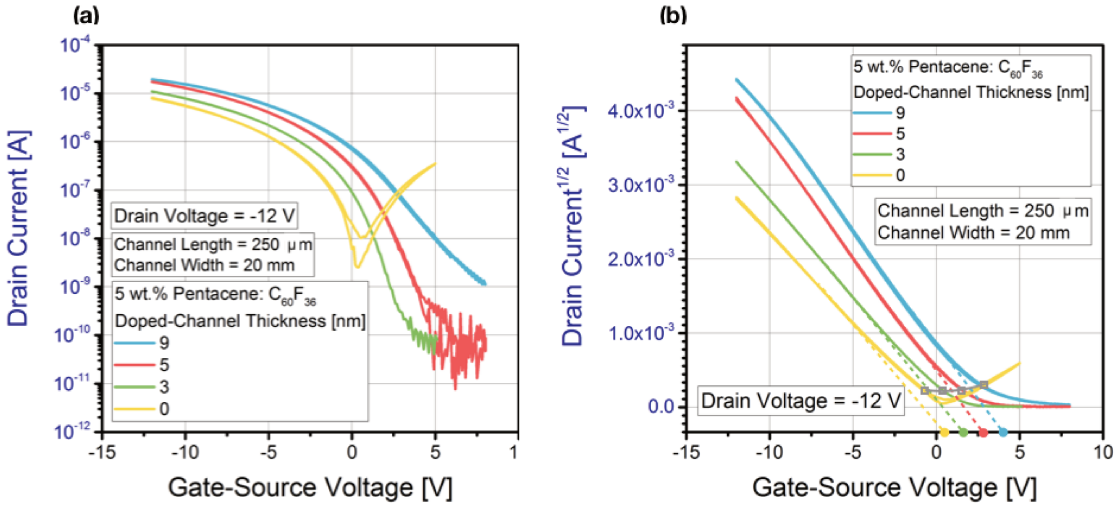


Figure 4: Transfer characteristics of Pentacene-based OFETs with increasing thickness of the doped channel. (a) Doping the channel of p-type OFETs leads to an shift in the on-set voltage. (b) shows the plot of $I_D^{\frac{1}{2}}$ vs. V_{GS}. The threshold voltage V_{th} is extracted by the intercept of a linear fit of $I_D^{\frac{1}{2}}$ with the V_{GS} axis.

The threshold voltage V_{th} is extracted from the $I_D^{\frac{1}{2}}$ vs V_{GS} plot shown in Figure 4 (b) and plotted in Figure 5 (a). Each threshold voltage is calculated from 9 devices and the error bar represents the corresponding standard deviation. The threshold voltage shifts from 3.13 $\pm$ 0.27 V to -0.15 $\pm$ 0.36 V by increasing the thickness of doped channel from 0 nm to 9 nm. The standard deviation is in the range of 0.3 V for each doped channel thickness, which shows a limited spread in device parameters.

The threshold voltage shows a linear dependence on the thickness of the doped channel. The linear fit (solid line) in Figure 5 (a) has an Adj. R-Square value of 0.996 indicating a good linear relation between the threshold voltage and the thickness of doped-channel. Using Equation 5, the free charge carrier density can be deduced from the slope of the linear fit, which results in $N_A = 9.6 \times 10^{17}\, cm^{-3}$. This density of free charge carrier can be divided by the total number of dopant molecules introduced by co-evaporation, resulting in a doping efficiency $\eta_{dop} \approx 3.5\%$, which is close to literature values reported for this matrix/dopant

combination at these rather large doping concentrations.[17,30]

Figure 5 (b) shows the average hole mobility, calculated from the saturation current using Equation 10, vs. the thickness of the doped channel. The charge mobility increases slightly from 0.077 ± 0.024 cm^2/Vs (intrinsic transistor) to 0.140 ± 0.033 cm^2/Vs (5 nm doped channel). When the thickness of the doped-channel increases to 9 nm, the charge mobility remains at the same plateau with 5 nm.

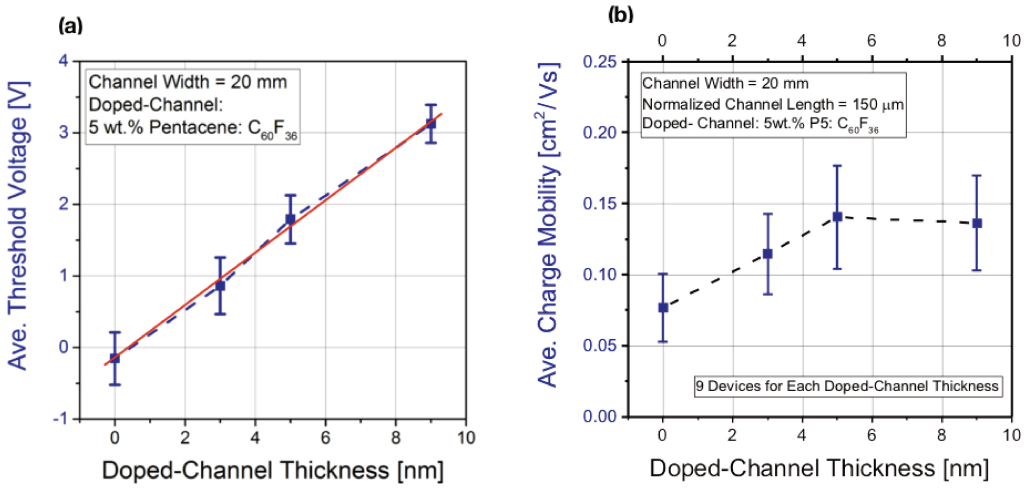


Figure 5: Threshold voltage and charge mobility of Pentacene-based OFETs with different thickness of the doped channel. (a) Threshold voltage vs. doped channel thickness extracted from Figure 4. (b) Charge mobility vs. doped channel thickness extracted from Figure 4 (b). Here, each data point consists of the results from 9 devices; the error bars represent the standard deviation of the measurement.

As shown in Section 2, the transistor is not completely off at the threshold voltage, but a residual drain current is carried by the free charge carriers inside the doped channel. Starting at Equation 10, the current at the threshold voltage becomes:

$$-I_{D,sat}(V_{GS} = V_{th}) = \frac{\mu w d_{dop} e N_A}{3L}(V_{PO} - V_{th}) \tag{15}$$

i.e., the drain current at the threshold voltage ($V_{GS} = V_{th}$) is expected to increase with the doped layer thickness. The current at the threshold voltage is marked by gray boxes in Figure 4(b), and indeed a small increase is observed. However, in particular the current

at the threshold voltage for the intrinsic transistor is artificially increased by the ambipolar characteristic of these transistors (see e.g. Figure 4(b)), i.e. significant electron currents at the threshold voltage, overall limiting the trends see in Figure 4(b).

To switch the transistor off, additional voltage has to be applied to the gate to completely deplete the channel of holes. According to Equation 11, this additional voltage, the pinch-off voltage V_{PO}, increases with the doped layer thickness d_{dop} as well. Figure 6 (a) shows a zoom

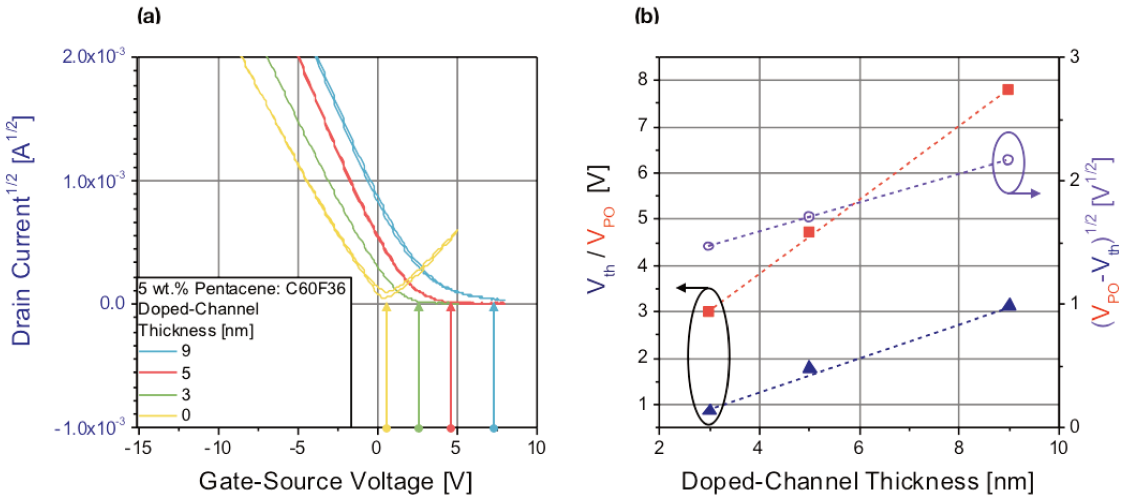


Figure 6: (a) Extraction of the pinch-off voltage (V_{PO}). (b) Comparison of threshold voltage V_{th} and pinch-off voltage V_{PO} (solid symbols with dashed line) and the plot of $(V_{PO} - V_{th})^{1/2}$ (open symbol).

of the transfer characteristic to focus on the transition from on-state to off-state. In Figure 6 (a), the pinch-off voltage V_{PO} is marked by arrows.

In Figure 6 (b), the threshold voltage V_{th} and the pinch-off voltage V_{PO} as deduced from Figure 6 (a) are plotted vs. the doped channel thickness by closed symbols. According to Equation 11, the difference between V_{PO} and V_{th} becomes:

$$(V_{PO} - V_{th})^{1/2} = \left(\frac{eN_A}{2\epsilon_s}\right)^{1/2} d_{dop}, \tag{16}$$

i.e. $(V_{PO} - V_{th})^{1/2}$ is linearly dependent on d_{dop}. Indeed, as seen in Figure 6 (b), right axis, the square root of the difference in the pinch-off an threshold voltage seems to scale with the

doped channel thickness.

3.2 Testing the Assumptions for the Analytic Model: Determining the Doping Profile

The analytical model described in Section 2 and the experimental analysis above relies on the assumption of a square doping profile described by Equation 2. To test this approximation, and to determine a more realistic doping profile, metal-insulator-semiconductor junctions are discussed in the following. By a joint experimental and modeling approach, it is shown that the capacitance/voltage characteristic of these junctions can be used to determine the doping profile $N_A(y)$ and leads to a comprehensive understanding of doped OFETs.

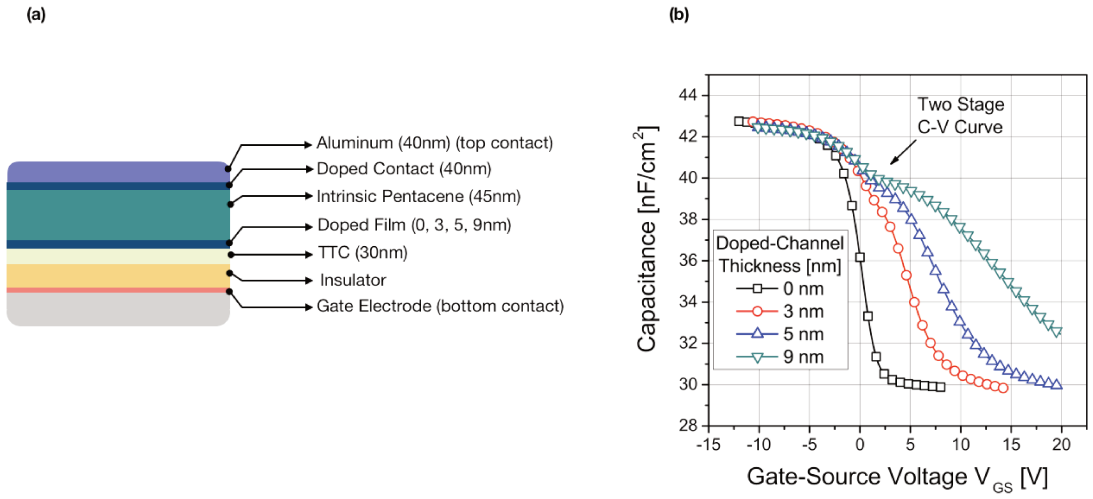


Figure 7: (a) Schematic of MIS junctions studied here. The structure is identical to the material stack of doped OFETs. (b) Capacitance-voltage (C-V) measurement of MIS junction with varying thickness of the doped layer. A two-stage curve is observed when doped layer is introduced.

Pentacene based MIS structures with different thickness of the doped channel are investigated. The structure is shown in Figure 7 (a), which is identical to the stack used for the study of doped Pentacene-based OFETs above.

Figure 7 (b) plots the C-V curve of MIS junctions with increasing thickness of the doped film. At negative voltages, holes are accumulated at the dielectric/pentacene interface, i.e.

the capacitor is in the accumulation regime. At positive voltages, however, the doped layer at the interface is depleted, the capacitance drops, and the junction is in the depletion regime.

Indeed, the maximum capacitance (42.8 nF/cm^2) at negative voltages is close to the capacitance of the insulator C_i as a large amount of charge carriers are accumulated at the surface of insulator (accumulation region). Therefore, in this accumulation regime, MIS junctions with different thickness of doped film show a similar capacitance.

However, different trends are observed in the depletion region. For MIS diodes without doped film, the C-V curve starts from the plateau of maximum capacitance (42.8 nF/cm^2) in the accumulation regime, and drops rapidly at around -5 V into its depletion regime. The device is fully depleted at around 5 V. For MIS junctions with doped films, the C-V curves show two distinct stages of depletion indicating different depletion modes.

3.2.1 Origin of the Reduction in Doping Concentration at the Dielectric Interface - Interface Roughness

To understand the shape of the C-V characteristics, the morphology of TTC films covering the Al_2O_3 oxide layer is studied. Figure 8 shows the top morphology of TTC (30 nm) as measured by Atomic Force Microscopy (AFM). The surface is characterized by small grains and an overall roughness of 1.5 nm root mean square (RMS) is observed, which indicates a rough surface.

Depositing the doped Pentacene layer on top of this rough interface, a blend layer of TTC and Pentacene is formed at the interface. This blend layer is expected to have a lower doping concentration and permittivity than a pure doped pentacene film. To study the influence of such a blend layer on the C-V characteristic, a small-signal device model based on a drift-diffusion model described in[24] was implemented.

The layer stack including a mixed blend layer at the TTC/pentacene interface is shown in Figure 8. To determine the AC response of these junctions, the potential $\phi(x)$ and hole concentration $p(x)$ inside the device are described by a superposition of a DC and a small-

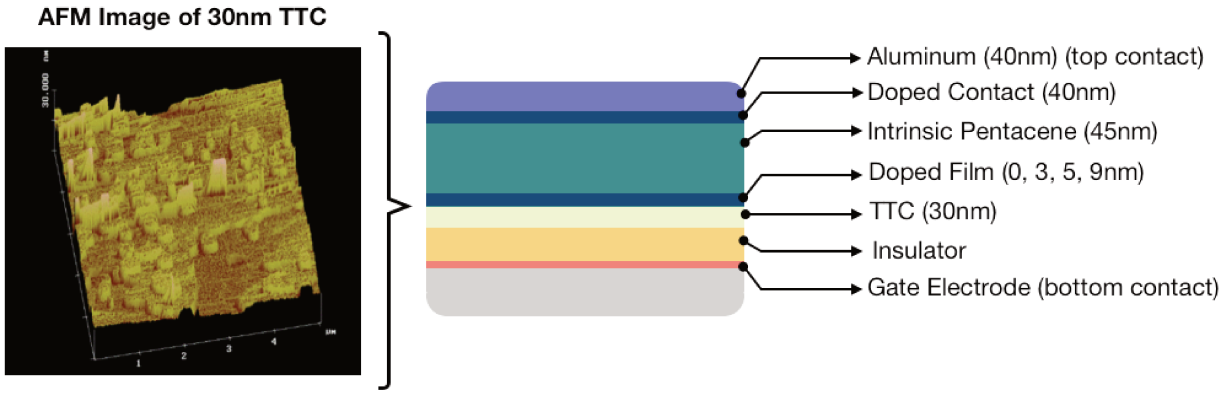


Figure 8: Introduction of a blend layer at the interface between TTC and the doped film. The left figure shows the top morphology of TTC by AFM, which is rough. Therefore, when the doped film is deposited on top of TTC, a blend layer of TTC and doped film is formed.

signal AC component[31,32]

$$\phi(x) = \phi^{DC}(x) + \underline{\phi}^{AC}(x)\exp(i\omega t) \tag{17}$$

$$p(x) = p^{DC}(x) + \underline{p}^{AC}(x)\exp(i\omega t) \tag{18}$$

where ϕ^{DC} and p^{DC} are the DC solutions for the potential and electron concentration, $\underline{\phi}^{AC}$ and $\underline{p}^{AC}$ are the complex AC amplitudes of the potential and the electron concentration, ω is the frequency of the AC component, and t is the time.

The system is described by Poisson's equation and the continuity equation for holes, which leads to the following system of equations

$$F(p,\phi) = \begin{pmatrix} \frac{d}{dx}\left(\epsilon\frac{d}{dx}\phi\right) - e(N_A - p) \\ \frac{d}{dx}\left(-ep\mu\frac{d\phi}{dx} - eD\frac{dp}{dx}\right) + e\frac{dp}{dt} \end{pmatrix} = 0, \tag{19}$$

with ϵ: dielectric constant, and D: diffusion constant.

Assuming that the AC component of the applied voltage is small compared to the DC one, the system can be linearized. Combining the hole concentration and potential in a

single vector $z = (\phi, p)$, one obtains[33]

$$F = F(z^{DC}) + J(z^{DC})\underline{z}^{AC}\exp(i\omega t) = 0, \tag{20}$$

where J is the Jacobian matrix with $J_{ij} = \frac{dF_i}{dz_j}$, z^{DC} and $\underline{z}^{AC}$ are the DC and AC solutions of the system, respectively.

The DC solution of the system z^{DC} can be calculated by a standard drift-diffusion algorithm based on the Gummel or Newton algorithm by setting $\frac{dp}{dt} = 0$. Once the DC solution is found, the Jacobian of the system J is calculated at the DC operation point (setting $\frac{d\underline{p}^{AC}}{dt} = i\omega\underline{p}^{AC}$), which allows to calculate the AC components of the potential and the hole concentration.

From $\underline{\phi}^{AC}$ and $\underline{n}^{AC}$, the AC component of the current $\underline{j}^{AC}$ is found by linearizing $j = -ep\mu\frac{d\phi}{dx} - eD\frac{dp}{dx}$. One obtains for the hole current at the i-th discretization site

$$\begin{aligned} j_p &= j^{DC} + \underline{j}_p^{AC}\exp(i\omega t) && (21)\\ \underline{j}_i^{AC} &= \frac{dj}{dp_i}\underline{p}_i^{AC} + \frac{dj}{dp_{i-1}}\underline{p}_{i-1}^{AC} + \frac{dj}{d\phi_i}\underline{\phi}_i^{AC} + \frac{dj}{d\phi_{i-1}}\underline{\phi}_{i-1}^{AC}, && (22)\end{aligned}$$

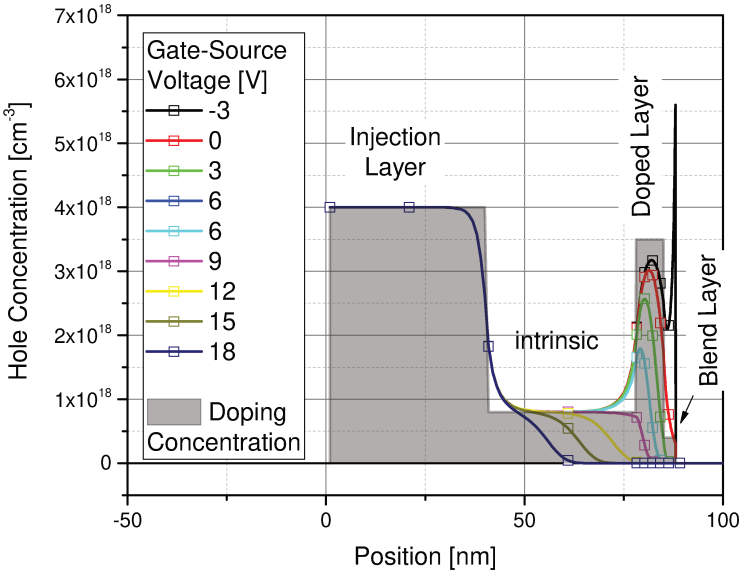
where all derivatives $\frac{dj}{dz}$ are taken at the DC operation point ϕ^{DC}, p^{DC}.

Finally, the total current inside the device $\underline{j}^{AC}$ at frequency ω is given by the sum of the displacement current $j_{disp} = \epsilon\frac{d\underline{E}^{AC}}{dt}$ and $\underline{j}_p^{AC}$. The complex impedance $\underline{Z}(\omega)$ and the capacitance C of the device can then be calculated by the AC component of the applied voltage $\underline{V}^{AC}$ and $\underline{j}^{AC}$, which, according to the continuity equation, is constant across the device

$$\begin{aligned} \underline{Z} &= \frac{\underline{V}^{AC}}{\underline{j}^{AC}} && (23)\\ C &= \frac{1}{\Im(Z)\omega}. && (24)\end{aligned}$$

The DC result $p^{DC}(x)$ of the device with a 9 nm thick doped film at varying voltages is

(a)



(b)

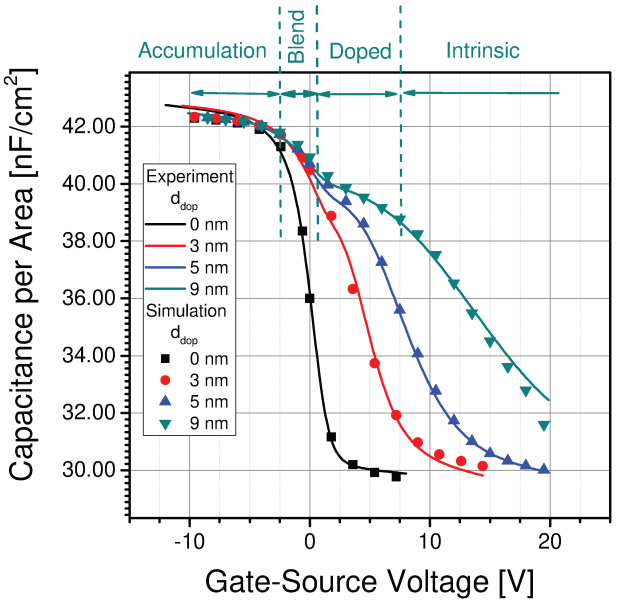


Figure 9: (a) DC Charge carrier density $p^{DC}(x)$ throughout the MIS junction at different gate-source voltages V_{GS} . With increasing gate-source voltage V_{GS}, the depletion zone starts to grow at the interface of insulator (Oxide/ TTC) and doped film, and continues to expand into the intrinsic layer. The doping concentration is included as grey area. (b) Comparison of experimental C-V data vs. C-V data as obtained from the small-signal AC simulation. Parameters used in the calculation are summarized in Table 1.

shown in Figure 9 (a). The simulation parameters are summarized in Table 1.

As shown in Figure 9 (a), in the accumulation regime ($V_{GS} = -3V$), charge carriers are accumulated at the interface between insulator (i.e. Oxide/TTC) and the doped film. Therefore, the capacitance of the junction is represented by the capacitance of the insulator (i.e. $C_{total} = C_{ins}$). With increasing V_{GS}, the holes are increasingly depleted and the depletion zone grows. For higher positive gate-source voltages, the depletion zone expands into the intrinsic layer. With a high gate-source voltage ($V_{GS} = 18\,V$), the charge carrier density inside intrinsic layer is almost fully depleted.

A fit of the MIS C-V curves for different thickness of the doped layer is presented in Figure 9 (b). The symbols represent the simulation data, while the lines plot the experimental data. With the knowledge of the charge carrier density distribution at varying V_{GS} from Figure 9 (a), the features of the experimental C-V curve can be assigned to particular layers of the MIS junction. Figure 9 (b) includes the different layers for the MIS junction with a doped layer thickness of 9 nm. Indeed, the two stages in the depletion region can be assigned to the depletion of the blend layer first, followed by the depletion of the doped layer.

Table 1: Parameter used in the numerical simulation. If the parameter was varied between samples with different thickness of the doped layer, the parameters are listed in the order of the thickness of the doped layer, starting with the undoped device.

Material	$\epsilon[\epsilon_0]$	Thickness $[nm]$	N_A $[10^{17}cm^{-3}]$
Al_2O_3	7.81	98	N/A
TTC	3.1	25	0
Blend Layer	3.1	$0; 3; 3; 3$	$0; 5; 1; 4$
Doped Layer	5.8[30]	$0; 2.5; 4.4; 7$	$0; 20; 30; 35$
Intrinsic Layer	5.8[30]	$48; 39; 38; 38$	$1; 3.5; 5; 8$
Injection Layer	5.8[30]	40	$60; 40; 40; 40$

The results of the AC model show that the doping profile is more complex than assumed for the analytic model (Equation 2). However, the average doping concentration from the blend and the doped layer as determined from the fit ($\overline{N_A} = 1.2, 1.8, 2.6 \cdot 10^{18}cm^{-3}$ for the 3,5, and 9 nm thick film, respectively) is very close to the doping concentration calculated from the shift of the threshold voltage observed in Figure 5 ($N_A = 9.6 \cdot 10^{17}cm^{-3}$). In fact,

the shift in threshold voltage is only proportional to the total density of free charges per unit area $N_A d_{dop}$, i.e. in first approximation the theory presented in Section 2 will not be heavily influenced by the deviation of the actual doping profile from the idealized profile described by Equation 2.

The background doping concentration in the nominal intrinsic layer is rather large (see Table 1). This large background doping concentration could be explained by a small diffusion of the dopant $C_{60}F_{36}$ into the intrinsic layer. Alternatively, it could be caused by the significant roughness of the pentacene layer, i.e. the effective doping layer in the intrinsic layer is caused by an intermixing of the doped layers (in particular the doped injection layer) and the undoped layer.

3.2.2 Origin of the Reduction in Doping Concentration at the Dielectric Interface - Interface Traps

In the previous section, the reduction in the effective doping concentration at the semiconductor/gate interface was explained by a blend layer at the TTC/Pentacene interface. However, other explanations for the reduction are possible - in particular a layer of traps at the interface between TTC and doped layer would have a similar effect. Doping is known to fill trap states and to shift the Fermi-Level inside the doped layer away from the trap energy,[17,34,35] which reduces the effective doping concentration N_A^{eff} by the density of traps N_{trap}, i.e. $N_A^{eff} = N_A - N_{trap}$.[24]

In the following, the response of doped transistors to extended gate bias stress is used to localize traps and to show that despite the TTC passivation layer traps are present at the dielectric interface. OFETs are known to be susceptible to gate-bias stress, i.e. the threshold voltage V_{th} of OFETs shifts when a constant gate bias is applied.[35–38] This shift is assumed to be caused by filling of trap states at the interface of dielectric gate and semiconductor or by filling trap states inside the bulk of the organic semiconductor. The high control over the doped layer thickness shown here will allow to localize the origin of traps responsible for

gate bias stress, and to distinguish between trapping at the dielectric interface or the bulk of the organic semiconductor.[37]

To study the influence of doping on gate bias stress, threshold voltages are extracted from transistors with different thickness of doped channel following the protocol of Klauk et al.[38] The gate-source voltage is kept constant at $V_{GS} = -12\,V$, while the drain-source voltage is kept at $V_{DS} = 0\,V$ to maximise stress within the operation range of the OFET. To measure the shift in V_{th}, the transfer characteristics of the OFETs is measured at $V_{DS} = -12\,V$, and gate-source voltage V_{GS} is swept from $-12\,V$ to $8\,V$.

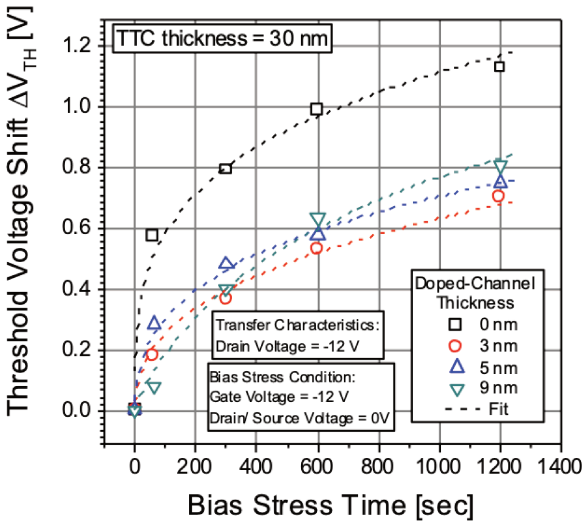


Figure 10: Threshold voltage shift vs. gate bias stress time: Solid symbols represent experimental data. Devices with a doped channel have a smaller threshold voltage shift compared to the devices without doping, which indicates that a transistor can be stabilized by inserting a thin doped layer between the dielectric gate and intrinsic organic semiconductor layer. Dashed lines are fits of experimental data with a stretched exponential function to quantify the lifetime improvement of OFETs for different thickness of doped-channel.

Figure 10 shows the threshold voltage shift vs. the gate-source bias stress time (solid symbols). For OFETs without doped layer, the threshold voltage shifts 1 V from -0.5 V to -1.5 V. For OFETs with a doped channel, the threshold voltage shift smaller, and ranges from 0.6 to 0.7 V.

The time-depended threshold voltage shift under a constant bias stress can be described

by a stretched exponential function:[38]

$$V_{TH}(t) = (V_{th,t\to\infty} - V_{th,t=0})(1 - e^{-(\frac{t}{\tau})^{\beta}}), \tag{25}$$

where the $V_{th,t=0}$ is the threshold voltage of the fresh device, $V_{th,t\to\infty}$ denotes the threshold voltage after equilibrium, i.e. for $t \to \infty$, τ is the time constant of the of the stress mechanism, and β is the stretching parameter. Equation 25 is an empirical function, which was firstly introduced by Kohlrausch et al.[39] The quality of the fit can be improved by the stretching parameter β. β ranges from 0 to 1 and describes dispersion in the trapping process, i.e. a variation in time constants τ of the process. The closer β approaches 1, the narrower the distribution of time constants. The time constant τ represents the time expected to reach 63% of the equilibrium voltage shift. However, the stretching leads to a slower-than-exponential response for times beyond $t = \tau$. Hence, the time t to reach 90%, 95% or 99% of the equilibrium value increases. Table 2 shows the parameters used to fit the threshold voltage shift shown in Figure 10 as dashed line. The $V_{th,t\to\infty}$ reduces from 9.95 V to 1.19 V by increasing the thickness of the doped channel from 0 nm to 9 nm.

Table 2: Table of parameters used to fit experimental results of gate bias stress by Equation 25.

d_{dop} $[nm]$	β	τ $[sec]$	$V_{th,t\to\infty}$ $[V]$
0	0.29	1.59×10^6	9.95
3	0.40	4.93×10^5	7.98
5	0.42	7.20×10^3	1.99
9	0.77	0.96×10^3	1.19

Figure 10 shows that gate bias stress effects are reduced by doping. However, the improvement in stability is strongest from intrinsic transistors to transistors with the thinnest doped layer, and no additional improvement is observed when the doped layer thickness is increased further. This indicates that doping improves the stability of OFETs predominantly by filling traps at the interface to the gate dielectric instead of in the bulk.

The difference in threshold voltage shift between the doped and intrinsic OFETs can be

used to estimate the density of traps present at the dielectric interface. Using an approximate difference of $\Delta V = 0.3V$, and using the capacitance of the gate stack ($C_i = 42.8nFcm^{-2}$), one arrives at a trap density per unit area $N_t^{\square} \approx 8 \cdot 10^{10} cm^{-2}$, which is slightly lower than the reduction in doping concentration in the blend layer per unit area used in the AC-model (approx. $3 - 5 \cdot 10^{11} cm^{-2}$, Table 1). Therefore, trap states at the dielectric interface are expected to contribute to the reduction in effective doping concentration at the dielectric interface, but the effect of traps alone seems to be too small to explain the full reduction in effective doping concentration. Most likely, a combination of trapping and reduction in doping concentration due to interface roughness contributes to the full reduction in effective doping concentration at the dielectric/semiconductor interface.

4 Conclusion

Doping organic transistors is a powerful method to increase the performance and electrical stability of organic field-effect transistors. Doping the transistor channel influences its electrical behavior in complex ways. Here, an analytic model is presented that can be used to discuss doped OFETs in the saturation regime and to design doped OFETs. The predicted trends in the threshold and pinch-off voltage are verified with the help of a series of transistors with increasing thickness of the doped layer.

The model is based in the assumption of a square doping profile in the transistor channel. This assumption is tested with the help of a series of doped MIS junctions. It is shown that the effective doping profile is reduced at the dielectric/semiconductor interface, which leads to a distinct two-stage capacitance curve in the depletion region. The reduced doping concentration can be explained by either a mixed layer of TTC (used as passivation layer on top of the gate oxide) and the organic semiconductor, interfacial traps at the same interface, or a mixture of these two. However, it is shown that the analytic model is not sensitive to these variations, but that the total density of charges per unit area determines the changes

in the transistor characteristic.

Overall, the presented model provides an analytical solution that can be used to discuss the transfer characteristic of doped OFETs and to deduce important device parameters such as the effective doping concentration. However, the model goes beyond providing a framework to discuss OFET results, and can as well be used to design doped OFETs that balance the need to minimize gate bias stress, to lower the threshold voltage, and to obtain a large sub-threshold swing not negatively affected by an increase in the pinch-off voltage.

5 Experiments and Methods

OFETs are assembled on cleaned glass substrates, which are cleaned by sequential ultrasonication in D.I. water, Acetone, Methanol and Isopropanol. An aluminum film (200 nm) is deposited by thermal evaporation onto the glass substrate and structured to form the gate patterns via shadow masks. Afterwards, an aluminum oxide layer of 104 nm is grown by anodization[15,40] to form the dielectric gate. The thickness of the thin aluminum oxide is controlled by the terminating anodization voltage,[40] which is set to 80 V(oxide growth rate is 1.3 nm/V). A passivation layer of TTC is deposited onto the oxide. Afterwards, substrates are annealed for 120 min at 70 ^{o}C in a nitrogen filled glovebox. The passivation layer is used to reduce the hysteresis and stabilize the performance of OFETs. A thickness variation of TTC is firstly tested as in our report, and then a fixed thickness of 30 nm TTC is used in the OFETs later on.

The doped channel is deposited by co-evaporation, where the matrix (Pentacene) and dopant ($C_{60}F_{36}$) are thermally evaporated from two independent sources simultaneously in vacuum deposition chamber manufactured by Angstrom Inc, where the pressure is in the range of 5×10^{-8}Torr. The doping concentration (5 $wt.\%$) is controlled by the evaporation rates of the matrix and dopant. On top of the doped channel, a film of intrinsic Pentacene (40 nm) is deposited. The source and drain electrodes consist of a 40 nm thick film of heavily

p-doped Pentacene (Pentacene: $C_{60}F_{36}$, 8 $wt.\%$) as the injection layer, which is covered by a film of aluminum (40 nm) to ensure the conductivity of the electrodes.

MIS devices are fabricated by the same process as used for the OFETs described above. The devices are characterized using a Keithley SCS-4200 semiconductor parameter analyzer inside the glovebox at room temperature (300 K). The Atomic Force Images were taken with the help of the characterization facilities of the Advanced Materials and Liquid Crystal Institute of Kent State (TT AFM of AFM Workshop).

Aluminum is purchased from Sigma-Aldrich with a purity of 99.999 % . The intrinsic material of Pentacene is purchased from Creaphys with a purity of 99.99 %. The the p-dopant $C_{60}F_{36}$was synthesized and provided by the group of Dr. Boltalina (Univ. of Colorado). All materials are used without further purification.

Supporting Information Available

A discussion of the stability of the OFETs discussed above are given in the Supporting Information.

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