Split-Capacitor Boost Converter Operating in Boundary Conduction Mode with Impedance Matching for Kinetic Energy Harvesting

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***Abstract*—The proposed circuit intends for an electromagnetic generator to harvest kinetic energy. A synchronous split-capacitor boost converter operating in boundary conduction mode (BCM) is proposed to efficiently convert the AC input to a DC output. BCM operation is uniquely achieved through zero current detection (ZCD) control of an AC input enabling impedance matching. The ZCD control offers simplicity over previously reported methodologies. To reduce power consumption and increase efficiency, the proposed circuit topology combines the rectifier and power stage while dynamically controlling the power stage. The proposed circuit is designed and laid out in 0.13 µm BiCMOS technology. Post layout simulations verify the operation of the proposed circuit.**

Keywords—kinetic energy harvesting, electromagnetic generator, split-capacitor boost converter, boundary conduction mode, impedance matching.

I. Introduction

Internet of Things (IoT) devices will be able to provide innovative services and solutions in the realms of such as smart homes, smart cities, and smart factories. A major challenge for massive deployment of wireless IoT devices is to replace or recharge the batteries. Energy harvesting is a promising solution to the problem.

Electromagnetic generators (EMGs) have been studied extensively in [1]-[7]. An EMG can be excited via vibration, flow, or rotation. When an EMG rotates by ambient energy, it usually generates a low AC voltage. The low AC output voltage should be rectified and stepped up to power IoT devices. The conventional two-stage topology of a full-bridge rectifier and boost converter for rectification and amplification, respectively, incurs large power dissipation across the rectifying diodes [8]. To combat this issue, a single-stage boost converter topology, in which the rectifier and power stage are combined, was proposed [9]. The single-stage boost converter operates in discontinuous conduction mode (DCM), where the input impedance is dependent on the input voltage and output voltage [3], [10]. As the input and output voltage can vary, so the impedance.

To address the issue, the proposed circuit adopts the single-stage boost converter operating in boundary conduction mode (BCM). BCM operation is commonly used in higher power circuits for power factor correction [11]-[13]. However, it becomes more pronounced for energy harvesting applications [14]-[16]. Xu et al. utilized BCM operation for boost converter impedance matching [14]. Alhawari et al. implemented a fine resolution BCM boost converter [15]. Lou et al. adopted BCM operation to limit inductor leakage current found during DCM [16].

Our previous team, Xu et al., proposed a split-capacitor boost converter operating in boundary conduction mode [14]. The split-capacitor boost converter rectifies the AC input signal and transfers energy to a DC output in one single stage. For the low side switch of the boost converter, it utilizes one NMOS and one PMOS in series as the bidirectional switch to accomplish the rectification. However, multiple MOSFETs in one conduction path implies higher resistance, which leads to higher conduction loss. The proposed circuit improves our previous design presented by Xu et al. in [14]. The proposed circuit adopts a bulk controlled bidirectional switch and a simplified ZCD control circuitry for the BCM. It also adopts the synchronous rectification to further reduce the conduction loss of the power stage.

An equivalent circuit model for an EMG is given in Fig. 1. An AC voltage source is in series with an inductor, L_S, and a resistor, R_S. The inductance and resistance emulate the internal coil windings on an EMG. The reactance of the inductor, $|\omega L_S|$, is typically much smaller than R_S due to a low oscillation frequency [14]. Therefore, L_S is ignored in the proposed circuit for impedance matching. The specifications for our energy harvesting system are based on a previously designed EMG in [9]. The targeted EMG has a peak output voltage, Vp, of 1.5 V operating at 700 Hz and an internal resistance of 1 Ω.

The proposed circuit's objective is to prove BCM operation induced through ZCD control can match the impedance of a boost converter. The paper is organized as follows. Section II will introduce key preliminary topics. Section III will discuss the proposed energy harvesting circuit operation. Section IV will

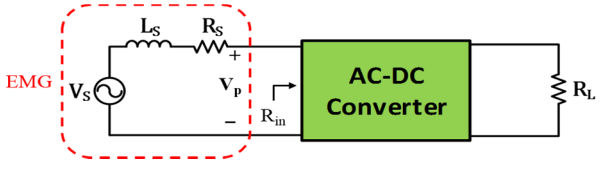

Fig. 1. EMG model.

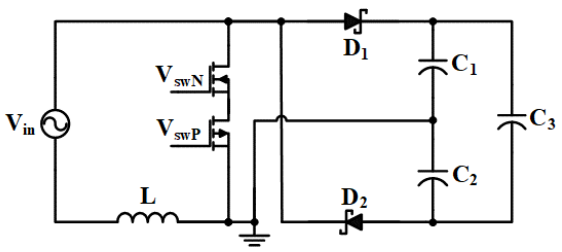

Fig. 2. Split-capacitor boost converter [9].

analyze the performance of the proposed circuit, and Section V will draw a conclusion.

II. Preliminaries

A. Impedance Matching

The maximum power transfer theorem states that maximum power is transferred to the load when the load impedance matches the source impedance. For energy harvesting, it is important to transfer maximum power load because the input power is small. A buck-boost converter operating in DCM is commonly used because the input impedance is easily controlled [17], [18]. The input impedance for a buck-boost converter operating in DCM is $R_{in}=2L/(D_1^2T_s)$, where L is the inductance, D_1 is the duty cycle and T_s is the switching period [17]. A boost converter operating in DCM has the input impedance as follows:

$$R_{in} = \frac{2L}{D_1^2 T_s}\left(1 - \frac{V_{in}}{V_{out}}\right) \quad (1)$$

The input impedance of a boost converter's is dependent on the input voltage V_{in} and output voltage V_{out}, resulting the impedance matching complex. The proposed circuit and our previous circuit in [14] address the problem through adoption of a single-stage boost converter operating in BCM.

B. Boundary Conduction Mode (BCM)

For BCM operation, the following charging period initiates when the inductor current, from previous period, returns to zero. The input impedance for a boost converter operating in BCM as derived in [14] is:

$$R_{\text{in}} = \frac{V_{in}}{I_{in}} = \frac{2L}{T_{on}} \quad (2)$$

Compared with (1), the input resistance for BCM solely relies on the inductance L and on-time or charging time T_{on}. Only one variable, T_{on}, must be controlled for the BCM.

C. Split-Capacitor Topology

A typical EMG for energy harvesting generates a low AC voltage with relatively high current. The AC voltage is rectified before being applied to a DC-DC converter. A full-bridge rectifier is not desirable because of the high voltage drop across the diodes and large conduction loss. To address the problem, Dwari and Parsa combined the rectifier and power stage called split-capacitor topology, which results in a smaller number of diodes on each conductance path and doubling the output voltage [9]. Fig. 2 shows the split-capacitor boost converter. The circuit is composed of an AC voltage source V_{in}, an inductor L, a bidirectional switch NMOS and PMOS, two Schottky diodes D_1 and D_2 and three capacitors C_1, C_2 and C_3.

Our previous circuit in [14] adopts the split-capacitor topology and is designed and fabricated in BiCMOS 0.18 µm technology. During the charging phases, current conducts through the two MOSFETs incurring high conduction loss and switching loss. Similarly, during the discharging phases, the diodes experience a large voltage drop and power loss. A zero current detector (ZCD) detects the point when the inductor currents becomes zero, which is necessary to operate the power stage in BCM. The ZCD algorithm implemented in our previous circuit is complex, requiring multiple comparators and op-amps. The numerous amount of static active components used for the ZCD draws large power dissipation because the active components waste energy when they are not needed.

III. Proposed Circuit

This section presents the proposed circuit with major building blocks and describes its operation.

A. Power Stage

The power stage of the proposed circuit is shown in Fig. 3. The circuit consists of the input voltage V_{in}, internal resistance R_s, inductor L, bidirectional switch M_1—M_3, PMOS M_4, NMOS M_5 and capacitors C_1—C_3. The voltage V_{in} is the input voltage to the converter, V_{sw} is the bidirectional switch voltage while V_{out1} and V_{out2} are the positive and negative output voltages, respectively.

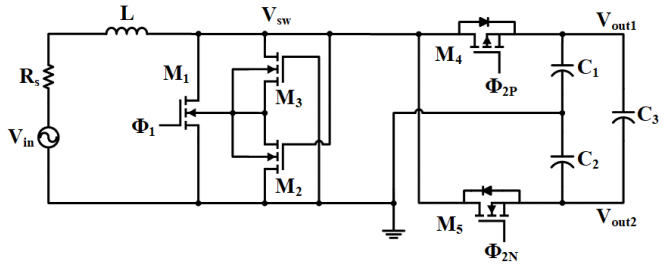

Fig. 3. Proposed power stage.

During the positive half cycle of V_{in}, the bidirectional switch is turned on by applying a positive voltage to Φ_1 to charge the inductor L. During the inductor L discharge period, the bidirectional switch is turned off. The discharge current flows through PMOS M_4 by applying a negative voltage to Φ_{2P}, allowing C_1 to charge. During the negative half cycle of V_{in}, the bidirectional switch is turned on by applying a positive voltage to Φ_1 to charge the inductor L. During the discharge period for the negative half cycle of V_{in}, the bidirectional switch is turned off. The discharge current flows through NMOS M_5 turned on by applying a positive voltage to Φ_{2P}. and charges C_2. The capacitors C_1, C_2 and C_3 use charge recycling to share energy.

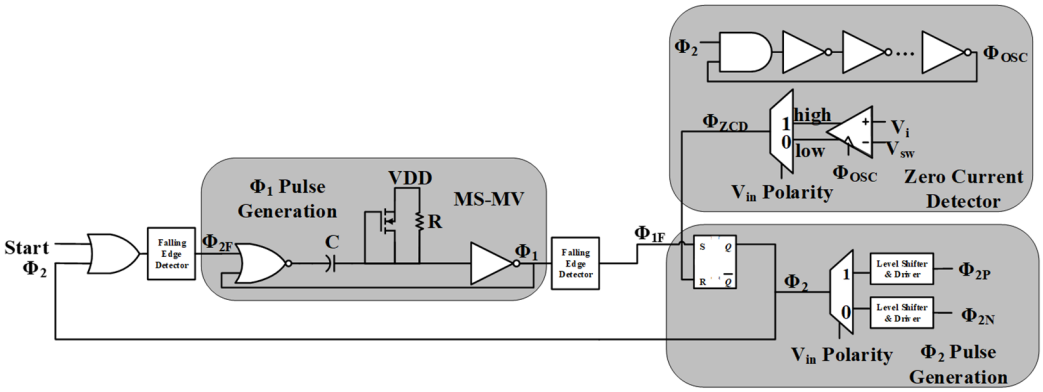

Fig. 4. Control circuit.

Comparing the proposed circuit with our previous circuit in [14], the major improvement includes the bidirectional switch, synchronous rectifiers M_4 and M_5, and the control circuitry including ZCD.

B. Bidirectional Switch

The bidirectional switch implemented in the proposed circuit is similar to the rectifier in [19] and shown in Fig. 3. The switch consists of three NMOS transistors, M_1—M_3. The bulk of M_1 always connects to the lower potential, so that a body diode can form in either direction. No current flows through M_2 and M_3 as their sole purpose is to control the bulk connection. The bidirectional switch topology is advantageous because one device performs the rectification and acts as the first stage of the boost converter. The combination reduces the conduction loss and switching loss for the converter.

C. Φ_1 Pulse Generation

To pulsate the bidirectional switch, an improved mono-stable multi-vibrator (MS-MV) is proposed and shown in Fig. 4. The circuit consists of a NOR gate, capacitor C, diode-connected MOSFET M_1, resistor R, and an inverter. The diode-connected MOSFET is an improvement to the previously reported MS-MV circuit in [20]. The proposed MS-MV is able to output a fixed-pulse width when a short pulse is injected. However, the conventional design has trouble retriggering with a fixed pulse width as it should wait for the capacitor to discharge. The diode-connected MOSFET decreases the discharge time constant.

D. Φ_2 Pulse Generation

The Φ_2 pulse generator sends signals to the synchronous MOSFETS M_4 and M_5. The Φ_2 pulse generator is shown in Fig. 4 and consists of a SR latch, demultiplexer, and two level shifters & drivers. When the signal Φ_1 falls, Φ_{1F} is generated by a falling edge detector and sets the SR latch. When the SR latch is set, the signal Φ_2 travels to Φ_{2P} during the positive cycle to drive M_4 and travels to Φ_{2N} during the negative cycle to drive M_5. The level shifter & driver circuits help to convert the signal to a higher voltage and provide more current to drive the MOSFETs in the power stage. The Φ_2 is reset by the ZCD circuit discussed in the next section.

E. Zero Current Detector

The ZCD circuit achieves BCM operation for the split-capacitor boost converter. The ZCD circuit shown in Fig. 4 consists of a ring oscillator, a dynamic comparator, and a multiplexer. The ring oscillator consists of an AND gate, to enable the ring oscillator, and a series of inverters. When Φ_2 is high, the ring oscillator is enabled and generates a clock signal, Φ_{OSC}, to pulse the dynamic comparator. The dynamic comparator is active only during a high Φ_{OSC} signal. Therefore, the comparator's static dissipation is near zero, helping to reduce the overall power consumption. Unlike [16], the dynamic comparator senses the voltage across the inductor instead of the PMOS M_4. This enables the zero crossing point to be detected during the positive and negative cycle without changing detection nodes. The dynamic comparator senses the voltage across the inductor to determine when V_i and V_{sw} become equal. At this time, the current through the inductor is zero, the critical point for BCM operation. The dynamic comparator output, either high or low depending on the input voltage polarity, resets the SR latch in the Φ_2 pulse generation circuit.

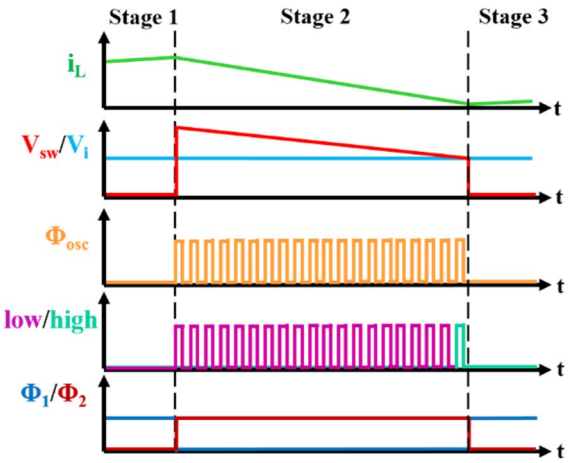

Fig. 5. ZCD waveforms.

The waveforms for the ZCD circuit are shown in Fig. 5. Stage 1 represents the time during the positive cycle; Φ_1 is a fixed on-time pulse generated by the MS-MV circuit. This fixed pulse is precisely controlled as it controls the input impedance

of the converter. Once Φ_1 drops low, beginning Stage 2, the falling edge detector sets the SR Latch beginning Φ_2. Pulse Φ_2 does not fall until the inductor current reaches zero. The zero crossing point is determined when V_{sw} equals V_i. Beginning Stage 3, the SR Latch is reset causing Φ_2 to go low. The falling edge of Φ_2 is detected, triggering the Φ_1 pulse generation circuit to start a new cycle.

F. Cold Start Capability

The proposed circuit is powered by the battery or supercapacitor, which is charged by the energy harvested by the circuit. When the storage device, specifically output capacitors, C_1 – C_3, are drained completely, the control circuit is not powered. Hence, the gates of the bidirectional switch and synchronous rectifiers are not switching.

During cold start, only the body diodes of the transistors and passive components are functioning [21]. The body diodes and the capacitors form a voltage doubler. When the EMG generates voltage V_{in} in Fig. 3, the current flows through the body diodes of M_4 and M_5. However, the body diode of M_1 prevents current from flowing through the bidirectional switch, so the capacitor C_3 can be charged to power the control circuit eventually.

IV. Post Layout Simulation Results

A. Layout

The proposed EH circuit was designed and laid out in 0.13 µm BiCMOS technology. The layout is shown in Fig. 6. The size of the core is 2 × 2 mm^2. All the passive components shown in Fig.3 and Fig. 4 are off-chip, and their values are L = 2.1 µH, C_1 = C_2 = 10 µF, C_3 = 20 µF, C = 100 pF, and R = 100 kΩ. With the C and R off chip, tuning the on-time pulse for different input impedance is possible. The simplified control circuity reduces the die area significantly compared our previous circuit.

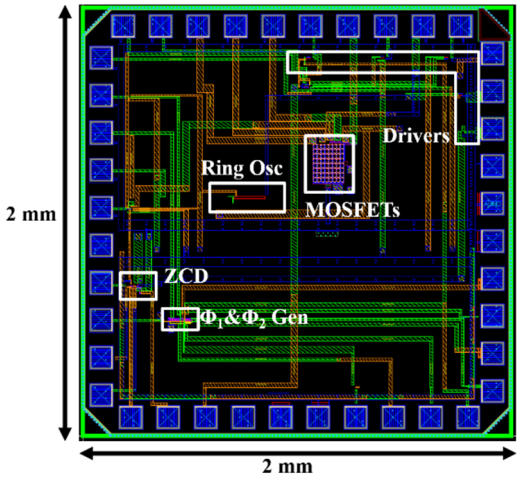

Fig. 6. Die photo.

B. Simulation Results

Post layout simulations were performed in Cadence. The EMG has peak input voltage of 1.5 Vp with 700 Hz frequency and 1 Ω source resistance Rs. Fig. 7 depicts simulated ZCD performance expected from Fig. 5. During Stage 2, i_L is discharging and the ZCD circuit is comparing V_i and V_{SW}. The dynamic comparator's low signal is oscillating up until $V_i = V_{SW}$, when the inductors zero current boundary is detected. Beginning Stage 3, Φ_1 and Φ_2 switch polarity initiating a new charging cycle. The waveforms exhibits the same behavior in Fig. 5, validating the circuit's performance.

Fig. 8 demonstrates the ability to cold start for the proposed circuit. As the EMG voltage V_{in} generates an AC voltage, the current charges the two capacitors, C_1 and C_2, and hence two capacitor voltages, V_{out1} and V_{out2}, start to increase.

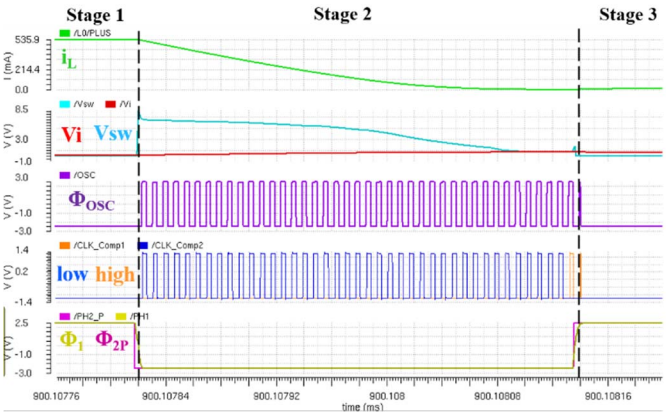

Fig. 7. Simulated ZCD waveforms.

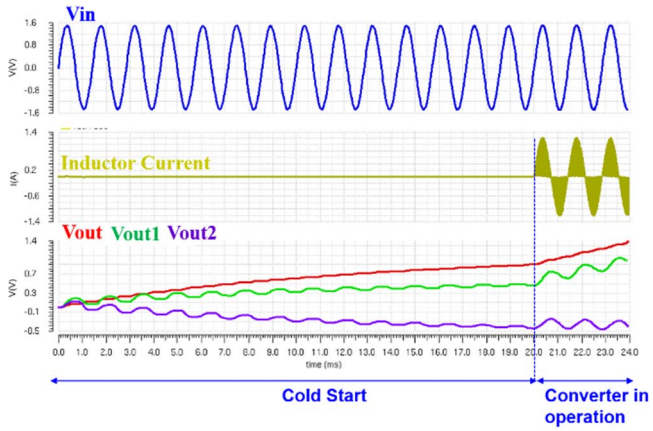

Fig. 8. Cold start to converter operation.

V. Conclusion

This paper presents a split-capacitor boost converter operating in BCM with impedance matching for kinetic energy harvesting. The ZCD control necessary for BCM offers simplicity over previously reported methodologies. The proposed design also implements synchronous rectification and

a bidirectional switch to decrease power stage conduction losses. The key advantage of the proposed circuit is the simplified control resulting in lower power consumption and increased efficiency.

ACKNOWLEDGMENT

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