Sub-microAmp Energy Harvesting and Power Management Units for Self-Powered IoT SoCs

Analog vs. Digital Implementations

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***Abstract*—The power consumption of ultra-low-power (ULP) Internet-of-Things (IoT) SoCs and components has been scaling down from µW to pW levels over the past ten years. Designing energy harvesting and power management units (EH-PMUs) that consume sub-µA quiescent current to efficiently provide such low load current is challenging. This paper reviews the trends and techniques for sub-µA EH-PMUs with a specific focus on the choice between analog and digital implementations. We first discuss ULP EH-PMU design trends based on recent published results and then analyze three design examples. The first example reviews a popular multiple-input multiple-output (MIMO) EH-PMU architecture with ultra-low quiescent current and compares tradeoffs for analog vs. digital zero-current detectors. The second example discusses the design of analog and digital low-dropout regulators (LDOs) with a performance comparison from silicon measurement results. The digital LDO can achieve faster settling time for step response than the analog structure, but the analog LDO has no ripple, making it ideal for noise-sensitive blocks like RF. Finally, an analog power monitor for maximum-power-point tracking (MPPT) in a piezoelectric energy harvester utilizes subthreshold transistor characteristics to simply a complex algorithm and to maintain low power consumption.**

Keywords—Energy harvesting and power management units; self-powered; system-on-chips; sub-microamp; internet-of-things; ultra-low-power; analog vs. digital implementations

I. Introduction

Self-powered and energy-harvesting Internet-of-Things (IoT) system-on-chips (SoCs) [1]-[4] have been gaining attention in recent years as system power consumption has dropped to match the available energy harvested from the environment. An energy-harvesting system with no batteries has the advantages of being maintenance free and more environmentally friendly. Furthermore, self-powered SoCs can be deployed in many places where battery changing is difficult or impossible, like inside building structures or the human body. For such a self-powered system, the energy harvesting and power management unit (EH-PMU) is an indispensable block whose function is to extract the energy from the environment, store it on a storage node like a supercapacitor, and then regulate and provide energy to the loads based on different requirements for the voltage supplies. Fig. 1 shows the system block diagram of a typical self-powered SoC. The energy flow path goes through an energy harvesting interface, an energy storage node, and different types of voltage regulators for different voltage supply (VDD) needs. For voltage regulators, a switched-mode power converter (SMPC) is usually adopted for the first stage to down-convert

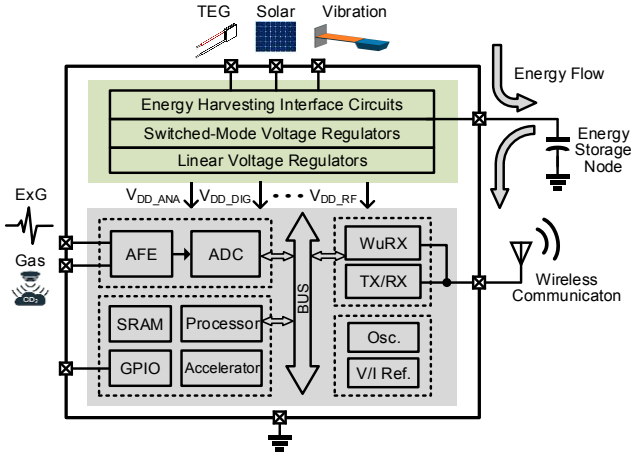

Fig. 1. System block diagram of a typical self-powered IoT SoC including the EH-PMU and its loading components.

the voltage from a high storage voltage to a low supply voltage with high power efficiency. This initial stage is often followed by low-dropout regulators (LDOs) to provide fast step response and isolate the switching ripple and noise of the local voltage supplies from outputs of the SMPC. For the loads, self-powered SoCs usually include a variety of loading components from analog front-ends (AFEs) and analog-to-digital converters (ADCs) for the sensor interface to processors for digital processing and wake-up receivers (WuRXs) and RF transceivers (TX/RX) for wireless communication.

There are many design considerations for EH-PMUs. The EH must convert energy from energy transducers to a usable voltage level for storage or direct deliver energy to the regulators, so EH circuits need to manage maximum-power-point tracking (MPPT), cold start-up, a wide input power range, etc. The PMU deals with the output to the loads, which needs to manage a wide output power range, step response, output voltage ripple, etc. Among all those metrics, the EH conversion efficiency and PMU power efficiency rank as highly important. The equation for the end-to-end EH-PMU power efficiency is given as follows.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_Q + P_{SW} + P_{COND}} \quad (1)$$

where P_{IN} and P_{OUT} stand for input and output power, and P_Q, P_{SW}, and P_{COND} stand for quiescent power loss, switching loss, and conduction loss in the EH-PMU circuits, respectively. For a high output power condition, the switching loss and conduction loss dominate due to negligible quiescent power compared with

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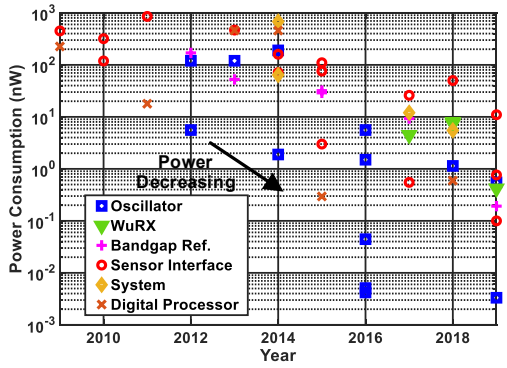


Fig. 2. The lowest power consumption of different types of loading components from 2009 – 2019 ISSCC/JSSC publications.

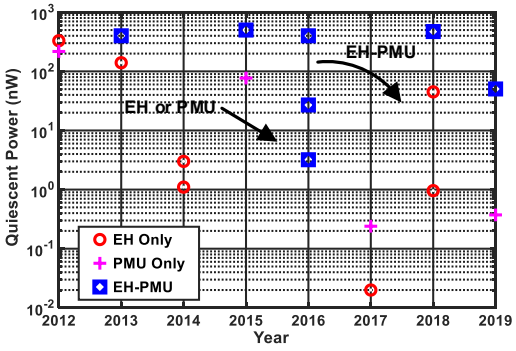


Fig. 3. The lowest quiescent power of EH-PMUs from 2012 – 2019 ISSCC/JSSC publications.

the total output power. For the low output power case, where the quiescent power is comparable to the output power, the quiescent power loss can dominate the total power loss. For many self-powered SoCs and components, which are designed to be ultra-low power to increase the system life time, this latter condition, where quiescent power limits efficiency, is more common. In an energy harvesting context, the available energy and environmental conditions can further limit available power. In poor environmental conditions, where energy is less available, the EH-PMU needs to consume ultra-low quiescent power to continue to provide meaningful power to the system at acceptable efficiency.

The system load power that the EH-PMU needs to support clearly depends on the design of the various loading components. Fig. 2 shows collected data of the lowest power consumption for a variety of components from the last 11 years. There are several trends that emerge from this figure. First, the power consumption of all the types of components is decreasing by orders of magnitude with time. This reduction in part depends on technology and voltage scaling but also on the invention of new circuit architectures and approaches. Second, the power consumption from 2009 to 2015 and after has changed from the µW-level down to pW-level, so the design of EH-PMUs must now gradually consider to support pW loads. Third, when the power comes to the pW-level, further power scaling slows down (with the exception of oscillators, which have simple structures and Hz-to-sub-Hz frequency range [5]), perhaps limited by silicon process parameters like the leakage through transistor gates and PN junctions.

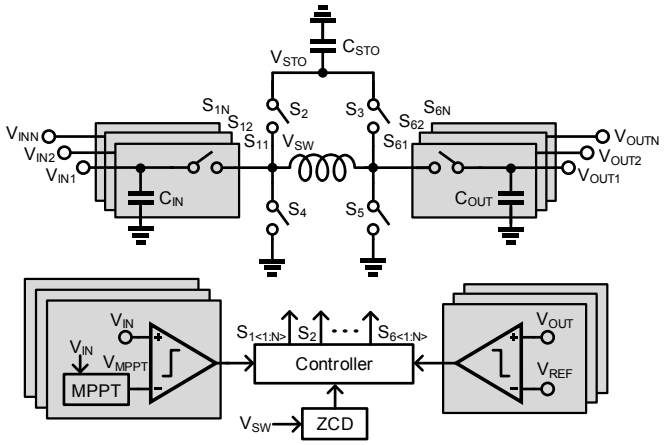


Fig. 4. Architecture of a classic MIMO EH-PMU.

Fig. 3 shows the lowest quiescent power of ultra-low-power (ULP) EH-PMU designs in recent eight years. There are two insights we can find from this plot. First, the EH-only or PMU-only circuits have already scaling down to the pW-level from the µW-level, and this trend is consistent with the loading components. Second, the power consumption of the integrated EH-PMU system, which typically is a versatile multiple-input multiple-output (MIMO) structure, is not scaling down as fast, perhaps due to the high design complexity of such a system.

From the two plots and the analysis, we observe that next-generation EH-PMUs need to be power efficient when powering nW or even pW loading circuits, which makes EH-PMU design very challenging. One of the keys to achieving this goal is to make the EH-PMU consume sub-µA quiescent power. Although many ULP techniques have been developed, the remainder of this review paper mainly focuses on the comparison of ULP analog and digital implementations for sub-µA EH-PMUs. The paper is organized as follows. Section II reviews a classic architecture for a multi-input multi-output EH-PMU with a comparison of analog and digital zero-current detectors (ZCDs). Section III discusses the analog and digital linear voltage regulator design with silicon measurement results, and Section IV discusses analog vs. digital signal processing and reviews an analog power monitor design for MPPT in a piezoelectric energy harvester. Finally, Section V briefly summarizes the highlights and conclusions of this paper.

II. Design of MIMO EH-PMUs

A. Architecture of an MIMO EH-PMU

Multi-input multi-output EH-PMUs [6]-[9] have become prevalent in recent years due to their ability to connect multiple energy sources and power multiple loads. Also, by delivering power from the harvesters to the loading circuits in only one stage instead of two (e.g., [10]), they eliminate additional losses from cascading two lossy stages. To optimize the power consumption and performance, most MIMO PMUs leverage hysteresis control. Fig. 4 shows a classic architecture for an MIMO EH-PMU, which includes power switches, comparators, MPPT detection blocks, a ZCD, and a digital controller. The comparators on the bottom left set the output voltages of the energy transducers to V_{MPPT}s, which are generated by the MPPT detectors as the optimal voltages for power transfer.

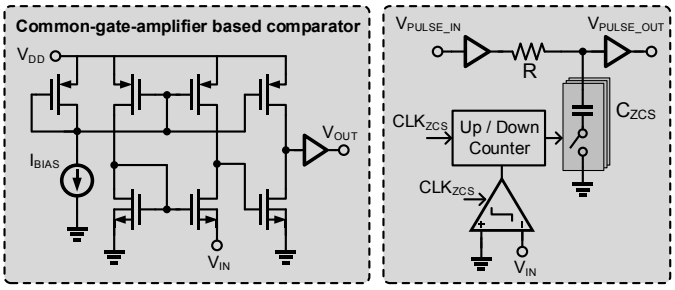


Fig. 5. Analog vs. digital zero-current detector.

The comparators on the bottom right regulate each output voltage to its reference voltage, V_{REF}. Options for these comparators include a hysteresis comparator for asynchronous control or a clock-driven comparator for synchronous control, which uses time information as the hysteresis value for the regulation. For sub-μA designs, the power converters usually work in discontinuous-conduction mode (DCM) [11] due to the ultra-light load at the output.

This MIMO architecture has several advantages. First, it has a very low quiescent current, since most of the components are digital circuits including the digital control, comparators, and passives. Also, the hysteresis control works as pulse-frequency modulation (PFM). When the load is larger, the frequency of switching pulses increases, and, when the load is reduced, the frequency reduces correspondingly. The controller can be improved to adaptively change the on-time of the switch, T_{ON}, as well as the switching frequency, F_{SW} [6] [7]. Second, it has a fast response to the load change since the output changes can be immediately detected by the hysteresis control. Whenever the output voltage is lower than its V_{REF}, it will trigger the comparator and toggle the power transistors to send energy to the appropriate loads, which is not like a traditional analog feedback loop whose step response depends on the control loop bandwidth. Third, the low-complexity control only includes the comparators and digital logic, unlike an analog feedback loop, which is often used in high output power applications, and needs a compensator for the loop stability [12]. Fourth, this structure has a high flexibility, which can be easily extended to any number of inputs and outputs, allowing connection with more energy harvesters and more power supplies for load circuits. Besides the adaptive T_{ON} and F_{SW}, some other techniques have also been proposed to reduce the quiescent current and increase the power efficiency for this structure, like switch size modulation [6] and automatic source selection [9].

B. Analog vs. Digtial Zero-Current Detector

ULP EH-PMUs usually work in DCM due to light loading currents, which requires a zero-current switching (ZCS) circuit to turn off the power switches when the inductor is fully discharged, otherwise the inductor will conduct current in reverse and deteriorate the power efficiency. A zero-current detector detects when the inductor current crosses zero and is an indispensable block in every DCM EH-PMU. The ZCD needs to be very fast to quickly detect the crossing point, which makes it one of the most power-hungry blocks in an EH-PMU system. Assuming the inductor value is 22μH and the load voltage is 0.5V, the inductor will experience 1mA reverse current after only a 44ns delay.

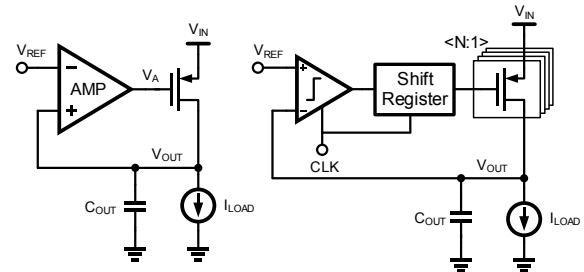


Fig. 6. Block diagram of (a) a traditional ALDO and (b) a traditional DLDO.

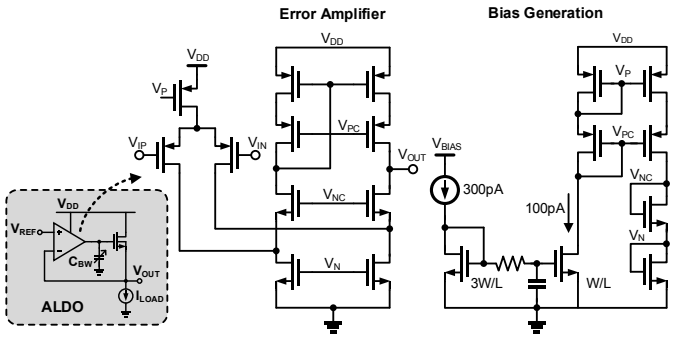


Fig. 7. Schematic of a sub-nA fully integrated NMOS ALDO.

There are usually two types of ZCD structures: the analog ZCD and digital ZCD shown in Fig. 5. The analog ZCD is a common-gate amplifier, used as a comparator. To get a fast speed, the bias current is usually large, up to a few μA. To reduce the average power consumption, duty-cycling has been widely used to turn on the comparator before the inductor switching and turn it back off after completing the detection. By using duty-cycling, the power consumption can be reduced to a few nW [6]. A digital ZCD includes a clock-driven comparator and an up-down counter to control the pulse width. The digital ZCD does not consume any constant power, so it is preferable in pW switching regulator or harvester designs [13] [14]. The drawback of the digital ZCD is it can only change a fixed step for the pulse width based on the comparison results, so it cannot respond to a fast or sudden change in the pulse width, unlike the analog ZCD, which can continuously detect the pulse width changing. So, the selection of different ZCD structures depends on the different requirements of the system.

III. SUB-NA ANALOG VS. DIGITAL LDO DESIGN

In recent years, with more and more loads working down to pW-level, the voltage regulator with sub-nA quiescent current consumption is becoming more critical. Previous switching voltage regulators [13] can achieve pW power but suffer from slow response time and large output switching ripple. Linear voltage regulars offer a fast response and a clean voltage supply. This section will introduce the design of sub-nA LDOs with examples of an analog LDO (ALDO) and a digital LDO (DLDO), respectively, and the performance comparison and analysis of the two types of LDOs.

A. Overview of Traditional Analog and Digital LDOs

Fig. 6(a) shows the schematic of a traditional ALDO,

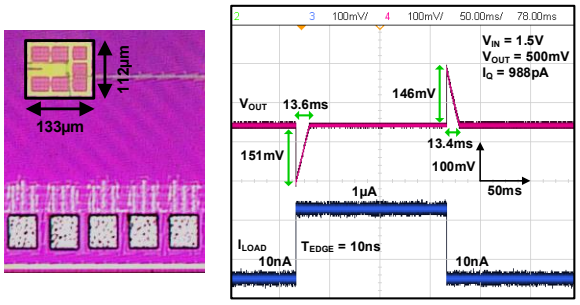


Fig. 8. Chip micrograph of the ALDO and measured output transient step response.

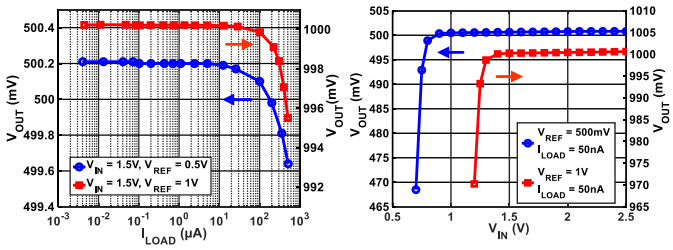


Fig. 9. Measured load and line regulation of the ALDO.

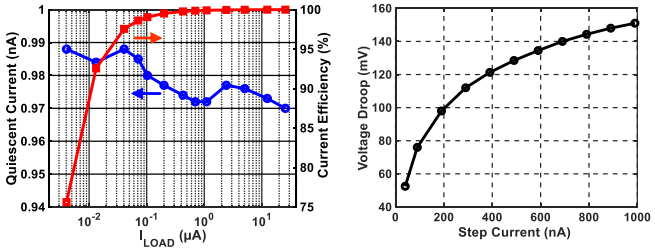


Fig. 10. Measured quiescent current, current efficiency and voltage droop vs. load step of the ALDO.

which uses an error amplifier to amplify the voltage difference between V_{OUT} and V_{REF}, adjust the gate voltage of the power transistor, and make the output voltage the same as the reference voltage. The dominant pole is at the output of the LDO, and for a pW-to-nW design, the output capacitor needs to be very large ~µF to make the feedback loop stable.

The digital LDO is first introduced in [15], motivated by the need for digital V_{DD} scaling for subthreshold (sub-V_T) circuits. A traditional ALDO needs a high voltage overhead for the high-performance error amplifier, which usually includes several stacked transistors, so it is less suitable for ultra-low-voltage circuits. DLDOs also benefit from flexible control schemes to improve their performance [16]-[19]. A DLDO uses a comparator to compare V_{OUT} with V_{REF} for each clock period, and, based on the comparison results, it increases or decreases the shifter register value to turn on/off switches in the PMOS switch array to regulate the output voltage.

B. Sub-nA Fully Integrated Analog LDO

A traditional sub-nA ALDO needs a large output capacitor, which is not ideal for many applications where form factor is strictly limited. Fig. 7 shows the schematic of a fully integrated sub-nA ALDO, which includes a NMOS power transistor, an error amplifier, and its bias generation circuit. The amplifier

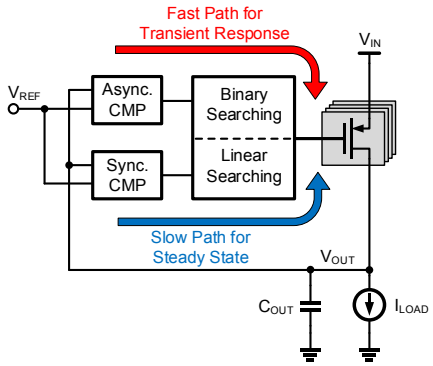


Fig. 11. Concept of the hybrid control scheme in the DLDO [20].

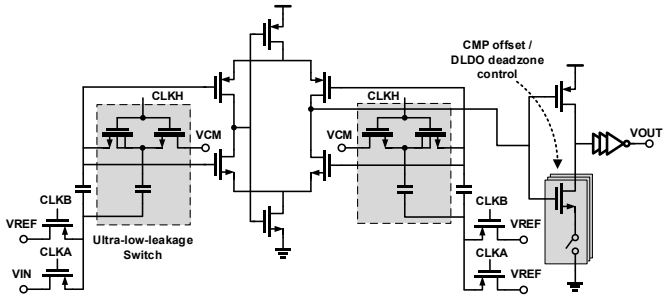


Fig. 12. Schematic of the inverter-based, self-biased and switched-cap comparator [20].

adopts a low-voltage folded-cascode structure, which can generate a high voltage gain with only one stage. The amplifier output has a high impedance that is set to be the dominant pole of the LDO, which eliminates the output capacitor from a traditional LDO to make the loop stable. C_{BW} is used to tune the LDO bandwidth with a value of 1-9.2pF. The ALDO uses an NMOS instead of PMOS as the power transistor, which has a lower output impedance and makes the feedback stable. A 300pA bias current feeds into the LDO and scales down to 100pA for the bias generation block. The LDO adopts 2.5V IO devices to reduce the transistor gate and channel leakage and the simulated voltage gain of the error amplifier is ~72dB.

The ALDO is fabricated in a 65nm CMOS LP process. Fig. 8 shows the chip micrograph with an area of 0.015mm^2 and the measured transient step response, which has a droop voltage of 151mV and settling time of 13.6ms for a 10nA to 1µA step input when V_{IN} = 1.5V and V_{OUT} = 0.5V. Fig. 9 shows the measured load and line regulation. As we can see, load range for the ALDO is from about 4nA up to 500µA. However, the phase margin will decrease for a light load, and the droop voltage will increase for a large step input. Fig. 10 shows the measured quiescent current with a minimum value of 970pA.

C. Sub-nA Digital LDO with a Hybrid Control Scheme

The power and speed trade-off in a traditional ALDO is strictly limited. However, with digital techniques, there are more digital control algorithms that can help with achieving pW operation and high performance simultaneously. There are basically four control schemes for DLDOs: synchronous, asynchronous, binary searching, and linear searching. Due to the power limitations in sub-nA designs, the highest clock frequency is usually tens of kHz or even less, so there is no high

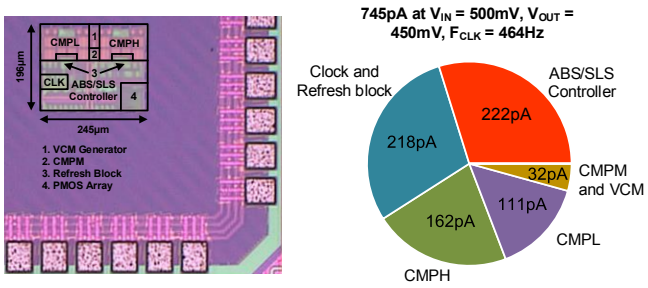


Fig. 13. Chip micrograph of the hybrid control DLDO and the measured quiescent current breakdown of the DLDO [20].

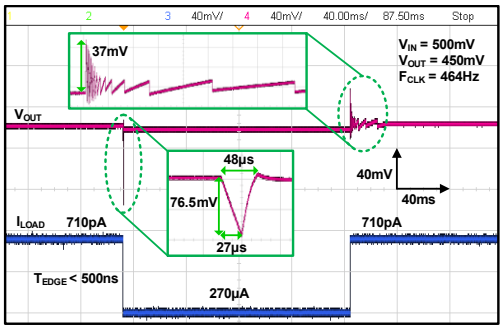


Fig. 14. Measured transient step response of the DLDO [20].

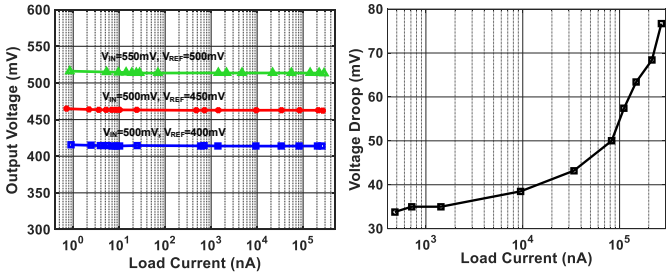


Fig. 15. Measured DLDO load regulation and voltage droop [20].

TABLE I: PERFORMANCE SUMMARY AND COMPARISON OF THE SUB-NA ALDO AND DLDO

	I_Q	Load Range	ΔV_{OUT} @ ΔI_{LOAD}	Settling Time	V_{IN}	Dropout Voltage	Output Ripple	C_{OUT}
ALDO	970pA	4nA - 0.5mA	151mV @ 1µA	13.6ms	0.7-2.5V	300mV	None	None
DLDO [20]	745pA	710pA - 0.27mA	76.5mV @ 0.27mA	48µs	0.5-1V	50mV	2mV	100nF

frequency clock, which means the synchronous control cannot detect the load change quickly enough during step response. The asynchronous and binary searching control both offer the advantage of a fast response. By combining the two schemes, it can get a fast response during transients and combining the synchronous and linear searching control schemes can improve performance during steady state, like low ripple and small steady-state error.

This hybrid control scheme, asynchronous binary-searching/synchronous linear-searching (ABS/SLS), is proposed in [20] and the concept of the hybrid control scheme is shown in Fig. 11. Whenever there is a step load change, the DLDO will use the ABS path including an asynchronous (async) comparator and a binary searching algorithm to get a fast response, and when V_{OUT} settles back to the steady state, it will go through the SLS path including a synchronous (sync) comparator and a linear searching algorithm. The detailed circuit-level implementation of the ABS/SLS DLDO is in [20]. This DLDO includes all the supportive blocks including the clock generation, and it utilizes the comparator offset as a deadzone, which eliminates the need for multiple voltage references. One of the critical blocks in the DLDO design is the async comparator, which dominates the performance of the transient step response. There are many comparator structures that have been analyzed to optimize power and speed [21]. Among all the structures, the inverter-based comparator has one of the highest power efficiencies due to utilizing PMOS and NMOS as input differential pairs together. The traditional inverter-based comparator needs to connect with the gate of both the PMOS and NMOS, which is not applicable to the DLDO design, because the input voltage, which is the output of the DLDO, is very close to the voltage supply, thus it cuts off the PMOS pair. To solve this issue, a switched-capacitor topology is used in this comparator. Fig. 12 shows the schematic of the async comparator, which adopts the inverter-based, self-biased and switched-cap structure. This comparator shows an excellent trade-off between power and speed, and the measurement results show the async comparator has a falling edge delay of 25.7µs and rising-edge delay of 15.4µs for a 30mV input step [20].

The hybrid control DLDO is fabricated in a 65nm CMOS LP process with a chip micrograph and measured current breakdown shown in Fig. 13. The measured minimum quiescent current is only 745pA when V_{IN} = 500mV, V_{OUT} = 450mV, and clock frequency is 464Hz. Fig. 14 shows the measured step response, which has a 76.5mV droop voltage, 27µs response time, and 48µs settling time for a 710pA to 270µA step input when the system clock is only 464Hz, thanks to the hybrid control scheme. The measured load regulation and voltage droop are shown in Fig. 15. The measured dynamic load range is from 710pA to 270µA, spanning over 5 orders of magnitude.

D. Performance Comparison of the sub-nA ALDO and DLDO

The performance summary of the ALDO and DLDO is shown in Table I. The two LDOs both consume sub-nA quiescent current. Although the load range of the two LDOs are similar, the DLDO has 2× lower droop voltage for a 270× larger step input, and it also has 283× faster settling time and 6× lower dropout voltage. However, the input voltage of the ALDO can go up to 2.5V due to using 2.5V IO devices, and there is no switching ripple for the ALDO. Also, the ALDO is fully integrated, so it does not need any output capacitors.

The performance comparison shows that the DLDO has advantages over ALDO in many aspects, like faster settling time, low dropout voltage, and lower input voltage, due to the benefits from low-voltage operation of digital circuits, flexible control algorithms and better power and performance scalability. But the ALDO has no switching ripple, which is suitable for noise sensitive circuits like RF transceivers. Recently, hybrid analog and digital LDOs have been reported [22]-[24] that get the advantage of the two types of LDOs to improve the overall performance further.

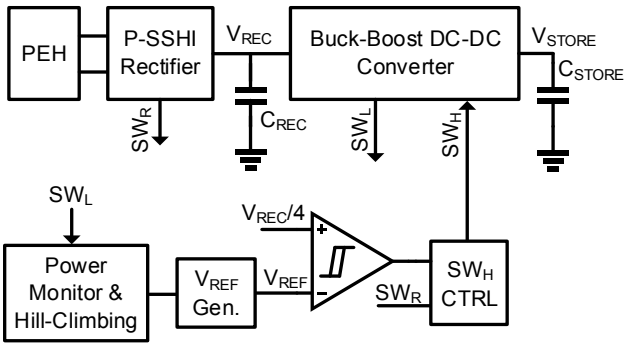


Fig. 16. System architecture of the piezoelectric energy-harvesting system including the MPPT control loop [25].

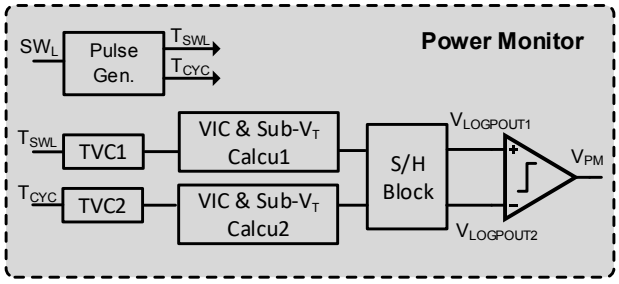


Fig. 17. Block diagram of the analog power monitor [25].

IV. ULP Analog MPPT Algorithm for Piezoelectric Energy Harvesting

A. Signal Processing in Analog vs. Digital Domain

EH-PMUs generally include two major sub-blocks, the power stage and control circuits. With more complex control algorithms developed to improve the EH-PMU performance, achieving those algorithms with ultra-low power is becoming challenging. The signal processing of those algorithms is typically achieved in the digital domain. To implement the digital signal processing, the analog signals need to be converted to digital signals with an ADC first, followed by a digital signal processing unit (DSP) or a custom accelerator. After signal processing, the outputs need to be converted back to the analog domain if a continuous analog control is needed. An oscillator is also necessary to provide the clock for the digital blocks. The power overhead of the digital processing is mainly determined by the clock frequency, the number of digital bits for the ADC, and the complexity of the DSP.

For some specific algorithms, the digital processing process can be dramatically simplified in the analog domain, which uses the sub-V_T characteristics of the transistors [25] or analog sub-blocks, like amplifiers [26]. Another benefit of signal processing in the analog domain is that signals do not need to convert to the digital domain first, avoiding the power for converting and the output can be directly used for the analog control.

B. Analog Power Monitor for MPPT of Piezoelectric Energy Harvesting

To extract the maximum power from energy transducers, the input impedance of the energy harvesting circuits needs to match the output impedance of the energy transducers, which is called MPPT. For piezoelectric energy harvesters (PEHs), MPPT

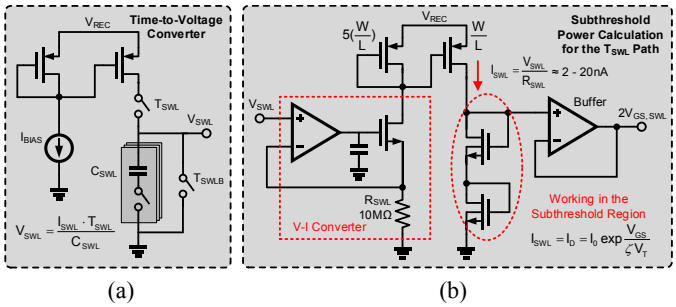


Fig. 18. Implementation of (a) the time-to-voltage converter and (b) the sub-V_T power calculation block [25].

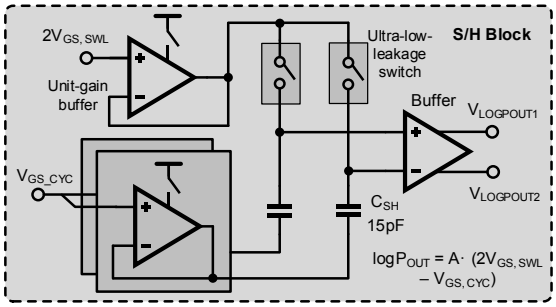


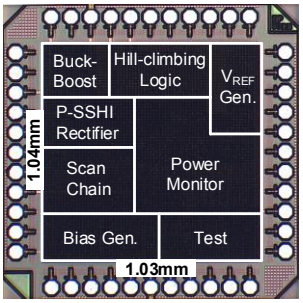
Fig. 19. Implementation of the sampling and hold block [25].

methods vary for different rectifiers. Parallel-synchronized-switch harvesting-on-inductor (SSHI) rectifiers have a high energy extraction improvement [27] [28], but their MPPT depends on the rectifier flipping efficiency and the characteristics of the PEH and excitation source, which makes the MPPT very complicated. Perturb & Observe (P&O) [29] [30] is a common MPPT algorithm, which is independent of PEH and rectifier characteristics, so it can be used with the parallel-SSHI rectifier.

Fig. 16 shows the system architecture of a piezoelectric energy-harvesting system [25] including the P&O MPPT control loop, which consists of a power monitor, a hill-climbing logic, and a reference generator. The power monitor calculates the output power of the piezoelectric harvesting system and compares the previous value with the current value to determine the P&O transition direction. An output power evaluation algorithm has also been proposed in [25]:

$$P_{OUT} = \frac{\Delta E}{T_{CYC}} = \frac{V_{STORE}^{\ 2} \cdot T_{SWL}^{\ 2}}{2 \cdot L \cdot T_{CYC}} \qquad (2)$$

where V_{STORE}, T_{SWL}, and T_{CYC} stand for the voltage on the energy storage node, pulse width, and period of the switching control signal during the inductor discharging phase. The power monitor is implemented in the analog domain, which utilizes the V-I exponential relationship in the MOSFET sub-V_T region. The block diagram of the power monitor is shown in Fig. 17, which includes a pulse generator, two time-to-voltage converters (TVCs), two sub-V_T power calculation blocks including voltage-to-current converters (VICs), a sampling and hold (S/H) block, and a comparator. The detailed schematic of the TVC is shown in Fig. 18(a), which uses a bias current to charge a capacitor, and the charging time is determined by the pulse width, T_{SWL}, which generates a voltage proportional to T_{SWL}. Fig. 18(b) shows the schematic of the sub-V_T calculation block.



Power monitor	Quiescent Current (nA)
TVC	122.3
Sub-V_T calculation	184.2
S/H block	63.1
Comparator	0.53
Pulse Gen.	60
Total	430.13

Fig. 20. Chip micrograph [25] and simulated quiescent current breakdown of the analog power monitor.

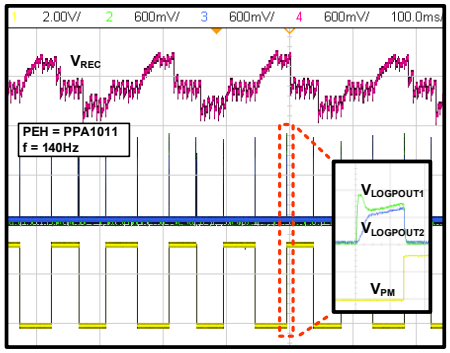


Fig. 21. Measured MPPT steady-state waveform [25].

The bias current used for the sub-V_T transistor is set from 2nA to 20nA. The schematic of the S/H block is shown in Fig. 19, where unit gain buffers have been used to get a fast sampling time. To reduce the average power of those buffers, they are designed to be duty-cycled. Ultra-low-leakage switches [30] further reduce the voltage error on the sampling capacitor.

The piezoelectric energy-harvesting system including the analog power monitor is fabricated in a 130nm CMOS process. The chip micrograph and simulated current breakdown of the analog power monitor is shown in Fig. 20. The total quiescent current of the power monitor is 430nA, and sub-V_T calculation block including the VIC consumes 184.2nA. Fig. 21 shows the measured transient waveform of the P&O MPPT with a ~300 mV voltage step, where $V_{LOGOUT1}$ and $V_{LOGOUT2}$ are the calculated output power, and V_{PM} is the output of the power monitor. Fig. 22 shows the tracking efficiency vs. open circuit voltage (V_{OC}) and excitation frequency. The measured maximum tracking efficiency is 97%, and the overall tracking efficiency across V_{OC} and vibration frequency is larger than 90%. Table II shows that the piezoelectric harvesting system achieves a 417% FOM rectifier, which is 4× higher than the full bridge rectifiers used with other MPPTs, and a maximum 97% tracking efficiency MPPT simultaneously.

C. *Future Work for MPPT Algorithms*

The analog power evaluation algorithm and the implemented power monitor for the piezoelectric harvesting system have proven to have an ultra-low quiescent current and high tracking efficiency for the P&O MPPT and a simpler implementation than digital processing using ADCs, DSPs, and clocks. However, signal processing in the digital domain has the advantage of being immune to many effects that analog circuits

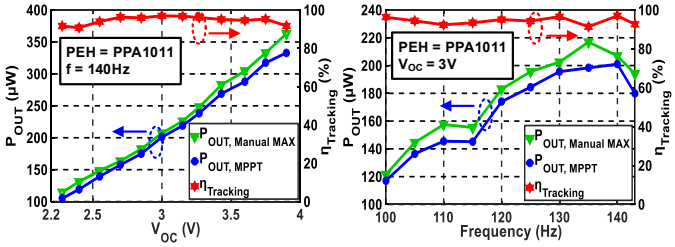


Fig. 22. Measured MPPT tracking efficiency vs. V_{OC} and excitation frequency [25].

TABLE II: PERFORMANCE COMPARISON OF STATE-OF-THE-ART PIEZOELECTRIC ENERGY-HARVESTING SYSTEMS AND MPPTS

	This work	[31] ISSCC'14	[30] ISSCC'13	[28] ISSCC'16	[32] JSSC'14
Process	0.13μm	0.35μm	0.25μm	0.35μm	0.18μm
Harvester Type	Piezoelectric	Piezoelectric	Electrostatic	Piezoelectric	Piezoelectric
Piezoelectric Harvester	MIDE PPA1021 & PPA1011	MIDE V20W & V21BL	N/A	MIDE V21B & V22B	Custom MEMS
Harvester Capacitance (nF)	20 & 100	11	N/A	26, 20 & 9	8.5
Rectifier Scheme	Parallel-SSHI	FBR	Off-chip FBR	Parallel-SSHI	Parallel-SSHI
Operation Frequency (Hz)	100 - 180	N/R	N/R	134.6 - 229.2	155 & 419
MPPT	Yes	Yes	Yes	No	No
MPPT Algorithm	P&O	Fractional V_{OC}	VS-P&O	N/A	N/A
Flipping Efficiency	0.86	N/A	N/A	0.93	0.76**
Energy-Extraction Improvement (FOM*)	**417%**	**90%**	**< 100%**	**681%**	**266%****
Maximum MPPT Efficiency	**97%**	**99%**	**99.9%**	**N/A**	**N/A**
Rectifier (>400% FOM) + MPPT (>90% Efficiency)	**Yes**	**No**	**No**	**No**	**No**

N/A = Not Applicable; N/R = Not Reported; * FOM = $P_{REC}/(C_P \cdot V_{OC}^2 \cdot f)$; ** Calculated from the paper

are sensitive to, like transistor offsets, output noise, signal coupling, and current leakage. The power evaluation algorithm for MPPT can also be implemented in the digital domain in the future, which potentially can achieve ultra-low power if designed properly.

V. CONCLUSIONS

This paper has reviewed the design trends and techniques for sub-microamp EH-PMUs. Analyzing the power consumption of IoT SoCs and components in the past ten years shows that the power of these loads is reducing from μW to pW levels, so this trend requires that EH-PMUs have sub-μA or even sub-nA quiescent current to power those loads efficiently. Ultra-low-power techniques for the EH-PMU design were reviewed and discussed with three examples. Specifically, we analyzed and compared analog vs. digital implementations for a classic MIMO EH-PMU architecture with analog vs. digital zero-current detector designs and for analog vs. digital LDO designs, and we evaluated an analog MPPT algorithm for piezoelectric energy harvesting. The three examples show the relative strengths and weaknesses of the two approaches, both of which can be optimal for the sub-μA space depending on the needs of the system and application.

Although traditional analog techniques still have the advantage over their digital counterparts for some capabilities like continuous-time signal detection or amplification and eliminating voltage ripple, digital implementations tend to provide more options for optimizing tradeoffs between ultra-low power and other performance metrics. Furthermore, the emerging hybrid strategies that combine strengths from both approaches promise even better solutions in some contexts for sub-μA EH-PMU design.

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