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Impact of front-end wearout mechanisms on FinFET SRAM soft error rate

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A B S T R A C T

We build a modelling and simulation flow to study how the front-end wearout mechanisms affect the FinFET SRAM soft error rate. This flow incorporates process variation, such as device dimensions, and degradation parameters. We first checked the impact of process parameters on critical charge and soft error rate. It is found that a larger gate length and higher temperature help us obtain better reliability for a FinFET SRAM cell under radiation, with a higher Q_{crit} and lower SER. Then, the time-dependent shift of Q_{crit} and SER is displayed. Within its range between 0% and 50%, a lower duty ratio leads to worse reliability due to soft errors. Moreover, a higher transition rate causes worse reliability.

1. Introduction

Radiation effects are an important issue for electronic circuits fabricated with advanced technologies, like FinFETs. These effects exist in harsh radiation environments, such as in space, in the sea, and in the space close to packaging and soldering materials, which contain radioactive contaminants. When circuits are operating in an environment with high energy particles, such as Alpha particles and neutrons, the particles' energy is transferred to the circuit by generating electrical charges and by causing transient currents. If the amplitude of transient currents is high enough, a circuit's node content is flipped easily. This phenomenon is known as a soft error. Although this interruption doesn't cause hard (permanent) breakdown, it could lead to the malfunction of an electronic system.

SRAMs occupy a majority of the area of a System on Chip (SoC). They are the main source of the SoC soft error rate (SER). FinFET SRAMs are suitable for many applications because of their low leakage and high density [1–5]. However, the reliability of FinFET SRAMs in the presence of soft errors should be taken seriously.

Accurate modelling and optimization for Alpha-SER in a deep-nanometer 6 T SRAM cell is performed with an experimental approach in [6]. [7] explored the soft-error performance evaluation of emerging low power devices, such as III–V FinFETs. [8] compared the SER of different SRAM cells (high-density and high-performance) when they are irradiated by alpha particles, thermal neutrons, and high-energy neutrons, respectively. It is found that a high-power cell is more sensitive to a single event upset (SEU) than a high-density cell [8]. [9,10] have studied how device dimensions and the technology node impact FinFET SRAM cells' SER. It is concluded that a higher Fin height degrades the radiation robustness of the SRAM cell, while improving the static noise margin (SNM). Moreover, the SER is improved by more than 40% as the technology node scales from 20 nm to 7 nm.

In this study, we determine how front-end wearout mechanisms impact FinFET SRAM SER, while considering time-dependent degradation and process parameter variations, such as gate length variation. The FinFET SRAM cell is stressed and degraded by Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Random Telegraph Noise (RTN) [11–15]. The stress of a cell, which is a function of its activity (duty ratio and transition rate), is included in the analysis. The modelling methodology for SER is adopted from [6,7]. Since the stimulus particles considered in this study are at a relatively low energy level, we only consider single-bit upset (SBU), and don't need to model multiple-cell upset (MCU) [16].

The structure of this paper is as follows. Section 2 describes the modelling methodology and the wearout mechanisms in a 6-T SRAM cell. Section 3 presents the simulation results and analysis for the impact of various factors, including process parameters, stress time, and cell activity. Section 4 concludes this paper.

2. Modelling methodology and the wearout mechanisms of a FinFET SRAM cell

2.1. Modelling methodology

The SBU and SER of FinFET SRAM cells can be evaluated through simulations with TACD tools and fast-SPICE. In TCAD simulations, the 3-D structure of a FinFET SRAM cell is constructed with Sentaurus Structure Editor (SDE) [17]. Then the Sentaurus Device Tool is applied to simulate the transient response of the SRAM cell due to the strike of heavy ions. The radiation settings, such as ion range depth and the profile lateral radius, are adjusted to match the case to be studied. The calculations are implemented with numerical simulations.

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TCAD tools can ensure high accuracy by emulating the physical process in semiconductor devices under radiation, at the cost of substantial computational cost. Due to the computational requirements of TCAD tools, we have adopted SPICE simulations for SER evaluation, which provide a faster speed. Although the SPICE simulation result can't provide a 100% match with the TCAD output, it enables us to study the impact of front-end wearout mechanisms on the FinFET SRAM soft error rate to extract a correct trend. In SPICE simulations, the effect of particles is incorporated with a current model. Several current models (Double Exponential model, Diffusion model, Roche model, and Freeman model) have been proposed to characterize the critical charge [18–22]. We use the Double Exponential model as follows

$$I(t) = \frac{Q}{\tau_2 - \tau_1}\left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}\right) \quad (1)$$

where Q is the amount of charge collected by a cell, which varies with radiation intensity. τ_1 and τ_2 are rise and fall timing constants, respectively. τ_1 and τ_2 are set to 2 ps and 20 ps to match the current waveform used for soft error evaluation of advanced devices.

To calculate the SER of an SRAM cell under specific configurations, the critical charge (Q_{crit}) needs to be determined with a Trial-and-Error technique. Q_{crit} is defined as the minimum Q with which the current pulse can flip the stored data of an SRAM cell. We swept Q from 0 to 5 fC to obtain the Q_{crit} when the state flips. The most efficient charge collection region exists in the vicinity of the reverse-biased junctions (off-nFET) in an SRAM cell.

Fig. 1 shows the 6 T SRAM cell with the off-nFET strike model. The data stored in this cell is 1. If the data is 0, the off-nFET strike model is assigned to the node QB. Since the SRAM cell can store either 1 or 0, we simulated the Q_{crit} for both cases and then adopted the smaller one as the final critical charge.

The probability of a bit upset also depends on charge collection efficiency which is [7]

$$\eta = LET \bullet T_{fin} \quad (2)$$

where *LET* is the linear energy transfer value, and T_{fin} is the thickness of a fin. Although there is a higher *LET* for extreme radiation conditions, since this paper focuses on the impact of front-end wearout mechanisms on FinFET SRAM SER, we adopt a medium *LET* of 150 fC/μm at ground level for the general neutron impact [7].

Finally, the probability of a bit failure under FinFET technology is [7–9]

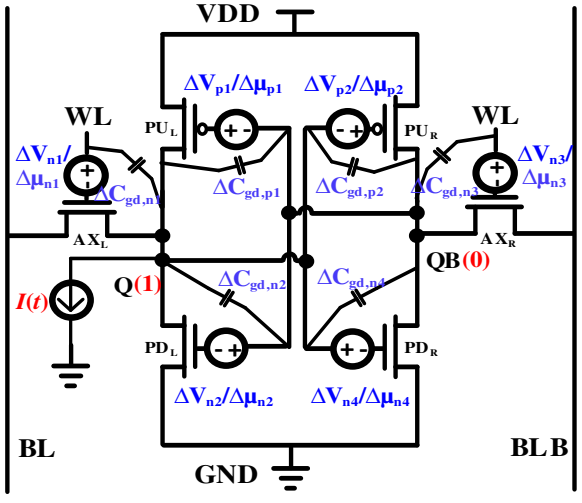

Fig. 1. 6 T SRAM cell with the off-nFET strike model (current source) and degradation parameters marked.

$$SER = k \bullet A_{diff} \bullet \exp\left(\frac{-Q_{crit}}{\eta}\right)[upsets/s] \quad (3)$$

where k is the particle flux, and A_{diff} is the sensitive diffusion area.

2.2. Wearout mechanisms in a FinFET SRAM cell

Our work considers Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Random Telegraph Noise (RTN). In our simulations, only pFET BTI (NBTI) is included [23,24]. The effect of HCI is considered for both pFET and nFET devices, while the HCI in pFETs is set as three times larger than that in nFETs for the same stress conditions [25]. Finally, RTN exists in both pFETs and nFETs.

Our models begin by considering the impact of wearout on interface traps (ΔN_{IT}) and the pre-existing (ΔN_{HT}) and generated (ΔN_{OT}) traps in the bulk, and then converts these trap densities into shifts in device parameters.

NBTI is modeled with three uncorrelated parts, which are interface traps (ΔN_{IT}) and the pre-existing (ΔN_{HT}) and generated (ΔN_{OT}) traps in the bulk [26]. These parameters shift as a function of time under stress and recovery. For NBTI, the time range and the ratios of stress and recovery are quite important for suitable prediction of degradation. There is a complete solution of stress and recovery for each stress and recovery time period, and a simplified solution for long time DC stress [27]. Considering the wide range of time in this work, we combine the long-term DC stress model with a duty factor equation to calculate the overall NBTI degradation. Specifically, we adopt a simplified expression of the recovery fraction in [27] due to the lack of experimental data for the impact of frequency, temperature, and stress voltage. With this method, we incorporate the effect of stress and recovery cycles using the duty ratio (DR).

HCI occurs when there are highly energized (hot) carriers that can flow from drain to source. In an SRAM cell structure, HCI happens when a transistor is on and is conducting current. Therefore, for the inverter structure studied here, HCI happens when the stored data is being flipped. Therefore, HCI in an SRAM cell is decided by the transition rate (TR) of the data stored. The interface trap degradation due to HCI during the time under stress varies with a FinFETs' dimensions, stress voltage, and temperature [28,29]. HCI is modeled with a shift in interface charge (ΔN_{IT}). This shift is not recoverable [30]. The equivalent time gap is applied to simulate the transition of each data flip in an SRAM cell.

For an inverter, HCI happens when there is state transition for the input and output (if the input transits from GND to VDD, the output transits from VDD to GND). During transition, the stress voltages at the gate and the drain are not constant. Thus HCI degradation can't be directly calculated with the analytical equation in Fig. 2. An equivalent time gap under the stress condition of V_{GS} = VDD and V_{DS} = VDD

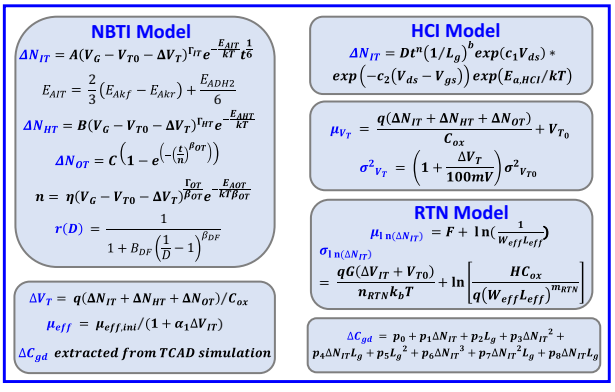

Fig. 2. The analytical expressions for the models of NBTI, HCI, and RTN [26–32].

during each transition is calibrated to simulate the HCI degradation. The overall stress time for HCI is the product of the equivalent time gap, transition rate, and the total stress time.

RTN is affected by device dimensions, temperature, and the interface charge density [31,32]. RTN introduces additional variation in the interface trap density (ΔN_{IT}). However, since the fluctuation is temporary, it doesn't affect the accumulated ΔN_{IT} induced by either NBTI or HCI. ΔN_{IT} induced by RTN is modeled as a lognormal distribution. The mean and standard deviation of the ΔN_{IT} distribution from RTN is added to the Normal distribution of ΔN_{IT} due to NBTI and HCI.

NBTI and HCI bring about the shift of charge density in transistors which further leads to the shift of threshold voltage, carrier mobility, subthreshold slope (SS), and the gate-drain capacitance [33]. It is verified in [33] that performance evaluation considering solely the impact on V_T results in over optimistic conclusions. To obtain convincing and persuasive results, it is necessary to include the impact on all device parameters.

Random process parameters cause time-zero variability in the threshold voltage. The overall shift of the threshold voltage due to NBTI and HCI is modeled as a normal distribution [34] and is added to the time-zero variability in the threshold voltage. The threshold voltage shift caused by RTN is obtained from a lognormal distribution. The overall threshold voltage shift distribution is the sum of the normal distribution and the lognormal distribution.

The other device parameters are taken as functions of the trap density shift due to NBTI and HCI. The relationship between the interface trap density and the effective carrier mobility is described with a linear equation. The deviation of the gate-drain capacitance due to wearout is extracted with TCAD simulation and fit with an empirical equation. We have checked that the SS of the devices in the library that we used has a negligible sensitivity to wearout mechanisms. Therefore, SS is not included in our simulations.

As shown in Fig. 1, NBTI affects ΔV_{p1}, $\Delta \mu_{p1}$, $\Delta C_{gd,p1}$, ΔV_{p2}, $\Delta \mu_{p2}$, and $\Delta C_{gd,p2}$. HCI affects ΔV, $\Delta \mu$, and ΔC_{gd} of each FET. RTN affects ΔV of each FET.

The analytical expressions for the NBTI, HCI, and RTN models are listed in Fig. 2. The NBTI and HCI models are calibrated with the assumptions that $\Delta V_{T,DC,Mean}$ is 100 mV after 10 years DC stress. The trap density shifts due to NBTI and HCI are calculated through the expressions in Fig. 2 by taking into account the specific stress conditions of each transistor in the SRAM cell, such as the stress voltage, circuit temperature, the cell's duty cycle and the cell's transition rate.

3. Simulation results and analysis

First, the impact of parameters, such as gate length (L_G) and temperature (Temp), on SER is discussed. The device degradation is considered as the first step. Then, the impact of wearout mechanisms and activity on SER is analyzed. Second, the effects of duty cycle and transition rate on the shift of the Q_{crit} and SER distributions are discussed.

3.1. Impact of parameters on SER

Before considering device degradation, we checked gate length and temperature affect Q_{crit} and SER. We consider the case where the gate length varies from 14 nm to 18 nm with a step size of 1 nm. The threshold voltage of each device is an independent Gaussian distribution with a mean of zero and a standard variation of 5% of the nominal value of the threshold voltage. The devices' carrier mobility and gate-drain capacitance vary accordingly as described in Fig. 2. The temperature is assumed to be a constant of 345 K.

Fig. 3 shows that a larger gate length results in a larger Q_{crit} and lower SER distributions which means that the FinFET SRAM has an obviously better resistance to radiation. This is because a larger gate length improves the device's capability to resist a content flip. Because

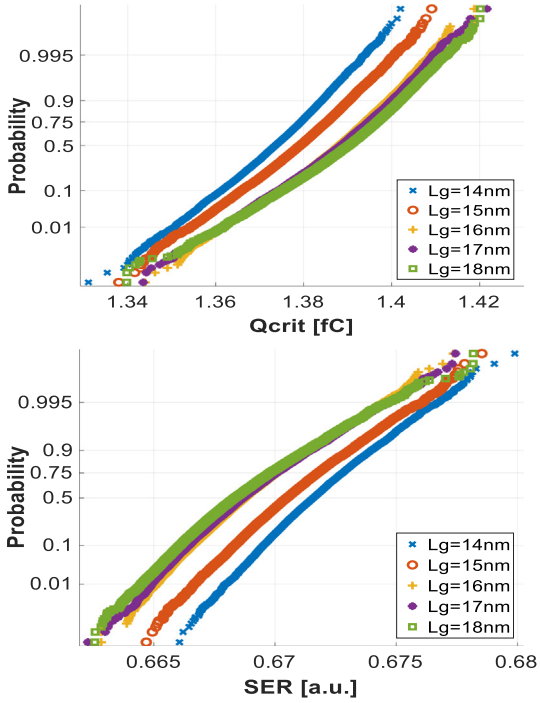

Fig. 3. The impact of gate length on Q_{crit} and SER.

of the existence of various variations, Q_{crit} and SER are distributions for each specific gate length. The impact of gate length on absolute value of SER is not very large, as shown in Fig. 3. It is because the expression for SER described by Eq. (3) incorporates the deviation of critical charge as an exponential function of $-Q_{crit}/\eta$, and η is adopted as 150 fC/μm for a serious radiation environment. If the circuits are radiated in a mild environment (for example η = 50 fC/μm), the impact on SER will be more obvious. If we see the impact of gate length on Q_{crit} in Fig. 3, the result indicates a larger impact. When the temperature varies from 66 °C to 74 °C, the gate length variation of each device is set as a Gaussian distribution with a mean of 16 nm and a standard variation of 5% of the nominal value.

The impact of other parameters, such as fin height on SER, is investigated in [9]. It is concluded that increases in the fin height of FinFET transistors degrades the radiation robustness of the SRAM cell, and at the same time the Static Noise Margin of the SRAM cell gets worse. This means the optimum device dimensions depend on the SRAM applications. Here, we studied the impact of gate length on SER as an example. We can also study the impact of other dimension parameters, such as fin height and width, with the same modelling methodology. Since the impact of fin height on SER has been studied in the [9] and the fin width is considered as a constant for FinFET technology, the related simulations are not incorporated here.

As shown in Fig. 4, higher temperature also leads to better reliability in the presence of soft errors. It should be noted that this conclusion is obtained based on the assumption that the temperature dependent charge collection efficiency is neglected. When the temperature dependent charge collection efficiency is included, SER could increase or decrease with temperature [35]. Currently, since there isn't an analytical expression for the temperature dependent charge collection efficiency, this phenomenon is not considered in our study. It can be incorporated easily when the temperature dependence is available.

3.2. Impact of wearout mechanisms and activity on SER

In this part, the temperature is constant at 345 K, and the gate length variation of each device is set as a Gaussian distribution with a

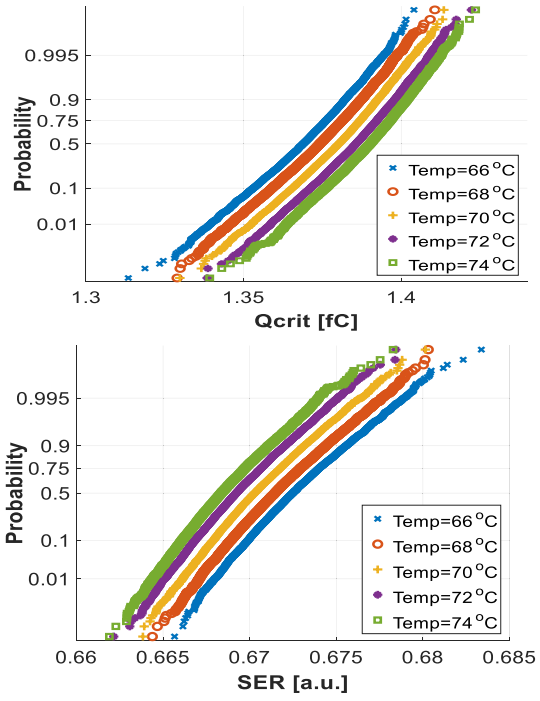

Fig. 4. The impact of temperature on Q_{crit} and SER.

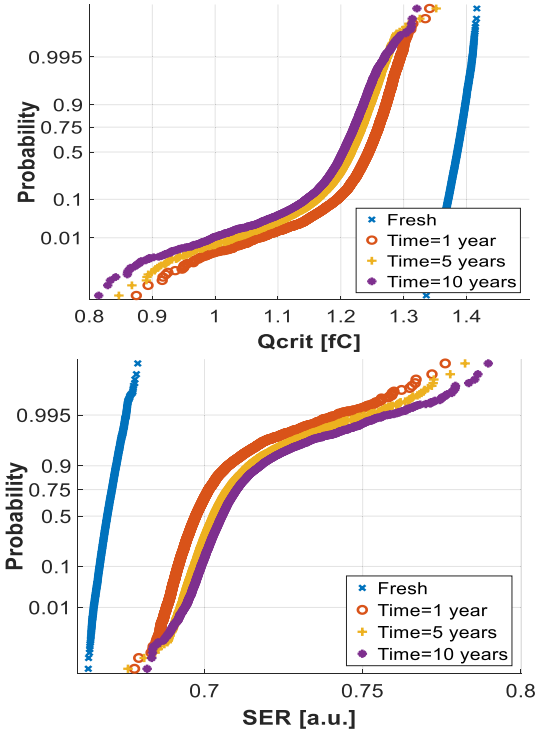

Fig. 5. The time-dependent shift of Q_{crit} and SER. The duty ratio is adopted as 30%, and transition rate is set with 20 time/μs.

mean of 16 nm and a standard variation of 5% of the nominal value. The other device parameters related to degradation are assigned as discussed in Section 2.

Fig. 5 shows the time-dependent shift of the Q_{crit} and SER distributions. The duty cycle ratio (DR) is adopted as 30%, and the transition rate is set as 20 transitions/μs. As time evolves, Q_{crit} gets smaller, SER gets higher, and circuit reliability degrades. Since the standard deviation of variations due to NBTI, HCI, and RTN increases with stress

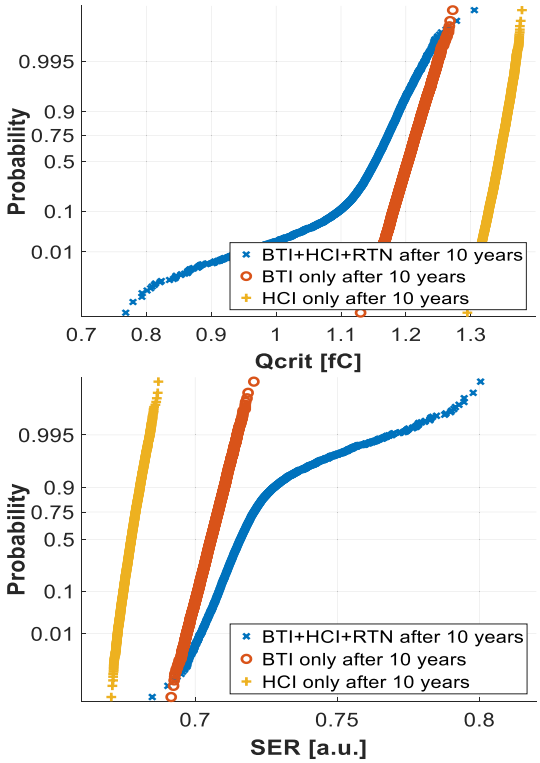

Fig. 6. The wearout mechanism-dependent shift of Q_{crit} and SER after a stress time of 10 years. The duty ratio is adopted as 10%, and transition rate is set as 20 transitions/μs.

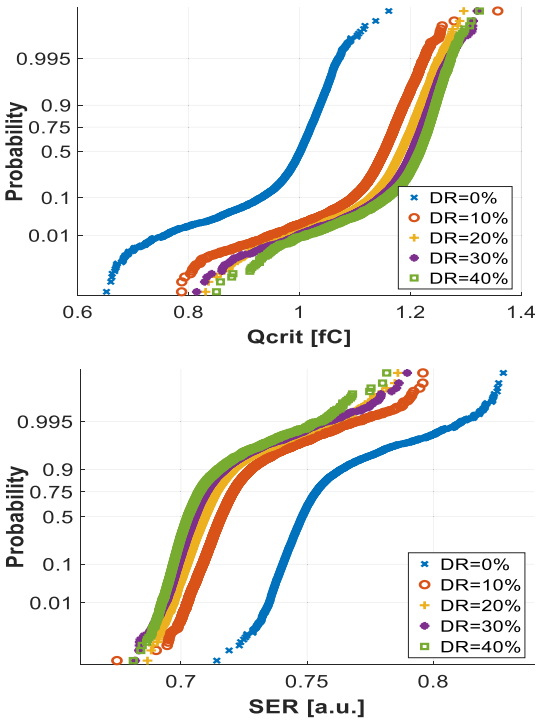

Fig. 7. The impact of duty cycle on Q_{crit} and SER. The transition rate is set with 20 transactions/μs.

time, the range of the Q_{crit} and SER distributions becomes wider and the distribution becomes more non-normal than when the devices are fresh.

Fig. 6 shows the impact of wearout mechanisms on Q_{crit} and SER, after a stress time of 10 years. It is found that BTI is more important

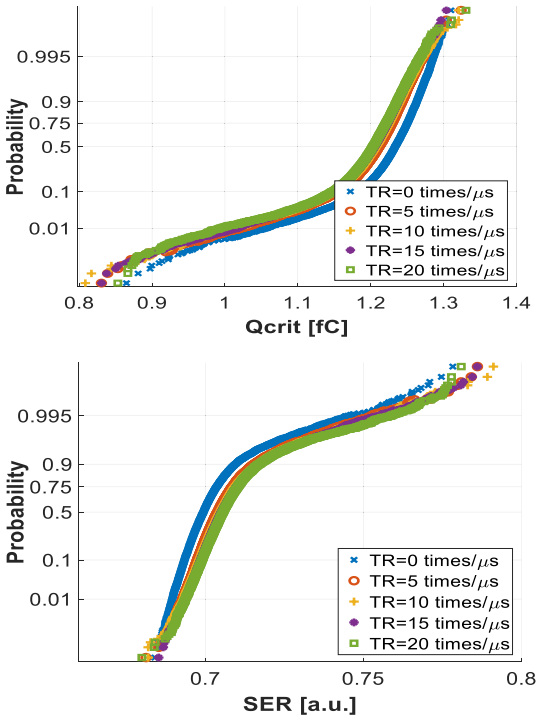

Fig. 8. The impact of transition rate on Q_{crit} and SER. The duty ratio is set as 30%.

than HCI for Q_{crit} and SER. The reason is that BTI causes more trap density accumulation than HCI in the specific case here. Meanwhile, since RTN is affiliated with the occurrence of BTI and HCI, its impact is not plotted separately. RTN introduces a long tail on the distribution of Q_{crit} and SER. It's necessary to take all of these wearout mechanisms into consideration simultaneously for SER modelling.

Figs. 7 and 8 show the impact of duty cycle (DR) and transition rate on Q_{crit} and SER, after a stress time of 10 years. The DR effect is symmetric between 0% and 100% with a centre of 50%. Thus we only show the impact of DR for half of its range. It is found that within the range between 0% and 50%, a lower DR leads to worse reliability, which is because a higher DR in this range relates to more NBTI recovery. The gradient of Q_{crit} and SER with respect to DR is greater when DR is closer to 0%. A higher transition rate (TR) causes worse reliability, which is intuitively explained because more transitions result in more device degradation due to HCI. Variation due to TR is smaller than variation due to DR, because has a greater impact on cell performance than HCI.

In this paper, we have studied the impact of front-end wearout mechanisms on FinFET SRAM cells' soft error rate. It has various potential applications for the design of reliable SRAM. For example, we can first model the overall SER of SRAM cache from the SER of each cell, given a distribution of duty cycle and transition rate among cells, defined by the application. We could study how different cache configurations impact its performance (such as hit rates) and SER. Based on a comprehensive analysis of performance and SER, we could optimize the cache design for a target environment. Moreover, we can study how error correcting codes (ECCs) impact SRAM SER, and then find a suitable type of ECC for a SRAM with specific target on SER.

4. Conclusion

The impact of process and wearout parameters on critical charge and soft error rate is studied for FinFET SRAM cells while considering various causes of variation. It is found that a larger gate length and higher temperature results in better resistance to radiation. The time-dependent Q_{crit} and SER of cells under specific stress conditions are displayed. Within its range between 0% and 50%, a lower DR leads to worse reliability, and a higher TR also causes worse reliability.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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