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ABSTRACT

Tellurene—the 2D form of elemental tellurium—provides an attractive alternative to conventional 2D semiconductors due to its high bipolar mobilities, facile solution processing, and the possibility of dopant intercalation into its 1D van der Waals lattice. Here, we study the microscopic origin of transport anisotropy in lithographically defined four-terminal tellurene devices using spatially resolved near-field scanning microwave microscopy (SMM). Our conductivity- and carrier type-sensitive SMM imaging reveals that the overall p-type transport measured between adjacent and opposite terminals originates from strong p-type character at the device edges. Despite using an atomic layer deposition-grown conformal overcoat that n-dopes the device interior, we observe only weak n-type transport along the main device channel at positive backgate voltages. This weak n-type transport along the device channel is shown to arise from local p-doping within a few micrometers of the electrodes, which produces a transport barrier from the n-type interior to the electrodes. These results reveal how the backgate-dependent conduction anisotropy could be leveraged to weigh different inputs for non-von Neumann architectures.

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Semiconducting low-dimensional van der Waals (vdW) materials have been widely studied as alternatives to traditional bulk materials for electronic and optoelectronic devices due to advantages offered by their reduced dimensionality and chemically inert interfaces.[1] While conventional applications of this class of materials face ongoing challenges in wafer-scale processing[2] and high defect densities,[3] applications for novel device architectures and non-von Neumann computing remain attractive.[4] In particular, owing to phenomena such as phase transitions,[5] thickness-dependent magnetism,[6] and chemical intercalation,[7] applications ranging from energy storage to neuromorphic architectures have been explored.[8,9]

Thus far, the dominant paradigm on 2D layered semiconductors has emphasized the transition metal dichalcogenides and black phosphorous. Although comparably few 1D vdW materials exist,[10,11] elemental tellurium provides an attractive alternative to existing layered systems.[12,13] Tellurium is composed of 1D helical molecular chains aligned along a single direction (c-axis) and held together by vdW forces. Nanometer thin sheets of tellurium—termed tellurene—can be solution processed[13] and exhibit long-term physical and electronic stabilities, even under ambient conditions.[14] Tellurene is generally observed to be a p-type semiconductor[12,13,15,16] with a thickness-dependent bandgap of $\approx 0.4\,\mathrm{eV}$[17] although it can be n-doped using a conformal atomic layer deposition (ALD)-grown Al_2O_3 overcoat.[18] The narrow bandgap, together with bipolar mobilities as high as $\mu_h \approx \mu_e \approx 700\,\mathrm{cm^2/V \cdot s}$, readily enables switchable bipolar transport[19] as desired for ambipolar field effect transistors (FETs).[20] In previous work, we revealed strong variations in the conductivity and carrier type across tellurene FETs.[19]

In this work, we study the transport anisotropy in four-terminal tellurene devices. We use near-field scanning microwave microscopy[21] (SMM, often called scanning microwave impedance microscopy, sMIM) to image spatial variations in both conductivity and carrier type in these devices. We find strong p-type character along all edges of the device, which provides the conduction pathway for the predominant p-type transport observed between adjacent and opposite electrodes. Our SMM imaging reveals that despite the strong n-type character in the device interior at positive backgate voltages, corresponding n-type transport is only observed

along the main device channel due to a lack of transport channels to the electrodes.

The four-terminal tellurene devices were fabricated as described previously.[13,18] Briefly, the tellurene films are grown by a solution-based process using face-blocking ligands to direct vdW self-assembly into 2D films.[13] Films are deposited onto Si substrates with 90 nm thermally grown oxide, and Cr/Au electrodes are subsequently fabricated using electron beam lithography. We then apply a 10-nm-thick conformal coating of Al_2O_3 using ALD to prevent electrical discharge from the tip to the device and to enable bipolar transport through n-doping.[18,19] Finally, the four-terminal geometry is defined using BCl_3/Ar plasma etching. Shown in Fig. 1(a) is an optical image of a representative device. The outline of the tellurene flake prior to etching is shown by dashed lines, with the 1D tellurium chains and c-axis aligned along the flake long axis as previously determined by Raman[22] and structural analysis.[13] Terminals are numerically labeled, and all are kept at 0 V/ground except during transport measurements. Device transport characteristics are measured by applying a voltage to either terminal 1 or 2 and measuring the drain current at terminals 3 and 4 simultaneously.

Shown in Fig. 1(b) is an illustration of the experiment. SMM is a scanning probe-based technique that can directly interact with free carriers in a sample of interest at GHz frequencies.[19,21,23,24] The SMM

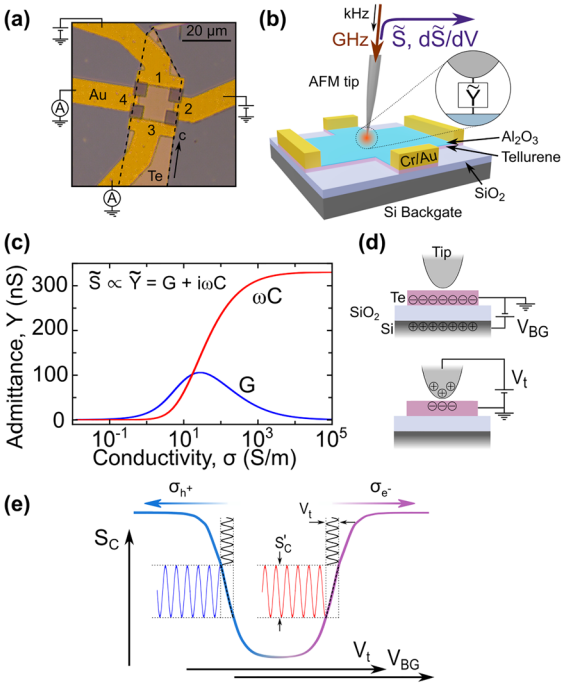

FIG. 1. (a) Optical micrograph of the tellurene device studied. (b) Illustration of the experimental setup using AFM-based microwave near-field microscopy to study conductivity variations in four-terminal tellurene devices. (c) Finite element modeling of the complex-valued tip-sample admittance as a function of tellurene conductivity. (d) Schematic illustration of the global electrostatic gating due to the backgate voltage V_{BG} and the local gating due to the tip voltage V_t. (e) Schematic evolution of the S_C signal with applied gate voltage in the electron- and hole-transport regimes. Here, V_{bg} is used to control the global device characteristics, while V_{tip} is used to interrogate the local carrier type via the corresponding bias-dependent slope.

is based on a modified atomic force microscope (AFM, Agilent/Keysight; mention of commercial products is for informational purposes only and does not imply NIST's recommendation or endorsement) operating under ambient conditions in contact mode with Pt tips (25Pt300A, Rocky Mountain Nanotechnology). The single-frequency microwave signal at 17.3 GHz is sourced from a vector network analyzer and directed to the tip. The signal $\tilde{S}$ reflected from the tip-sample junction depends on the complex-valued tip-sample admittance $\tilde{S} \propto \tilde{Y} = G + i\omega C$, with G being the conductance, C the capacitance, and ω the operating frequency. We detect the reflected signal using an IQ mixer[19] to yield the in-phase and out-of-phase components of the complex-valued signal $\tilde{S} = S_G + iS_C \propto G + i\omega C$. We also use a bias tee to superimpose a low-frequency (50 kHz) AC voltage at the tip with a peak-to-peak amplitude of $V_t = 1$ V. Lock-in detection on S_C then yields the differential signal $S'_C \equiv dC/dV_t$.[19,25,26]

Shown in the inset of Fig. 1(c) is the modeled tip-sample admittance as a function of sample conductivity.[24] The measured SMM signal $\tilde{S} \propto \tilde{Y}$ is, thus, directly sensitive to the sample conductivity, and since $S_C \propto C$ increases monotonically with sample conductivity, we use that channel exclusively in this work. As illustrated in Fig. 1(d), we use V_{BG} applied to the global Si backgate to control the carrier density, while V_t serves as a local tip-gate. S_C is then sensitive to the distinct V_{BG}-controlled electron- and hole-transport regimes as schematically shown in Fig. 1(e). Also illustrated in Fig. 1(e) is how the global carrier density and type can be locally modulated by V_t. The slope-sensitive S'_C measurements, thus, interrogate the local carrier type, where the phase of the detected signal directly reflects the local carrier type via the sign of the lock-in signal.[19] S'_C measures the high-frequency branch of the capacitance-voltage curve,[27] and so the signal vanishes at high carrier densities as well as near carrier neutrality.

We begin by examining the V_{BG}-dependent spatial evolution of the conductivity in a multi-terminal tellurene device. All measurement sequences were performed in a systematic manner for reproducibility and in order to mitigate the hysteretic effects in transport and SMM imaging. After initially setting V_{BG} to the largest positive value used and allowing the device to settle for $\approx$ 5 min, we acquired an SMM image ($\approx$ 6 min/scan) followed by a current-voltage (IV) sweep before lowering V_{BG} to the next value in the sequence.

Shown in Fig. 2(a) is the AFM topography of a four-terminal device. The device is $\approx$ 50 nm thick with a 10-nm-thick Al_2O_3 overcoat. Large pieces of debris are seen on the surface, which are the result of hardened etching resist that is then moved/cleaned by repeated AFM scanning. Shown in Figs. 2(b) and 2(c) are a sequence of S_C and S'_C images, respectively, shown in chronological order and acquired with applied backgate voltage as indicated (see the supplementary material for the full dataset as well as the simultaneously acquired S_G and S'_G channels). Based on the S_C images, we see that at large positive backgate voltages, the conductivity within the flake interior is higher, which we can assign to n-type conductivity based on the S'_C images. However, there nevertheless appears to be discernible p-type conductivity at the device edges. As the backgate voltage is decreased, we see that the n-type conductivity in the device interior decreases and the p-type conductivity at the device edge increases and becomes wider. Around $V_{BG} = 0$ V, we see that the conductivity within the device interior reaches a minimum, corresponding to local charge neutrality as the conductivity switches from n-type to p-type. As V_{BG} is further decreased, we see p-type conductivity throughout the device although

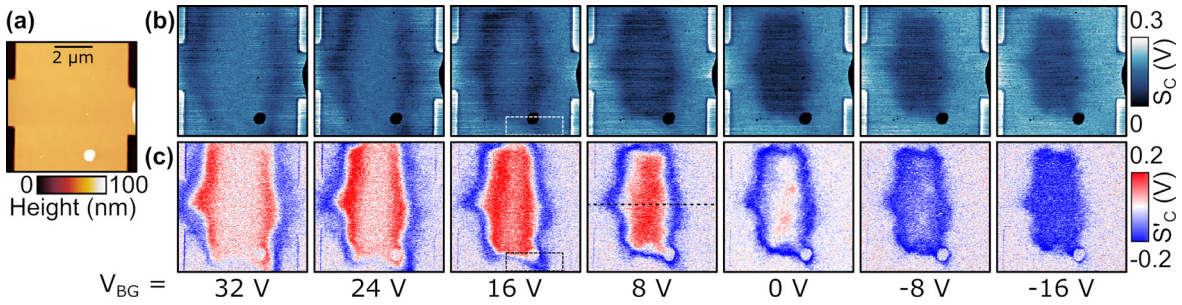

FIG. 2. (a) AFM topography of a four-terminal tellurene device. A sequence of S_C (b) and S'_C (c) images acquired at backgate voltages as indicated.

the edges remain more conductive than the interior. As expected, the S'_C contrast vanishes (white regions) at high and low carrier densities as seen at the device edges at negative values of V_{BG} and the low-conductivity regions marking the spatial p-type to n-type boundaries.

The V_{BG}-dependent spatial conductivity and carrier-type distribution reflect previous results on two-terminal devices.[19] These devices are characterized by an interior region that can readily be switched between n-type and p-type conductivities and edges that appear to remain p-type throughout the full range of applied values of V_{BG}. We also note that throughout the devices studied here, the exposed edges perpendicular to the tellurene molecular orientation (c-axis) do not appear significantly different from the molecule-parallel edges (a-axis, see the supplementary material). While this is surprising considering the strong structural anisotropy of tellurene, both experimental[15] and theoretical work[28,29] suggests only a weak transport anisotropy.

In order to address the interplay between spatial inhomogeneity in conductivity and carrier type and the device characteristics, we examine the IV sweeps acquired after each SMM image during measurement sequences. Shown in Fig. 3(a) are a set of IV sweeps taken between terminals 2 and 3 (I_{32}) at values of V_{BG} indicated. Shown in the inset is the schematic arrangement of the terminal numbering. These IV sweeps show a linear relationship over the voltage range measured, suggesting near-Ohmic behavior. A clear p-type behavior is further seen in these sweeps as evidenced by the increase in I_{32} with decreasing V_{BG}.

Shown in Fig. 3(b) are I_{32} and I_{41} as a function of V_{BG} extracted from a full set of IV sweeps at values of $V_{sd} = \pm 0.1$ V. These measurements show the clear p-type character observed throughout all measurements between adjacent terminals. This transport is as expected given the presence of a well-defined p-type channel along the device edge. We also note that I_{32} is larger than I_{41} for all values of V_{BG}. This could be because the p-type edge that serves as the conduction channel for I_{32} is notably larger than the I_{41} conduction channel although this can also be influenced by

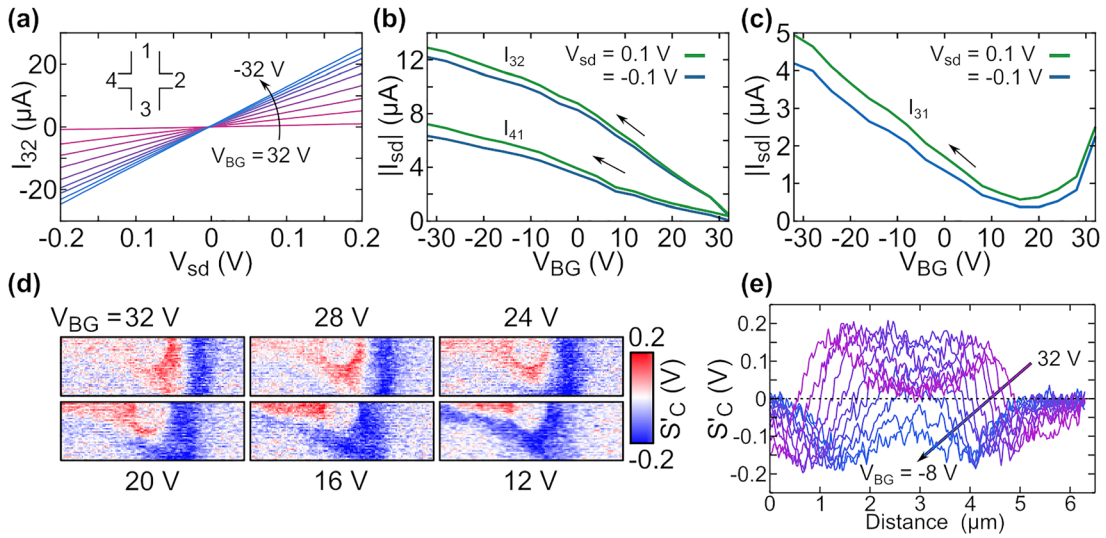

FIG. 3. A sequence of IV sweeps between terminals 3 and 2, I_{32} (a), with the terminal numbering indicated in the inset. I_{41} and I_{32} as a function of V_{BG} are shown in (b), extracted at $V_{sd} = \pm 0.1$ V from a full set of sweeps. The corresponding V_{BG}-dependent I_{31} plot is shown in (c), exhibiting a conduction minimum around $V_{BG} \approx 20$ V. Shown in (d) are zoomed images of the region enclosed by dashed lines in Figs. 2(b) and 2(c) at values of V_{BG} as indicated. The line cuts shown in (e) are taken along the dashed lines in Fig. 2(c) at 4 V increments showing the movement of the boundary (zero-crossing) between the p-type (negative values) and n-type (positive values) regions.

current to other electrodes. We note that I_{42} also exhibits clear p-type behavior (see the supplementary material) although the measured current is an order of magnitude smaller than I_{41}.

The p-type transport seen along the device edges differs from the behavior seen along the main axis of the device. Shown in Fig. 3(c) is I_{31} as a function of V_{BG}, acquired concurrently with I_{41}. Here, we see bipolar transport, with n-type behavior at large positive values of V_{BG} that transitions to p-type behavior as V_{BG} is decreased, and a conductivity minimum at $V_{BG} \approx 20$ V. Similar to our previous work,[19] the spatial conductivity and carrier type distribution in Fig. 2 near the conductivity minimum correspond to a coexistence of p-type edges and n-type interior.

In Fig. 3(d), we focus on the region near the bottom contact enclosed by dashed lines in Figs. 2(b) and 2(c) for values of V_{BG} in the vicinity of the conductivity minimum. These images illustrate the presence of a pinch-off point for n-type transport along the device axis, and the disappearance of the conduction channel from the electrode to the n-type interior agrees well with the disappearance of n-type transport at these values of V_{BG}.

Our measurements under ambient conditions preclude the observation of topological transport,[18] and the origin of the spatial variations in conductivity and carrier type seen here remains unclear. Tellurium generally exhibits p-type behavior,[13,15,16,22] and our n-type behavior originates from n-doping due to the ALD overcoat.[18,19] Our imaging here reveals that the resulting n-doping is spatially nonuniform and that edges retain their p-type character. We note that as-grown and full encapsulated edges studied previously[19] as well as the etched and ambient-exposed edges studied here remain p-type. We also note that fringing fields—which result in the field concentration and, thus, increased gating efficacy at the edges—cannot explain the observed behavior since the p-type edges persist at positive values of V_{BG} and also when the bias is turned off. While this behavior may arise due to strain,[19] we cannot rule out the effects of defect intercalation during growth or ALD deposition. The observed accumulation of hole charges on the edge could also be due to the Fermi level pinning effect. Like other well-explored semiconductor systems, Fermi level pinning in vdW materials is related to the atomic bond termination and interfacial chemistry and can have a complicated origin.[30]

Metal contacts can also induce electronic variations through local band bending that extends into a device channel.[31] In order to avoid damaging the tip by touching the metal contacts, we set the edge of our SMM imaging field of view to within a few 100 nm of the contacts. This mitigates the impacts of scan-to-scan drift while still allowing us to access electronic effects near the electrodes. Throughout our imaging, the interior regions of the device near the contacts at image bottom and top (terminals 1 and 3) appear to be more strongly p-type than the otherwise n-type interior. This is a common observation throughout our measurements (see the supplementary material for an additional device) and is likely due to spatially extended p-doping by the electrodes. Although our Cr-contacted electrodes were seen to result in downward band bending (n-type doping) in previous work for p-type tellurene,[32] it is unsurprising that the higher fermi level of our n-type material induces upward band bending (p-type doping). In addition to confirming the p-doping near the electrodes, our imaging also confirms that this effect is localized to within a few μm of the contacts and, therefore, does not explain the p-type edges observed in our devices.

Interestingly, unlike fixed p-n junctions that are defined by spatially fixed dopant distributions or material heterojunctions,[23] the boundary between our p-type and n-type regions remains fluid and translates laterally as the device is modulated. This is clearly seen in the sequence of line cuts shown in Fig. 3(e), which are taken at the location of the dashed line in Fig. 2(c). Here, the boundary between the n-type (positive values) and p-type (negative values) regions occurs at the zero-crossing (dashed line) and moves toward the device center as V_{BG} is decreased until the device transitions entirely to p-type. Our SMM imaging, thus, clearly shows that the spatial inhomogeneity in conductivity and carrier type can be controlled by gating, while the transport measurements reveal that this can be used to control the relative source-drain current between different terminals simultaneously. This suggests that the deliberate and targeted engineering of spatial inhomogeneity in carrier type and conductivity could lead to controlled and deterministic weighting of multiple inputs into the same device as we demonstrate for two terminals simultaneously.

Here, we have performed a systematic study correlating the backgate voltage-dependent transport in four-terminal tellurene devices with the spatial distribution of conductivity and carrier type. We find that all edges of the etch-defined tellurene device show strong p-type conductivity throughout the range of backgate voltages applied here, consistent with the p-type transport measured between adjacent terminals. In contrast, the device interior shows bipolar transport that can readily be switched between the n-type and the p-type. However, our spatially resolved imaging reveals that the overall weak n-type transport measured along the main device channel results from the absence of suitable n-type conduction pathways between the device interior and the electrodes. The spatially complex conductivity and carrier type distribution arise from the spatially inhomogeneous n-doping of the ALD overcoat together with local p-doping within a few micrometers of the Cr-contacted electrodes. Our results suggest that the spatial inhomogeneities in carrier type observed in tellurene devices that result in differing transport characteristics between different terminals simultaneously could be used for the weighting of different inputs for non-van Neumann architectures.

See the supplementary material for the full dataset for the scan sequence shown in Fig. 1, dataset for an additional device, comparison of the a-axis and c-axis terminated flake edges, and additional transport data.

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DATA AVAILABILITY

The data that support the findings of this study are available from the authors upon reasonable request.

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