A 7.4dBm EIRP, 20.2% DC-EIRP Efficiency 148 GHz Coupled Loop Oscillator with Multi-feed Antenna in 22nm FD-SOI

Muhammad Waleed Mansha, Mona Hella
Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute, USA
manshm@rpi.edu, hellam@rpi.edu

Abstract — This paper presents a 148 GHz coupled loop oscillator with multi-feed (MF) octagonal slot antenna. The MF antenna combines the output power from four single ended fundamental oscillators \((f_o)\) and back radiates the combined fundamental power through a silicon lens. The output power from each oscillator is ac coupled to the following stage using a phase compensation capacitor, whose value is selected to increase the oscillation frequency of the coupling loop network. The oscillator is fabricated in 22nm FD-SOI process and has a peak EIRP of 7.4 dBm and a corresponding DC-EIRP efficiency of 20.2%. To the best of the authors' knowledge, this offers an order of magnitude improvement in DC-EIRP efficiency among 100-200 GHz VCOs reported to date.

Keywords — on-chip antenna, CMOS, Millimeter wave integrated circuits, Silicon-on-insulator, voltage-controlled oscillators

I. INTRODUCTION

Efficient signal generation in the mm-wave frequency range continues to be a challenge for silicon based processes (CMOS/SiGe) despite recent advances producing transistors with \((f_t/f_{max})\) beyond 300 GHz. This is due to the limited breakdown and supply voltages of transistors and low quality factor of on-chip passives at such frequencies. Prior art on millimeter/sub-millimeter wave signal generation in silicon can be broadly categorized into: (1) \(N^{th}\) harmonic oscillators such as push-push, triple-push and quad push-topologies [1], [2], [3], (2) amplifier multiplier chains (AMC) [4], as well as fundamental oscillators with on-chip power combining or antenna arrays [5], [6], [7]. The different approaches present a compromise between output power, tuning range, chip area, layout complexity, and DC-RF efficiency.

In this paper, a coupled loop fundamental oscillator is proposed. As can be seen in Fig. 1, oscillation occurs at the frequency at which the overall phase contribution around the loop is \(2\pi\) or a multiple of \(2\pi\). For a symmetric design with four oscillators, there would be a phase difference of 90 degrees between adjacent oscillators. Existing approaches for coupled oscillator arrays would either utilize the coupling mechanism for the extraction of one of the harmonics, or use the ring or loop configuration, as shown in Fig. 1, to generate the signal at the fundamental frequency, which can be extracted from any point along the loop. Here, the power from each oscillator is efficiently combined and radiated through a single, multi-feed slot antenna. The output power from each oscillator is AC coupled to the source terminal of the transistor in the following oscillator stage. This allows the gate bias of each oscillator to be set independent of the supply voltage and can be optimized for maximum power and efficiency.

The circuit, implemented in 22nm FD-SOI (Fully Depleted Silicon-on-Insulator) technology has a measured peak EIRP of 7.4 dBm with a DC-EIRP efficiency of 20.2% from a 0.8 V DC supply.

II. CIRCUIT DESIGN

Fig. 1 shows the schematic of the proposed coupled loop oscillator. It consists of four single ended modified Colpitts oscillators connected in a loop/ring configuration. The transmission lines connecting the oscillators are utilized as matching/feeding networks to provide sufficiently high impedance to the output of each oscillator and route the bulk of the generated RF power to the antenna.

A. Single Ended VCO Core

The single ended VCO utilized in the loop is based on a common drain Colpitts topology. The conventional topology is modified to receive a coupling signal at the source terminal of the core transistor \(M_1\) coming from the output of a preceding oscillator stage. This is in contrast to prior art such as [8], in which the signal coming from the preceding stage is DC coupled to the gate terminal of the core transistor. This connection allows the gate bias of each oscillator to be set independent of the supply voltage and can thus be optimized for maximum output power and efficiency.

Fig. 2 shows the detailed schematic of the single ended VCO core. The inductance of the tank is implemented using a \(21\mu\)m length of coplanar waveguide (CPW) transmission line \(TL_1\). The parasitic capacitance of a 36 \(\mu\)m wide, 20 \(\mu\)m gate length NMOS transistor acts as the tank capacitance. The small inductance of the CPW transmission line and the absence of a fixed capacitor results in a high fundamental oscillation frequency. A single 100 ff varactor is connected to the source terminal of the transistor \(M_1\) for tuning the oscillator. The back gate bias of the core transistor provides a second tuning mechanism. A shorted shunt stub, implemented by \(TL_7\) provides a path for the DC bias current of the oscillator. It also acts as the input matching network and is designed to provide a small input impedance looking into the input coupling port of the oscillator.

A phase compensating capacitor is added to output of the oscillator. This capacitor serves a dual purpose. First, it allows AC coupling of the oscillator output, that enables the coupled
signal to be applied to the source terminal of the transistor. Second, the capacitor also reduces the phase contribution of each oscillator. This is due to the fact that the coupled loop oscillates at the frequency where the overall phase around the loop is $2\pi$, so the addition of the phase compensating capacitor increases the oscillation frequency of the loop. We define the phase compensation (PC) as the reduction in the phase contribution of each oscillator due to the addition of the compensating capacitance.

$$PC = |(\angle V_{IN} - \angle V_A) - (\angle V_{IN} - \angle V_{OUT})|$$  \hspace{1cm} (1)

Where $\angle V_{IN}$, $\angle V_{OUT}$ and $\angle V_A$ are the signal phases at the input, output, and node A of the core oscillator, as marked in Fig. 2. The capacitance value determines the phase compensation of each oscillator, and ultimately the increase in oscillation frequency. Fig. 3 shows the simulated phase compensation of each oscillator in the loop as a function of the phase compensating capacitance. Smaller values of phase compensating capacitance will yield higher improvement to the peak oscillation frequency. However, very small capacitors have a higher uncertainty associated with the modelling and would be relatively more affected by parasitics. As a trade-off, a 23 fF 4-layer MOM capacitor is utilized.

**B. Quad-feed Slot Antenna**

An octagonal slotted loop antenna divided into four sections is used in the design. The topology is chosen because of its wide bandwidth and feasibility for use with a silicon lens, due to its back-side radiation. Dividing the antenna layout into four sections improves the isolation between each signal feed. If each section of the antenna is excited with signals with the right phase difference, the radiated power will get added up in the far field without distorting the radiation pattern of the antenna. Thus the single antenna functions as both the power combiner and radiator, which reduces the chip area requirement compared to the conventional approach of using a separate antenna for each signal as described in [7] and [9].

The antenna is implemented on the second metal layer from the top with a loop diameter of 230 $\mu$m. A high resistivity (HR) hyper hemispherical silicon lens is employed to enhance the radiation efficiency. A plot of the simulated radiation efficiency of the antenna with and without the silicon lens is shown in Fig. 4. The plot also shows the structure of the proposed antenna, annotated with the input signal phase difference required at each port for power combining.
C. Power Feed Network

A buffer stage typically follows individual oscillators to reduce the loading effect, which could dampen the oscillations. However, the buffer stage would use a significant amount of power. To maximize the efficiency of the overall circuit, this work utilizes a passive power feeding network composed of transmission line sections to transform the small impedance of the antenna to a higher impedance for the oscillator output. The feed network must be designed in such a way that the bulk of the output power from the oscillator gets routed to the power combining and radiating multi-feed antenna while a small fraction of the power gets routed to the following oscillator stage such that the oscillator loop remains locked with the desired phase difference between the oscillators. This requires the co-design of the feed network, multi-feed antenna and the oscillator input coupling. Fig. 2 shows the schematic of the designed power feed network. Transmission lines forming the network are implemented using grounded coplanar waveguides whose structure is also shown in Fig. 2. The signal line of the CPW transmission line is implemented on the second metal layer from the top, which is the same metal layer used for the multi-feed antenna. A \( \lambda/4 \) CPW transforms the small input impedance of the oscillator input coupling port into a large impedance at the junction of TL8 and TL9. This allows most of the power flowing through TL8 to get routed towards TL9. The series transmission line section formed by TL8 and TL9 transforms the 7.5 \( \Omega \) impedance of the multi-feed antenna to a higher impedance limiting the loading of each oscillator stage. This power feed network design was done while maximizing the utilization of the series length of the transmission line needed to connect the output of each oscillator to the input coupling port of the following oscillator around the antenna.

III. MEASUREMENT SETUP AND RESULTS

The quad-coupled oscillator is fabricated in Global Foundries 22nm FD-SOI process and occupies a chip area of 920 \( \mu \text{m} \times 570 \mu \text{m} \). Fig. 5 shows the chip micrograph. For testing, the chip is mounted on a PCB with a central slot containing a tile of HR silicon. A non-metallic epoxy is used to attach the die to the silicon tile such that it does not impede the back-side radiation. Biasing connections were wire bonded from the chip to the PCB. A silicon lens is then attached to the back side of the silicon tile. The radiated signal from the chip is observed in the far field using a Virginia Diodes N9029AV05 140 GHz - 220 GHz Signal Analyzer Range Extender, connected to a Keysight N9030A PXA Spectrum Analyzer. The PCB was mounted on a swivel platform to measure the radiation pattern.

The voltage tuning characteristics of the oscillator are measured for back gate bias voltages from -0.5 V to +2.0 V. As shown in Fig. 7, the oscillation frequency range is from 146.7 GHz to 150 GHz. Fig. 8 shows the measured and normalized radiation pattern. The radiator has a high directivity in the desired broadside direction. The peak EIRP is measured for different supply voltages and the DC-EIRP efficiency is calculated from the observed DC power consumption. A plot of the measured peak EIRP and DC-EIRP efficiency is shown in Fig. 9. At the nominal supply voltage of 0.8 V, the chip draws only 34 mA to yield a peak EIRP of 7.4 dBm at a DC-EIRP efficiency of 20.2%. This efficiency is higher than that for prior reported VCOs with radiated output in...
the 100GHz - 200GHz frequency band. At an elevated supply voltage of 0.9 V, the peak EIRP improves to 8.1 dBm. Table I provides a comparison of this work to state of the art VCOs in the same frequency range.

IV. CONCLUSION
A fundamental coupled loop oscillator operating at 148 GHz is demonstrated in 22nm FD-SOI process. A Multi-feed octagonal slot antenna is presented as a more efficient alternative to dedicated on-chip power combining networks, when the output signal ultimately has to be radiated. A power feeding network is inserted between the oscillators within the loop, which provides the impedance transformation required to reduce the loading effect on the oscillators while also feeding the antenna ports. Measurement results show a peak EIRP of 7.4 dBm and a corresponding DC-EIRP efficiency of 20.2% at a 0.8 V supply.

ACKNOWLEDGMENT
The authors acknowledge the Global Foundries University Program for chip fabrication. The authors would also like to thank Jerry Dziuba for help with the testing setup.

REFERENCES


