Guidelines for Ferroelectric FET Reliability Optimization: Charge Matching

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***Abstract*- An optimization principle for ferroelectric FET (FeFET), centered around charge matching between the ferroelectric and its underlying semiconductor, is theoretically investigated. This letter shows that, by properly reducing the ferroelectric polarization charge and its background dielectric constant, charge matching can be improved to enable simultaneously: i) reduction of the interlayer and semiconductor electric fields during programming, reading, and retention, leading to prolonged endurance and retention; ii) improvement of the memory window; and iii) suppression of device-to-device variations by affording full polarization switching. Theseattributes provide anincentive for the presentation of the proposed guidelines for FeFET optimization as detailed in this letter.**

***Index Terms*- Ferroelectric, FeFET, reliability optimization, charge matching.**

I. INTRODUCTION

FERROELECTRIC memory has received a strong resurgence of interest since the discovery of scalable and CMOS-compatible ferroelectrics based on Hf(h . Excellent performance (e.g., more than 1V memory window for ~10nm thick HfO2, write time as short as lOns, and ultralow write energy on the order of lOfJ, etc.) has been demonstrated in advanced technology nodes [l], [2]. However, challenges in reliability remains a major roadblock for its adoption, such as charge trapping [3], [4], degraded endurance [5], and unacceptable variations upon scaling [2], [6]. Therefore, optimization of device reliability without degrading other performance metrics will be critical for its success.

We believe that many of the reliability issues are associated with the large charge mismatch between the ferroelectric layer and the semiconductor. With the typical polarization charge around $20\mu C/cm^2$ for HfO 2, compared with the corresponding charge on the silicon side (including the depletion charge and the channel inversion charge) of less than $2\mu C/cm^2$, there is a large charge mismatch between the two, as illustrated in Fig. 1 (a). This stresses the semiconductor and interlayer significantly during programming with $Va = +Vw/-Vw$, because a large polarization charge, $Pw+/Pw-$, has to be screened by the semiconductor. Hence, substantial charge trapping and defect generation are induced by the write pulses, degrading FeFET endurance [3]. The charge mismatch also forces the ferroelectric to work on non-saturated hysteresis loops [7]. It has been shown that partial polarization switching induces significant variations due to the stochasticity during domain switching [6]. Therefore, mitigating charge mismatch becomes critical for reliability improvement.

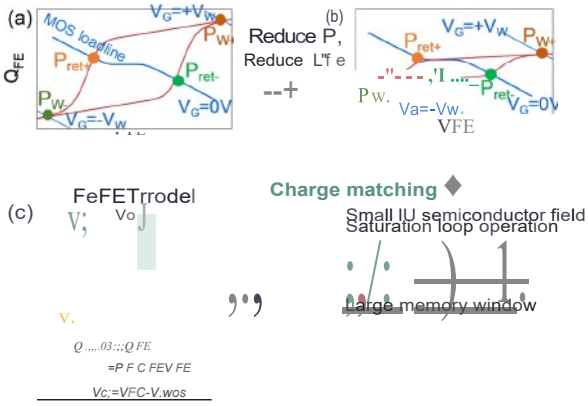

Fig. 1. Overview of charge mismatch between the ferroelectric and semiconductor, and the mitigation strategy. (a) For a normal Hf0 2-based FeFET withlargePr and eFE , the large polarization charge <Pw+ IPw_) during programming significantlystresses theinterlayer and semiconductor.Thebluelineis theMOS loadline and the red curveis the ferroelectric OrcE - VFE loop. (b) Reduced Pr andeFE limit the switched polarization charge, andenable fullpolarizationswitching withlessstress on the interlayer and semiconductor. (c) The model that is utilized to investigate the optimization guidelines of FeFET.

There have been several device designs that are targeted at addressing this charge mismatch, such as FeMFET (or MFMIS) structure [8]- [10]. In those devices, a metal-ferroelectric-metal (MFM) capacitor is integrated on top of the gate of a MOSFET. By scaling down the area of the MFM capacitor with respect to the MOSFET, the electric field in the **MOSFET** is reduced, and the ferroelectric can operate along the saturation loop. Challenges with this approach are the small area ratio (e.g., ~ 0.1) required, which limits the device scaling capability as well as retention degradation due to leakage current and depolarization field. Therefore, other approaches to improve charge matching without compromising performance are desirable.

In this work, we demonstrate an alternative approach for optimization, i.e., to reduce the ferroelectric polarization *(P,)* and its background dielectric constant (8FE) [11], [12],

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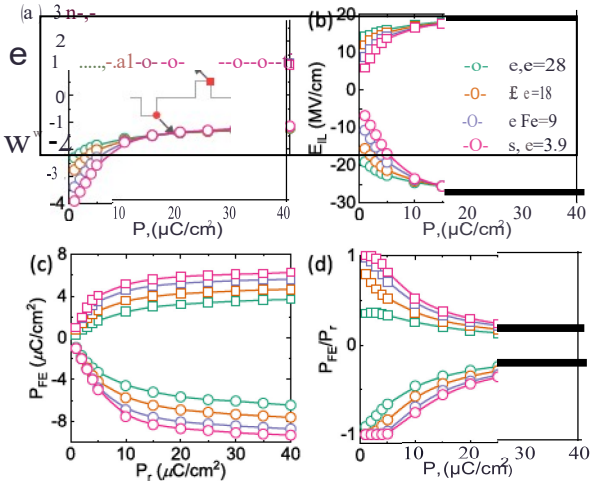


Fig. 2. Electric fields in (a) ferroelectrics (EFE), (b) inter1ayers (E|L), (c) abso lute PFE's, and (d) normalizedP FEIP r at the end of write pulse for 4 different dielectric constants. The square/circle symbol represents 1μs, + 4V/- 4V write pulse, respectively. All the line colors are consistent with (b).

as shown in Fig. 1 (b). In doing so, the amount of polarization that needs to be screened by the semiconductor is reduced , relieving the electrical stress in interlayer and semiconduc- tor during programming, and thus improving the endurance, as also proposed in [13]. Additionally, it also enables the fer- roelectric to operate along the saturation loop that minimizes the variation [6].

11. E VA L UAT ION A PPR OAC H

A recentl y developed model for FeFET [14] is utilized to theoretically study the optimization strategy. The ferroelectric is modeled as a lumped capacitor, which is connected with the gate of a MOSFET. The voltage division equation and charge

conservation equation are solved self-consistently to obtain the

FeFET characteristics, as shown in Fig. 1(c). The ferroelectric film is composed of multiple independent switching domains, where each domain can be in the up or down polarization state. A nucleation limited switching model is applied to describe the polarization switching dynamics [15]. With this model, the size scaling, inter-device variation, switching stochasticity, and polarization accumulation can be successfully captured.

III. RESULTS AND DISCUSSNS

Write pulses of ±4V, 1μs are applied to FeFETs with 8nm Hf(h as the ferroelectric and 1nm Si(h as the interlayer Theelectric fields in the ferroelectrics (£FE) and interlayers (£ IL) at the end of write pulses as functions of *P,* with four different e FE are shown in Figs. 2(a) and (b), respectively. At a given f:f E, the less the polarization charge that needs to be screened, the smaller the *EJL.* This is consistent with the charge conservation requirement (Fig. 1 (c)). A smaller *P,* improves the charge matching between the ferroelectric and the semiconductor, relieving the electrical stress on the interlayer and semiconductor. Moreover, additional drop in £IL can be achieved by lowering f:f E• For example, during the - 4V write pulse, £IL reduces merely 1.3x when *P,* shrinks from 20μC/cm^2 to 2μC/cm^2 for f:FE = 28; while reduces as much as 2 x for eFE = 9. Such decline in £IL is beneficial for endurance improvement, as it can reduce charge trapping and interface defect generation.

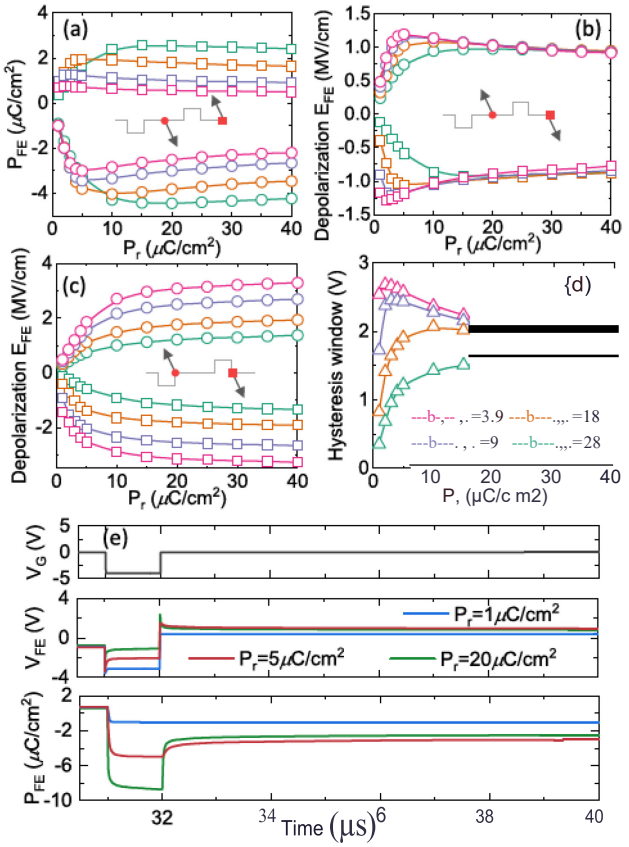
The boost of £FE is a direct consequence of the reduction in *EJL.* As such, the £FE increases by 1.7x when *P,* shrinks from 20μ C/cm^2 to 2μC/cm^2 for f:f E = 28, and grows by 2.5x for f:FE= 9. Note that this *EFE* increase should not degrade the endurance of the Hf(h -based FeFET (~ 10^5 cycles [1], [2]), as it is mainly limited by charge trapping [5]. This is further illustrated by the much higher end urance (> 10^8 cycles [16], [17]) in MFM capacitors cycled with similar £FE stress (£ FE ~ 3MV/cm). The absolute and nor- malized polarization charge (PFE) at the end of write pulses are shown in Figs. 2(c) and (d), respectively. The enhancement in switched PFE with *P,* becomes marginal when *P,* grows beyond 15μC/cm^2. This indicates that, for the optimization of FeFET, pursuing a high *P,* is the wrong direction because: (i) it will not improve the switched PFE, and even worse, (ii) it will increase the stress on the interlayer and semiconductor, degrad- ing its reliability. The normalized PFE indicates the portion of domains that participate in the switching process. Interestingly, it exhibits an opposite trend to the absolute PFE due to t h e sa turating behavior of PFE with respect to *P,*. For small *P,,* especially at small eFE, the *PFEI P,* is close to 1, indicating full polarization switching due to the charge matching. The benefit of full polarization switching in controlling the variation will be explained below.

When the applied gate pulse is turned off, some of the switched domains will flip back, relaxing the polarization. Fig. 3(a) shows that PFE during retention exhibits a peak at some intermediate *P,,* especially for small e FE. This is related to the depolarization field [18], shown in Eq. 1, that causes the polarization relaxation.

$$V_{FE,rel} = -\frac{C_{FE}}{C_{FE} + C_{1s}} P_{FE} \quad (1)$$

where VFE,ret is the voltage across the ferroelectric during retention, C1s is the series combination of the interlayer and the semiconductor capacitance. As shown in Fig. 3(c), the depolarization field at the initial relaxation moment strengthens with increasing *P,,* and get further enhanced for small E:fE , which is consiste nt with Eq. (1). For small *P,,* the depolarization field is sufficiently small such that PFE during retention follows the switched f'fE after the write pulse (Fig. 2(c)). However, for a large *P,,* the depolarization field is strong enough to cause significant polarization relaxation after the write pulse, causing the decline of f'fE- This is also illustrated in the transient waveform for a - 4V write pulse, shown in Fig. 3(e). At the moment when *Va* switches from - 4V to 0 V, the VFE,ret is greater for higher *P,,* causing more polarization relaxation. As a result, a nonmonotonic dependence is observed. Note that even after polarization relaxation, shown in Fig. 3(a), nearly full polarization switch- ing is observed for small *P,* and E:fE, suggesting its potential for suppressing inter-device variations.

According to Eq.(1), there is a tradeoffbetween the memory window and depolarization field, hence retention performance. The depolarization field during retention, shown in Fig. 3(b) follows a similar trend as the Fig. 3(a), due to Eq. (1).



F ig. 3. (a) P F E and (b) the depolarization field EFE during reten- tion; (c) The depolarization field l:fcE at the initial relaxation moment; (d) Memory windows of FeFET as functions of Pr for 4 different eFE; (e) transient waveforms showing polarization switching and relaxation during - 4V writepulse for 3 different Pr cases. The square/circle symbol in (a-c) represents 1μs,+4V/- 4V write pulse, respectively. Curvecolors are consistent with (d).

It suggests that even though the depolarization field at the initial relaxation moment (Fig. 3(c)) is much higher for a film with a smaller eFE, it does not hold for the depolarizationfield during retention. This is because PFe during retention is also reduced for small E:fE, thus rendering similar depolarizatio n field during retention, irrespective of the E:fE. For example, for a eFE of 9, the *EFE* during retention increases approximately only 30% when *Pr* reduces from 25μC/cm^2 to 5μC/cm^2 (the peak of the curve). It is also possible to maintain the same depolarization field as the existing HfO2 FeFET (*Pr* of 20 μ C/cm^2 and E:fE of 28) by simultaneously decreasing *Pr* and E:fE . Therefore , i t is still possible to improve the device reliability, including retention, while maintaining the same device performance.

Fig. 3(d) shows the FeFET memory windows as functions of *Pr* for four different E:fE . It suggests that the degradation in memory window caused by weak *Pr* can be compensated by reducing E:fE. This again demonstrates that pursuing a high *Pr* is no t the right direction as only marginal improvement in memory window can be achieved given the limited write voltage. Thus, the FeFET reliability can be improved without degrading its performance.

The simulated device-to-device variations in scaled FeFET are presented in Fig. 4. The model incorporates a Monte Carlo

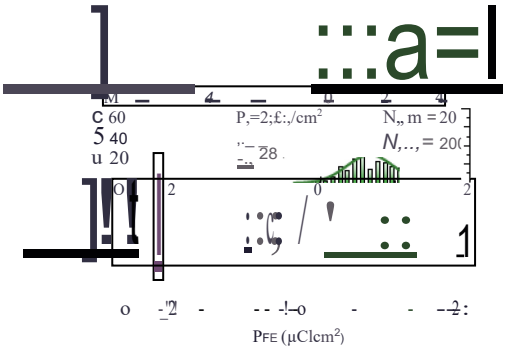


Fig. 4. Device-to-device variations of FeFETs with 3 different Pr and eFE combinations. The distributions of PFE alter + 4V and - 4V write pulses are shown. 200 devices each with 20 domains are simulated.

induced by the switching process [14]. For a FeFET with *Pr* of 20μC/cm^2 and eFE of 28, only 20% of domains participate in the switching. Reducing *Pr* to 2μC/cm^2 increases *EFE* framework, which allows to capture the intrinsic variations

during write, resulting in nearly full polarization switching. Reducing ε_{FE} to 9 further suppresses the variation. This suggests that, by proper charge matching between the ferroelectric and the semiconductor, *EFE* can be enhanced to enable full polarization switching, regardless of the ferroelectric domain distribution. This could potentially provide a way to suppress the variations. Note that this model only cap tures the lower bound of the variation as it only considers variation induced by the intrinsic ferroelectric switching process without taking into account the phase inhomogeneity [19] and sources for conventional transistor variations [20]. The appropriate design of relatively low *Pr* and ε_{IFE} ferroe lec trics compared to the prevailing values currently being pursued, should therefore be the target for the optimization of FeFETs for memory applications.

Engineering a HfO2 based ferroelectric film with low *Pr* and eFE should therefore be the target for the optimization of FeFET. Previously, a polarization reduction strategy has been proposed, which is to control the polarization orientation so that the out of plane polarization component can be reduced [13]. However, its effectiveness remains to be tested. Moreover, several other strategies can also be potentially applied. For example, it has been shown that by inhomoge- neous layering of HfO2 and SiO2, the remnant polarization and potentially also the dielectric constant can be reduced [21]. Another interesting approach to reduce *Pr* and eFE is through film engineering by adjusting the atomic layer deposition cycle ratio of HfO2 and *ZrOi* [22] . Therefore , exp loration in the process ing tech niques and their effectiveness in reducing *Pr* and EiFE , and thus improvement in FeFET reliability, will need to be performed in the future.

IV. CONCLUSION

Based on the simple principle of proper charge matching between the ferroelectric and its underlying semiconductor, we have presented a set of guidelines for optimizing HfO2-based FeFETs for nonvolatile memory applications. Specifically, our simulation results have demonstrated that, by appropriately reducing the ferroelectric's *Pr* and its background EiFE , the electrical stress in the interlayer/semiconductor can be reduced, the memory window can be improved,and the inter-device variations can be suppressed.

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