Dual-storage-port Nonvolatile SRAM based on Back-end-of-the-line Processed $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Capacitors Towards 3D Selector-free Cross-point Memory

Hao Jiang, Owen Li, Wen Li and T.P Ma, *Fellow, IEEE*

Abstract: This work presents the design and experimental demonstration of a novel dual-storage-port nonvolatile SRAM based on back-end-of-the-line processed $Hf_{0.5}Zr_{0.5}O_2$-based metal-ferroelectric-metal capacitors, which offers significant advantages over the conventional single-storage-port version without area penalty, and paves the way for implementing our proposed selector-free 3D cross-point memory.

***Index Terms*— Nonvolatile SRAM, Ferroelectric capacitor, Selector-free, 3D cross-point memory**

I. Introduction

Nonvolatile SRAM (NVSRAM) combines the advantages of SRAM, such as high speed and low power consumption, and non-volatility, which are highly desired for numerous applications in the era of Internet-of-Things (IoT) [1-6]. One of the most promising NVSRAM designs integrates SRAM cells with nonvolatile ferroelectric capacitors. Miwa et al. proposed and demonstrated a 6-transistor-2-capacitor (6T2C) NVSRAM, based on conventional perovskite ferroelectrics, which are difficult to scale beyond the 130 nm node [2]. Recently, ferroelectricity has been demonstrated in the $Hf_xZr_{1-x}O_2$ (HZO) material system fabricated at relatively low annealing temperatures (≤ 450 ^{0}C), suggesting the possibility of fabrication using the Back-End-of-the-Line (BEOL) process [7-11]. M. Kobayashi et al. successfully demonstrated functionalities of the NVSRAM with the same 6T2C configuration using the newly discovered HZO-based ferroelectric capacitors [5,6]. However, the attractive properties of HZO ferroelectric capacitors, especially their BEOL compatibility, remain to be further exploited for novel applications.

In this paper, we propose and experimentally demonstrate a novel 6T4C dual-storage-port NVSRAM by simply integrating two pairs of HZO-based ferroelectric capacitors onto SRAM cells through the BEOL process. The information can be selectively stored into and recalled from two nonvolatile storage ports, providing advantages over the traditional single-storage-port NVSRAM and offering one more choice to various IoT application scenarios. Moreover, our work can also be seen as one step further towards the realization of the 3D selector-free cross-point memory introduced last year by one of the authors [12,13].

Manuscript received XX; revised XX; accepted XX. Date of publication XX; date of current version XX. H. Jiang and T.P. Ma would like to acknowledge the partial support by the National Science Foundation under Award 1941316. The authors acknowledge Hengyuan Li and Stephen Chung at ITRI of Taiwan for fabrication help. The review of this letter was arranged by Editor XX.

H. Jiang, T.P. Ma are with the Electrical Engineering Department, Yale University, New Haven, CT 06511 USA (e-mail: hao.jiang@yale.edu, t.ma@yale.edu).

O. Li and W. Chen are with AP Memory Technology Corp., Zhubei, Hsinchu 30288, Taiwan (R.O.C.) (email: wchen@apmemory.com).

II. Experimental

For experimental demonstration, the front-end process of our dual-port NVSRAM was carried out at a commercial foundry based on its 0.18 µm technology node, and then the test wafers were transferred to a pilot line facility for the subsequent BEOL fabrication that included the HZO-based metal-ferroelectric-metal (MFM) capacitors with TiN as the electrodes and 10 nm atomic-layer-deposited (ALD) HZO films sandwiched in between. A nitride cap layer was used after the front-end process for protection during the transport, which was stripped off before the BEOL fabrication. A post-deposition annealing step at 450 ^{0}C for

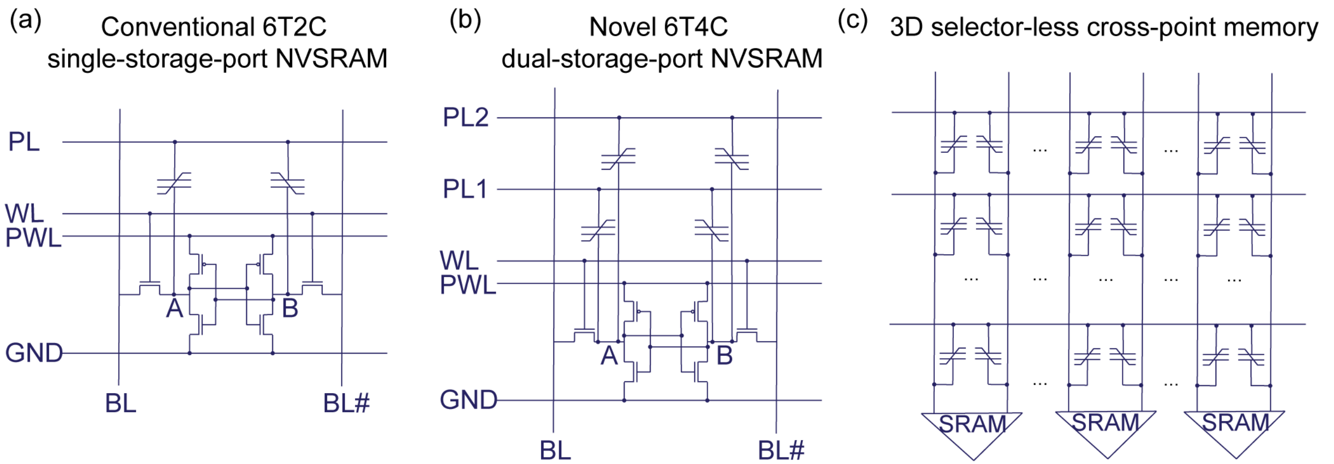


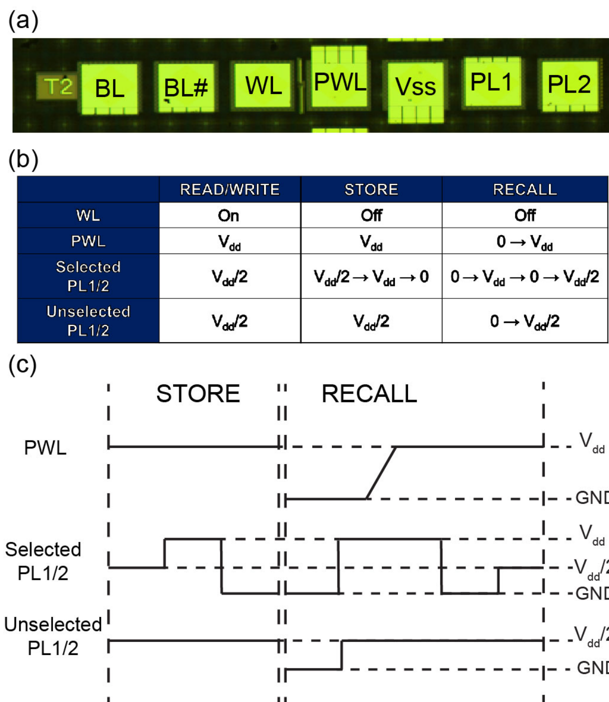
Figure 1 (a) Conventional 6T2C single-storage-port NVSRAM configuration [2,5], (b) our novel 6T4C dual-storage-port NVSRAM configuration, and (c) our proposed 3D selector-less cross-point memory architecture with differential design.

30s was employed to form the ferroelectric phase. The compatibility of the HZO-based ferroelectric capacitors using the same annealing temperature as the CMOS process was also demonstrated recently by T. Francois et al. [10], which suggests their potential for mass production. During the electrical measurements of these stand-alone MFM capacitors, the top electrodes were biased with the bottom electrodes grounded.

III. Results and Discussion

A. Design and Principle of Our Dual-storage-port NVSRAM

Fig. 1(a) shows the circuit diagram of a conventional 6T2C single-storage-port NVSRAM, which consists of a 6T-SRAM portion and a nonvolatile storage port by directly



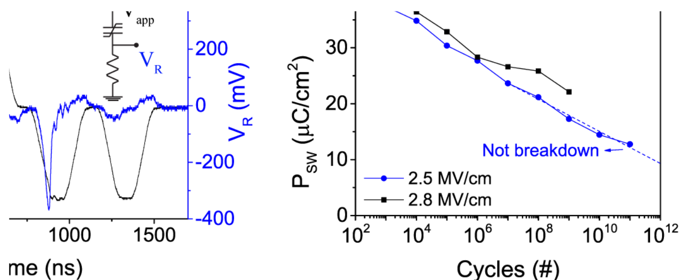
	READ/WRITE	STORE	RECALL
WL	On	Off	Off
PWL	V_{dd}	V_{dd}	$0 \rightarrow V_{dd}$
Selected PL1/2	$V_{dd}/2$	$V_{dd}/2 \rightarrow V_{dd} \rightarrow 0$	$0 \rightarrow V_{dd} \rightarrow 0 \rightarrow V_{dd}/2$
Unselected PL1/2	$V_{dd}/2$	$V_{dd}/2$	$0 \rightarrow V_{dd}/2$

Figure 3 (a) A partial photo of the fabricated chip shows contact pads assigned to different lines. (b) Bias conditions for the dual-storage-port NVSRAM during operation. (c) Schematic waveforms applied to PWL and PL1/2 during STORE and RECALL.

the power supply is back, one can either increase the power line (PWL) to Vdd with the PL kept at the ground level [2,5] or pull up the PL to Vdd before raising the PWL voltage from the ground level to Vdd [1], leading to the voltage difference at nodes A and B because of the difference in differential capacitance of the ferroelectric capacitors with opposite polarization states, and finally results in SRAM latching onto the pre-stored state. The Vdd needs to be carefully chosen such that, with Vdd applied during a STORE/RECALL operation, the voltage across the ferroelectric capacitors should be sufficient to trigger polarization switching, while no switching should occur when Vdd/2 is applied to the PL. It should be noted that the integration of extra capacitors delays the WRITE speed while it can shorten the read access time, making such NVSRAM more promising for many read-centric applications, which is the trend nowadays [2].

"1" written to SRAM	Before power-down	After RECALL	"0" written to SRAM	Before power-down	After RECALL
Storage port 1 selected with port 2 unselected					
BL	2.0 pA	2.0 pA	BL	35.9 μA	35.9 μA
BL#	33.9 μA	33.9 μA	BL#	2.0 pA	2.0 pA
Storage port 2 selected with port 1 unselected					
"1" written to SRAM	Before power-down	After RECALL	"0" written to SRAM	Before power-down	After RECALL
BL	2.0 pA	2.0 pA	BL	35.9 μA	35.9 μA
BL#	33.9 μA	33.9 μA	BL#	2.0 pA	2.1 pA

Figure 4 Demonstration of successful STORE/RECALL on a selected storage port with the other as the back-up. The storage port 1/2 refers to the pair of ferroelectric capacitors connected to PL1/2. The measured high currents are in blue to guide the eye.



ıpacitors with 4 different area sizes after wake-up. (b) PUND measurements using a 20 × 20 μm² capacitor. The rise/fall times and pulse width are all 100ns.

before it is worn-out, which can extend the device lifetime when compared with the previous single-storage-port design. More importantly, the dual-storage-port NVSRAM provides the unique flexibility that one can selectively store/recall different information into/from the two ports without doubling the transistor count nor increasing the cell area. We should also note that, although the introduction of an extra pair of capacitors will affect the programming speed, our dual-storage-port NVSRAM holds the potential for many applications with relaxed requirements on the WRITE speed.

	"1" stored to port 1 and "1" stored to port 2			
	Store "1" to port 1	Store "1" to port 2	RECALL from port 1	RECALL from port 2
BL	1.9 pA	1.9 pA	1.9 pA	1.9 pA
BL#	33.9 μA	33.9 μA	33.9 μA	33.9 μA
	"0" stored to port 1 and "0" stored to port 2			
	Store "0" to port 1	Store "0" to port 2	RECALL from port 1	RECALL from port 2
BL	35.9 μA	35.9 μA	35.9 μA	35.9 μA
BL#	2.0 pA	2.0 pA	2.0 pA	2.0 pA
	"1" stored to port 1 and "0" stored to port 2			
	Store "1" to port 1	Store "0" to port 2	RECALL from port 1	RECALL from port 2
BL	2.0 pA	36.0 μA	2.0 pA	35.9 μA
BL#	34.0 μA	2.0 pA	33.9 μA	2.0 pA
	"0" stored to port 1 and "1" stored to port 2			
	Store "0" to port 1	Store "1" to port 2	RECALL from port 1	RECALL from port 2
BL	35.9 μA	2.0 pA	35.9 μA	1.9 pA
BL#	1.9 pA	33.9 μA	2.0 pA	33.9 μA

Figure 5 Demonstration of successful STORE and selective RECALL on the two storage ports. The storage port 1/2 refers to the pair of ferroelectric capacitors connected to PL1/2. The measured high currents are in blue to guide the eye.

By further integrating more pairs of ferroelectric capacitors and making them into arrays, we can realize the 3D selector-free cross-point memory architecture with differential design, as illustrated in **Fig. 1(c)**, which is very attractive [12,13]. Each memory cell consists of only one pair of ferroelectric capacitors, without a transistor or any other selector device. However, further memory cell engineering may be required to optimize the above. For example, an ideal square-shape polarization-voltage (PV) hysteresis loop with large switchable polarization charge is desired, which has been recently demonstrated in the Al1-xScxN material system [14].

B. Characteristics of Fabricated Stand-alone HZO Ferroelectric Capacitors

Fig. 2(a) shows the typical PV hysteresis characteristics of stand-alone HZO ferroelectric capacitors with areas ranging from 20 × 20 μm^2 to 1 × 1 μm^2, where no significant size-dependence is observed, suggesting good potential for further scaling. The standalone capacitors are fabricated along with the dual-port NVSRAM devices on the same wafers through the same BEOL fabrication process. The PV loops were collected after a wake-up procedure (data not shown here). The statistical results of 20 × 20 μm^2 ferroelectric capacitors from 10 dice were obtained, demonstrating excellent device-to-device uniformity. The +/- P_r exhibit mean values of 20.311 and -20.918 μC/cm^2, with small standard deviations (STDs) of 0.2441 and 0.292 μC/cm^2, respectively. The mean value and STD for + V_c are 1.269 V and 17 mV, while for -V_c are -0.968 V and 25 mV. We performed the Positive-Up-Negative-Down (PUND) measurements of a 20 × 20 μm^2 capacitor with an RC circuit as shown in **Fig. 2(b)**. The voltage pulses have a rise/fall edge/width of 100 ns. The HZO ferroelectric capacitor can switch within 100 ns in our experimental setup, and faster speed is expected if the parasitic RC-delay can be reduced in the measurement system. **Fig. 2(c)** shows the endurance test results of a 20 × 20 μm^2 capacitor under two different electric fields of the same pulse shape shown in **Fig. 2(b)**. Under an applied electric field of 2.5 MV/cm, the capacitor continued to switch over 10^{11} cycles without breakdown. By extrapolation, a switchable polarization (P_{sw}) higher than 10 μC/cm^2 can be achieved after 10^{12} cycles. The results shown above serve to demonstrate rather reliable ferroelectric properties in the BEOL-processed HZO capacitors.

C. Demonstrated Functionality of our Dual-storage-port NVSRAM

The proposed 6T4C dual-storage-port NVSRAM devices were fabricated and their functionality was demonstrated. For the test devices, the six transistors for the SRAM portion have the same channel width/length of 1 μm, and the four ferroelectric capacitors have a size of 0.64 × 2.6 μm^2 each. A partial photo of the fabricated chip is shown in **Fig. 3(a)**, illustrating the contact pads assigned to different lines. The bias conditions for our dual-storage-port NVSRAM during normal SRAM READ/WRITE, STORE and RECALL operations are listed in **Fig. 3(b)**. The waveforms applied to the selected/unselected PLs and the PWL for STORE and RECALL are schematically shown in **Fig. 3(c)**. During measurements, Vdd is set to be 2.5V, and a world line (WL) voltage of 2V/0V is used to turn on/off the access transistors. For simplicity, the two bit-lines (BL and BL#) were biased with DC signals for WRITE and READ operations. To read out the state of the SRAM internal nodes (A and B) before power-down, or after RECALL when power-up, we pull up the two bit-lines (BL and BL#) to a high voltage level and measure their currents. It should be noted that quantitative analysis of the circuit's WRITE/READ speeds requires on-chip sensing circuits, which is included in our on-going/future work.

We first perform STORE and RECALL operations when one of the two ports is selected with the other unselected as the back-up. The measured currents from BL and BL# are listed in **Fig. 4**, illustrating successful RECALL of the pre-power-down SRAM states when the power is back. The demonstrated endurance of the HZO ferroelectric capacitors

ensure the NVSRAM devices are capable of sufficient power-down/RECALL cycles. The HZO ferroelectric capacitors can reliably retain their polarization states at room temperature and elevated temperatures [10], contributing to the robust data retention of the NVSRAM cells [6]. Successful RECALL has been experimentally demonstrated over 14 hours after power-down.

Finally, and more significantly, we have demonstrated that digital values can be stored in both ports and one can selectively RECALL from either of them. **Fig. 5** shows the experimental results from all four cases, which serve to highlight the novelty of our dual-storage-port NVSRAM.

IV. Conclusion

We have proposed and experimentally demonstrated a novel 6T4C NVSRAM, which is promising for numerous IoT applications, such as multiple context memory and programmable logic devices. Our work also suggests the possibility of incorporating 3D selector-less cross-point memory by integrating many pairs of ferroelectric capacitors through the BEOL process.

References

[1] G K. Dimmler and S. S. Eaton, "Memory cell with volatile and non-volatile portions having ferroelectric capacitors," *U.S. Patent* 4 809 225, Feb. 28, 1989.

[2] T. Miwa J. Yamada, H. Koike, H. Toyoshima, K. Amanuma, S. Kobayashi, T. Tatsumi, Y. Maejima, H. Hada, and T. Kunio, "NV-SRAM: a nonvolatile SRAM with backup ferroelectric capacitors," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 522, Mar. 2001. DOI: 10.1109/4.910492.

[3] T. Miwa et al., "A 512 Kbit low-voltage NV-SRAM with the size of a conventional SRAM," *IEEE Symp. On VLSI Circuits*, June 2001, Kyoto, Japan. DOI: 10.1109/VLSIC.2001.934217.

[4] S. Masui, T. Ninomiya, M. Oura, W. Yokozeki, K. Mukaida and S. Kawashima, "A ferroelectric memory-based secure dynamically programmable gate array," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 715, May 2003. DOI: 10.1109/JSSC.2003.810034.

[5] M. Kobayashi, N. Ueyama and T. Hiramoto, "A nonvolatile SRAM integrated with ferroelectric HfO_2 capacitor for normally-off and ultralow power IoT application," *IEEE Symp. On VLSI Technology*, June 2017, Kyoto, Japan. DOI: 10.23919/VLSIT.2017.7998161.

[6] M. Kobayashi, N. Ueyama, K. Jang and T. Hiramoto, "Experimental demonstration of a nonvolatile SRAM with ferroelectric HfO2 capacitor for normally off application," *IEEE J. Electron Dev. Soc.* vol. 6, no. 1, pp. 280, Jan. 2018. DOI: 10.1109/JEDS.2018.2800090.

[7] J. Müller, T. S. Böscke, S. Müller, E. Yurchuk, P. Polakowski, J. Paul, D. Martin, T. Schenk, K. Khullar, A. Kersch, W. Weinreich, S. Riedel, K. Seidel, A. Kumar, T. M. Arruda, S. V. Kalinin, T. Schlösser, R. Boschke, R. van Bentum, U. Schröder, and T. Mikolajick, "Ferroelectric Hafnium Oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," *in IEDM Tech. Dig.*, Dec. 2013, pp. 10.8.1–10.8.4. DOI: 10.1109/IEDM.2013.6724605.

[8] T. Mikolajick, S. Slesazeck, M. H. Park, and U. Schroeder, "Ferroelectric hafnium oxide for ferroelectric random-access memories and ferroelectric field-effect transistors," *MRS Bulletin*, vol. 43, pp. 340-346, 2018. DOI: 10.1557/mrs.2018.92.

[9] M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon, and C. S. Hwang, "Evolution of phases and ferroelectric properties of thin $Hf_{0.5}Zr_{0.5}O_2$ films according to the thickness and annealing temperature," *Appl. Phys. Lett.*, vol. 102, no. 24, pp. 242905, June 2013. DOI: 10.1063/1.4811483.

[10] T. Francois, L. Grenouillet, J. Coignus, P. Blaise, C. Carabasse, N. Vaxelaire, T. Magis, F. Aussenac, V. Loup, C. Pellissier, S. Slesazeck, V. Havel, C. Richter, A. Makosiej, B. Giraud, E. T. Breyer, M. Materano, P. Chiquet, M. Bocquet, E. Nowak, U. Schroeder, F. Gaillard, "Demonstration of BEOL compatible ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ scaled FeRAM co-integrated with 130nm CMOS for embedded NVM applications," *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, San Francisco, United States. DOI: 10.1109/IEDM19573.2019.8993485.

[11] S. J. Kim, D. Narayan, J. Lee, J. Mohan, J. S. Lee, H. S. Kim, Y. C. Byun, A. T. Lucero, C. D. Young, S. R. Summerfelt, T. San, L. Colombo, and J. Kim, "Large ferroelectric polarization of $TiN/Hf_{0.5}Zr_{0.5}O_2/TiN$ capacitors due to stress-induced crystallization at low thermal budget," *Appl. Phys. Lett.* vol. 111, no. 24, pp. 242901, Nov. 2017. DOI: 10.1063/1.4995619.

[12] W. Chen, "Selector-free cross-point memory architecture based on ferroelectric MFM capacitors," *IEEE International Memory Workshop (IMW)*, June 2019, Monterey, United States. DOI: 10.1109/IMW.2019.8739707.

[13] W. Chen, "Ferroelectric memory device," *U.S. Patent* 10 109 350, Oct. 23, 2018.

[14] S. Fichtner, N. Wolff, F. Lofink, L. Kienle and B. Wagner, "AlScN: A III-V semiconductor based ferroelectric," *J. Appl. Phys.* vol. 125, no. 11, pp. 114103, Feb. 2019. DOI: 10.1063/1.5084945.