A Reliability Study of Thickness Dependence of HfO_2-based 3D-FeRAM Cell

Olivier Maher*, Hao Jiang, Zhan Liu and T.P. Ma
Department of Electrical Engineering, Yale University – Olivier.Maher@yale.edu

Introduction

Among the various emerging memory technologies, the FeRAM (Ferroelectric Random-Access-Memory) is a promising candidate for ultralow power, high speed, and non-volatile memory applications. The currently commercialized FeRAM employs conventional ferroelectric materials that suffer from severe drawbacks that have prevented FeRAM's scaling ever since it reached the 130nm node two decades ago. A detrimental problem for continued scaling is that, beyond the 130nm node, 3D (trenched or stacked) storage capacitors are needed to enhance the effective area of the storage capacitor in order to enable the sensing circuit to function, just like the DRAM memory technology, but neither PZT nor SBT would show ferroelectric properties when deposited on the side-walls [2]. Since the advent of the novel HfO_2-based ferroelectric materials in 2011 [1], the ferroelectric memory community has been re-energized, which has led to the publication of 3D FeFRAM cells built on trenches etched into Si substrates deposited with Al-doped HfO_2 that exhibits ferroelectric properties on trench walls [2]. Although this is an excellent accomplishment, the Al-doped HfO_2 requires fairly high temperatures to achieve the required ferroelectricity, which precludes its use in the back-end-of-the-line process. In this paper, we report the study of the retention and endurance characteristics of $Hf_xZr_{(1-x)}O_2$ (HZO)-based 3D FeRAM memory cells that are compatible with back-end applications, due to its low thermal budgets (~450°C for less than 1h).

Experiments

The 3D MFM (Metal-Ferroelectric-Metal) capacitors in this study are fabricated using ALD to deposit the HZO films at 250°C on Si substrates having pre-etched trenches coated with 3nm TiN film as the bottom electrodes. The trenches all have 0.6µm in depth, with various diameters (0.15, 0.2, 0.25, 0.35, and 0.5µm). Three different HZO thicknesses are studied ($\mathbf{d_F}$ = 7, 10, and 15nm). After the top TiN (3nm in thickness) deposition and metal pattern etching, a post-metal annealing step was used to form the ferroelectric. Fig. 1 shows a schematic drawing of a representative 3D FeRAM cell used in this study compared to the conventional 2D devices. After sample fabrication, standard electrical measurements are performed to obtain the *P-V* hysteresis loops, the endurance as well as the retention characteristics at various temperatures, and to study the associated mechanisms.

Results and discussion

Fig. 2 shows the typical *P-V* characteristics for a trenched sample (3D) in comparison with a planar sample (2D) of the same projected area, showing much enhanced polarization of the former due to the increased effective area arising from the side walls. Fig. 3 shows the RT retention characteristics for 3D samples with 3 different thicknesses, each switched under 3 different fields. Note that the starting polarizations are all different for different samples as expected, but what's striking is that the trend is qualitatively the same for all curves, despite the wide range of thicknesses and applied fields. This observation may provide an important clue for solving the retention puzzle. The data are quite encouraging for 3D FeRAM retention as essentially all curves passed the 10-year retention mark. Fig. 4 shows the retention characteristics at elevated temperatures for the 10nm samples, where one can see that it does meet the 10-year requirement at 85°C, but it falls short above that ***T°***. Fig. 5 shows the endurance characteristics for the same group of samples shown in Figure 3. where one can see that basically all samples survived 10^{10} cycles, and the two thinner samples (7 and 10nm) reached 10^{13} (extrapolated) with relatively low switching fields (2MV/cm). These are record numbers for 3D FeRAM cells, as far as we know. One should note that, in the cases that failure occurs around 10^{10} cycles, the failure mode is primarily due to dielectric breakdown. Based on our knowledge of dielectric breakdown in ultra-thin CMOS gate dielectrics, the total injected charge passing through the dielectric is a critical factor that determines the breakdown event. We decided to investigate the gate leakage currents in these samples as well as the associated current conduction mechanisms. From our extensive temperature-dependent *I-V* measurements (not shown here), we decided that Fowler-Nordheim (F-N) is most likely for the 15nm sample and Poole-Frenkel (P-F) is most likely for the 7nm sample, and therefore, focused our subsequent studies accordingly. Figs. 6(a) through 6(f) are various plots to fit the F-N and P-F models, from which we have been able to determine the barrier heights and the trap energies. These results will be discussed at the SISC Conference.

Summary

Thickness-dependent reliability in 3D-Cap HfO_2-based FeRAM capacitors has been studied. Results show endurance larger than 10^{11} cycles and >10 years of extrapolated retention time. A significant polarization gain was made possible due to trenched capacitors that enhanced the effective areas. A major cause of the endurance failure is the dielectric breakdown after numerous cycles, which is linked to the gate leakage

currents. Our temperature-dependent study of I-V characteristics has revealed Fowler-Nordheim tunneling at low temperatures and Frenkel-Poole conduction at room-to-high temperatures as the culprits. Such findings will be helpful for future commercialization of this technology.

Acknowledgement

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References

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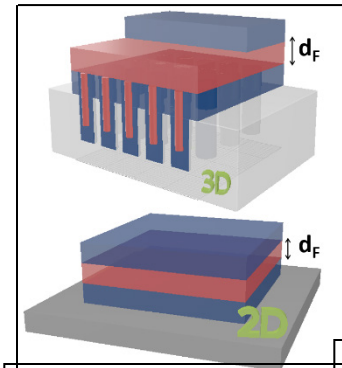

Fig. 1. 3D trench capacitor FeRAM and conventional 2D

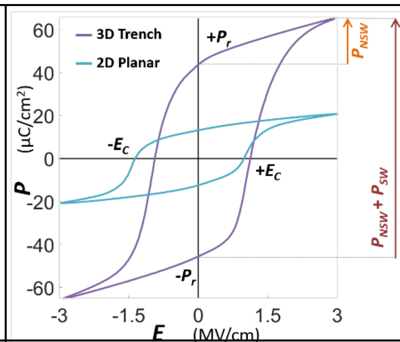

Fig. 2. *P-V* loops of 3D FeRAM with 4225 0.6μm deep trenches evenly spaced (TiN), and 2D FeRAM with 260°C HZO deposition (TaN)

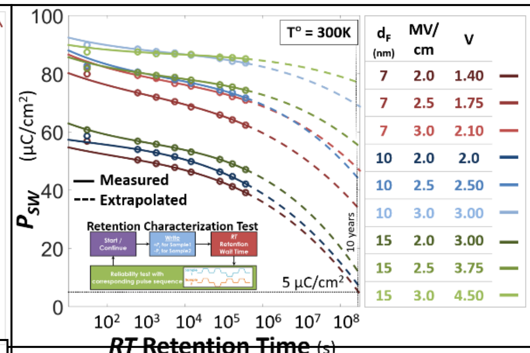

Fig. 3. Retention characteristics of 3D-Cap FeRAMs for $\mathbf{d_F}$ =7nm, 10nm and 15nm at room $\boldsymbol{T°}$. $\boldsymbol{P_{SW}}$ was calculated by subtracting the response of Sample1 to the response of Sample2 at specific times.

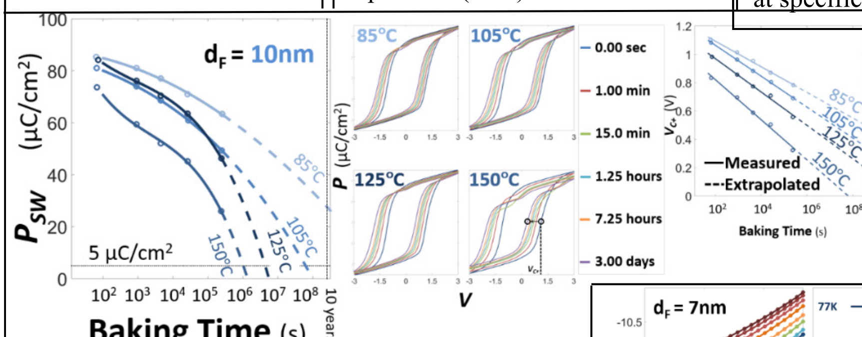

Fig. 4. Retention characteristics of 3D-Cap FeRAMs for $\mathbf{d_F}$ = 10nm at room 85°C, 105, 125 and 150C. *P-V* loops with corresponding coercive $\boldsymbol{V_C}$ shifts

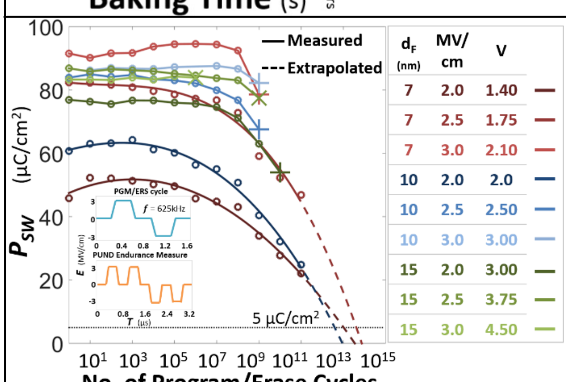

Fig. 5. Endurance failure mechanism of 3D-Cap FeRAMs for $\mathbf{d_F}$ =7nm, 10nm and 15nm. **-X-** marks represent breakdown points.

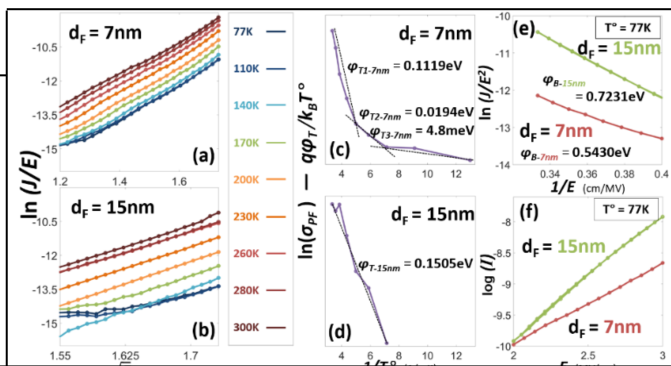

Fig. 6. Poole-Frenkel plots for $\mathbf{d_F}$=7nm (a), and for $\mathbf{d_F}$=15nm(b). If *P-F* is a dominant mechanism, a plot of ln($\boldsymbol{J}$/$\boldsymbol{E}$) against $\sqrt{\boldsymbol{E}}$ should be linear. Fowler-Nordheim plots for $\mathbf{d_F}$=7nm and $\mathbf{d_F}$=15nm(e) at 77K to supress thermionic emission. If *F-N* is dominant at low T°, a plot of ln($\boldsymbol{J}$/$\boldsymbol{E^2}$) vs. 1/$\boldsymbol{E}$ should be linear. *I-V* plot at 77K for $\mathbf{d_F}$=7nm and $\mathbf{d_F}$=15nm (f)