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Applications and Impacts of Nanoscale Thermal Transport in Electronics Packaging

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ABSTRACT

This review introduces relevant nanoscale thermal transport processes that impact thermal abatement in power electronics applications. Specifically, we highlight the importance of nanoscale thermal transport mechanisms at each layer in material hierarchies that make up modern electronic devices. This includes those mechanisms that impact thermal transport through: (1) substrates, (2) interfaces and 2-D materials and (3) heat spreading materials. For each material layer, we provide examples of recent works that (1) demonstrate improvements in thermal performance and/or (2) improve our understanding of the relevance of nanoscale thermal transport across material junctions. We end our discussion by highlighting several additional applications that have benefited from a consideration of nanoscale thermal transport phenomena, including RF electronics and neuromorphic computing.

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A. INTRODUCTION

This review discusses relevant nanoscale thermal transport processes impacting thermal abatement in power electronics applications. In the introduction section, the impact of nanoscale thermal transport on electronics thermal management is established, and a primer is given on the physics governing nanoscale thermal transport. With core concepts established, several brief perspectives are provided on relevant topics dealing with nanoscale thermal transport in power electronics. Figure 1 depicts the organization of the contents of this paper.

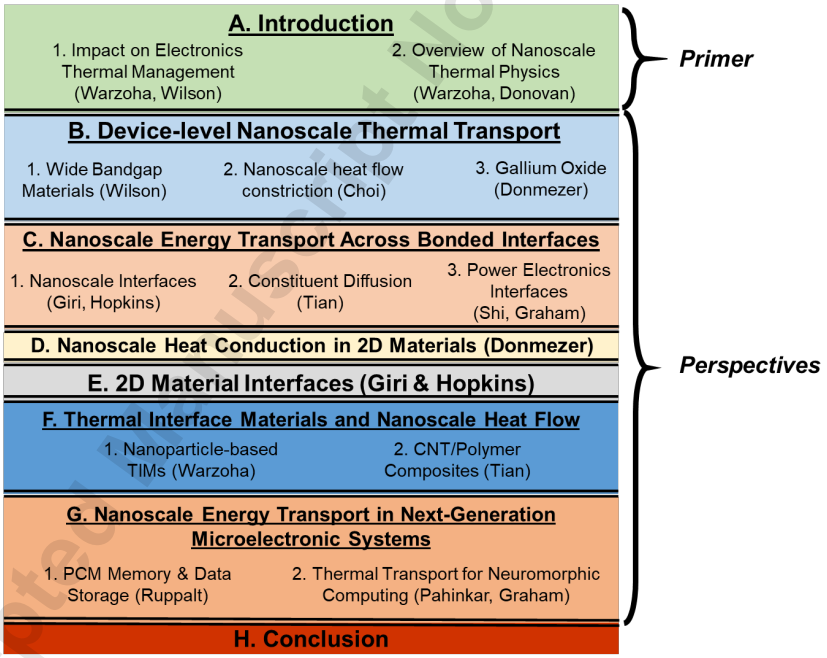

Figure 1: Outline of content in this review article.

A.1. Impact on Electronics Thermal Management

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Electronics thermal management is critical to the implementation of modern computational architectures [1], power electronics [2], re-writeable media [3] and, more recently, data storage and transfer [4, 5]. Increasingly at odds with continued advancements in the performance of such applications, however, is a reduction in the characteristic length scales of heat generating elements that support primary functionality. The magnitude of this singular issue is now widely expected to result in the violation of Moore's Law within the next decade, captured by Fig. 2 and described below.

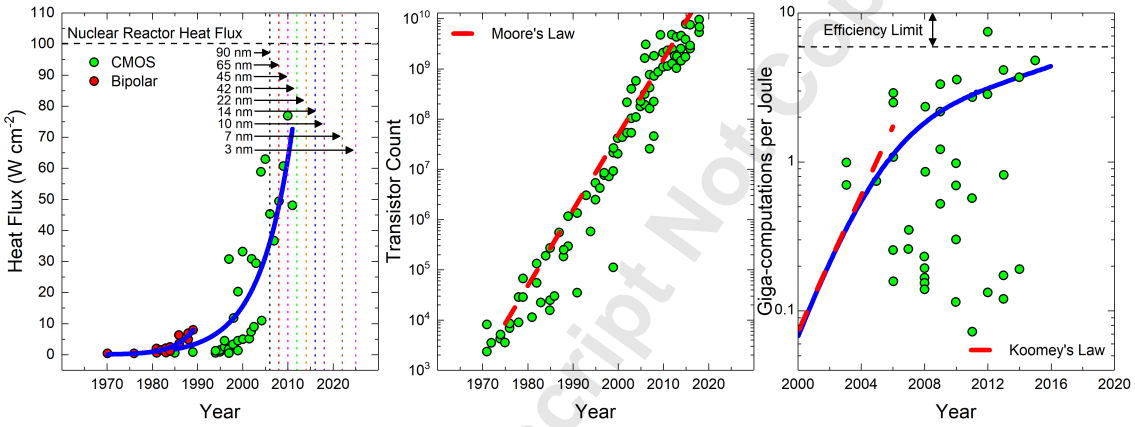

Figure 2: (a) Historical trend in heat flux of Bipolar and CMOS-based CPU architectures (data taken from [6, 7]) (b) Rate of increase in CPU transistor count relative to Moore's Law (red dashed line; data taken from [8, 9]) and (c) Computational efficiency of CPUs as a function of year and transistor length-scale (data and trends taken from [10]).

Moore's Law has remained stable for nearly five decades, principally due to advancements in cooling technologies and simultaneous improvements in computational efficiency with developments in parallel processing, GPU architectures and, more recently, 3-D chip stacks [11]. However, both computational efficiency and cooling technologies are beginning to approach their fundamental limits [12]. Consequently, Moore's Law for conventional CMOS-based architectures is predicted by some to run its course within the next decade [13-15].

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Beyond these fundamental limits, the size of individual electronic components are fast approaching length scales that are on the order of the primary mean free paths of thermal energy carriers. FinFET technologies, for example, are expected to result in the fabrication of 3 nm transistors in the near future [16], orders of magnitude smaller than the majority of thermal carrier mean free paths in silicon [17]. As thermal management is concerned, the physics that govern heat dissipation within a material and across an interface are not the same as those experienced in bulk material systems. At these length scales, the physics that govern heat dissipation within a material and across interfaces deviate significantly from bulk thermal properties.

Accordingly, when exploring the thermal impact of electronic size scaling, we need to consider the nanoscale properties of the thermal carriers carefully. At these scales, heat energy carriers (primarily phonons in non-conducting materials) can be interrupted by atomic defects, phonon-phonon interactions, nanoparticles, grain boundaries, material mismatches in phonon density of states at a boundary and, in electrically conducting materials, electron-phonon and electron-interface interactions [18]. Figure 3 illustrates the variety of phonon scattering mechanisms that govern thermal transport at these length scales.

Given the level of complexity associated with nanoscale thermal transport physics and the scattering mechanisms outlined in Fig. 3, it is *critical* to understand and model these energy exchange and transfer mechanisms for the successful development and implementation of next-generation electronics devices. In this work we specifically focus on nanoscale thermal transport in next-generation microelectronic devices.

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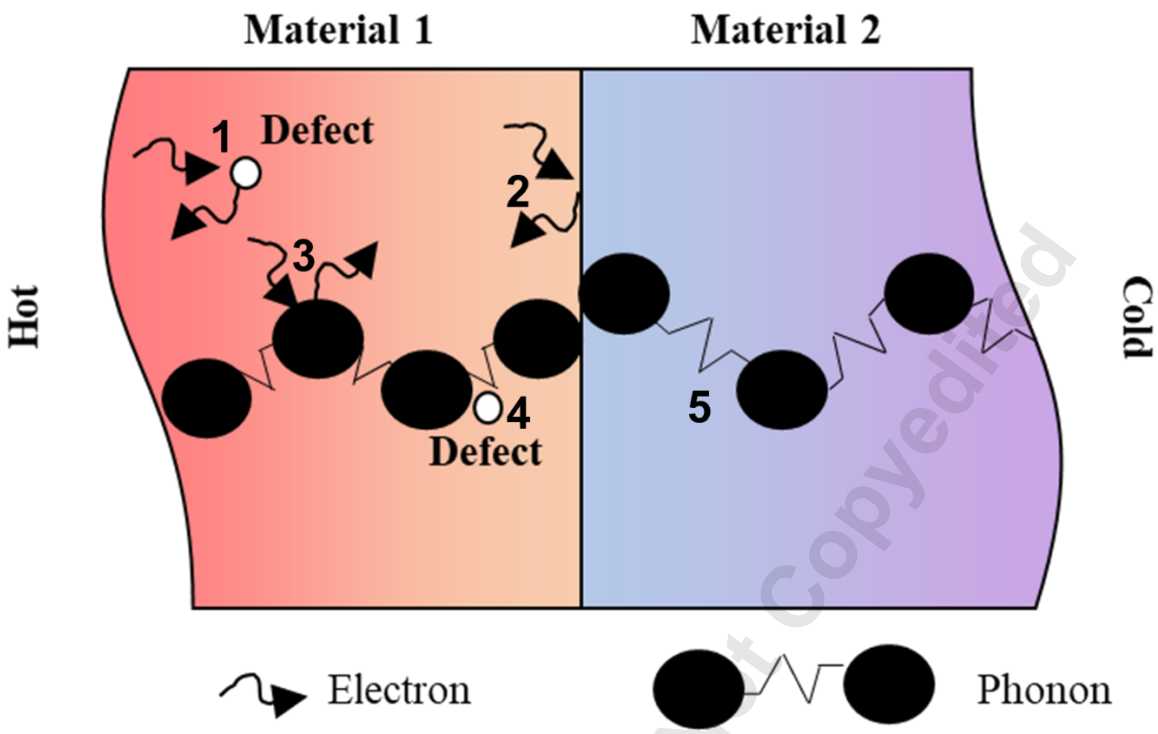

Figure 3: Schematic of phonon scattering mechanisms within individual materials and across interfaces, including: 1) electron-defect scattering [19], 2) electron-interface scattering [20], 3) electron-phonon scattering [21], 4) phonon-defect scattering [22], 5) phonon-phonon scattering [23] and 6) scattering across an interface based on mismatches in material density of states [24], interface surface roughness [25], etc.

To demonstrate the key areas where phonon scattering plays a critical role in electronics packaging, we consider a typical electronic package configuration. This is depicted in Fig. 4, together with a representative temperature distribution of the device, which depends on the thermal resistance of each constituent element. The device is comprised of several layers of differing materials, interfaces between those materials, and a bulk substrate. The devices are packaged on die attached via thermal interface materials and are then coupled to a heat sink. Each of these components in the package contain opportunities for nanoscale thermal transport to provide a substantial enhancement in device performance. At the device level, the interfaces and small scale of the devices make nanoscale thermal metrology crucial for further development – whether the goal is to reach higher power or to continue trends in device miniaturization. At the package level,

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nanoscale thermal transport is necessary to understand what makes a better thermal interface material, or how to remove heat from the package at the heat sink effectively. Furthermore, the materials used may see reduction in phonon scattering by removing scattering sites such as defects and dislocations via improved processing parameters, thus increasing the thermal conductivity of the layer adjacent to the interface. Therefore, in the electronics package, from material-level to device-level to packaging-level, nanoscale thermal transport is critical to further advances in performance.

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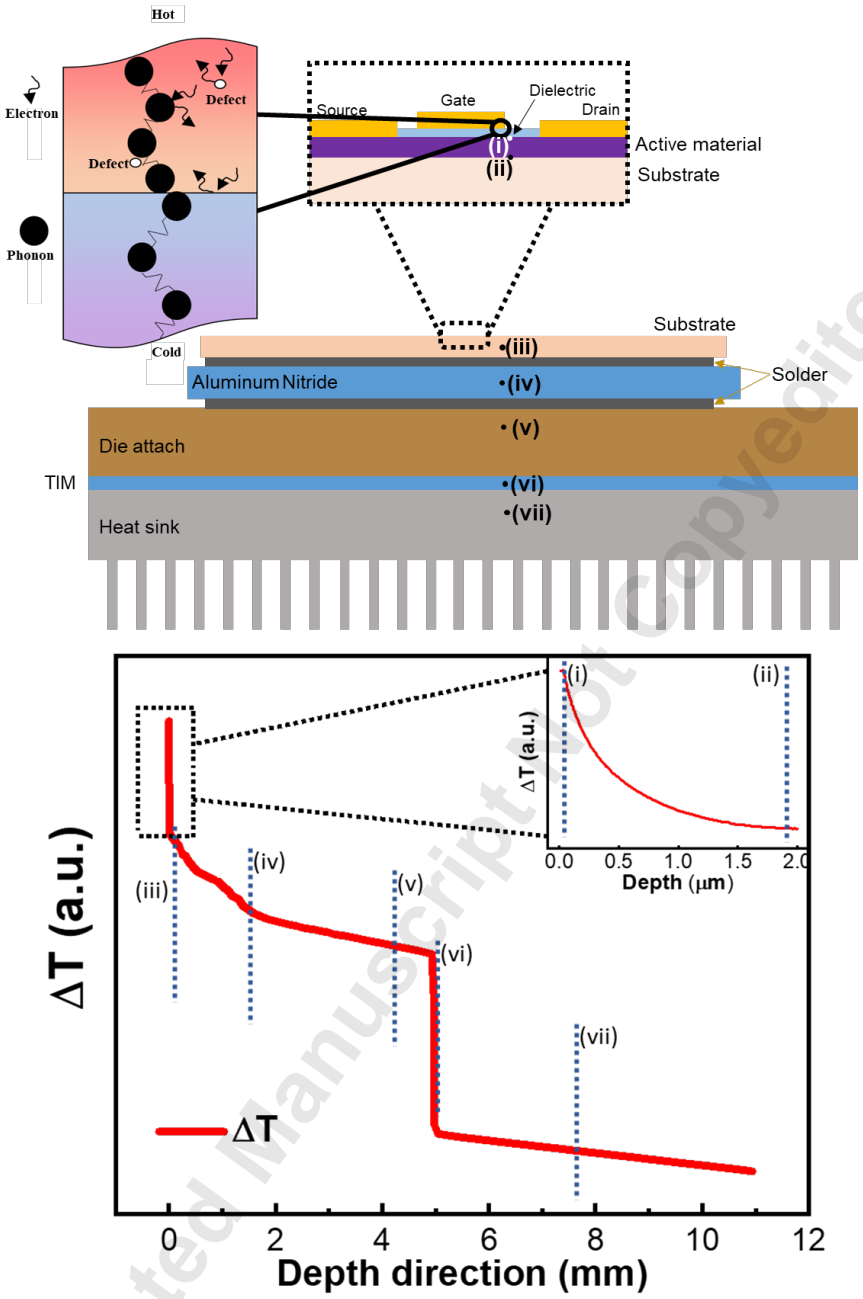

Figure 4: Representative electronics package and active device temperature profile. Temperature profiles are combined from adapted data appearing in [26] and [27].

In this work, we put forth a series of perspectives constructed by the authors to highlight the nanoscale thermal physics used to model scattering mechanisms within materials and across interfaces. In particular, we provide the reader with analytical and numerical techniques that lend physical insight into heat flow through materials and

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interfaces that are critical in electronics packaging and discuss experimental evidence of these consequences in application. A final discussion of nanoscale thermal transport in RF-based devices and thermoelectric materials is provided to demonstrate the broad class of application space where these physics are critical to electronic device performance and cooling.

A.2. Nanoscale Thermal Physics

In the ensuing sub-sections, we provide a limited overview of the physics that are typically used to analytically model thermal transport both (a) within materials and (b) across device interfaces. These topics are covered in great detail elsewhere [18, 28-30] and are provided here to give those readers unfamiliar with nanoscale thermal transport context for the perspectives written as part of this work.

A.2.i. Thermal Transport within Nanostructured Materials

In solids, heat is carried predominantly by electrons (for metals) and/or phonons (for non-conducting materials). At device length scales proportional to the mean free path of these energy carriers, scattering elements like grain boundaries and point defects can profoundly reduce the thermal conductivity of a material, which then makes thermal abatement significantly more challenging for packaging engineers. Consequently, a fundamental understanding of energy carrier scattering is critical to the design of thermal management solutions for next-generation packaging systems.

For electrically conducting materials, thermal conductivity (κ) is governed by an electronic component (κ_e) and a phononic component (κ_{ph}) such that $\kappa = \kappa_e + \kappa_{ph}$. The

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electronic component of thermal conductivity can be approximated by the Wiedemann-Franz Law [31],

$$\kappa_e = \sigma \cdot \frac{\pi^2}{3} \cdot {k_{B,eV}}^2 \cdot T \quad (1)$$

where σ is the electrical conductivity of the material (S/m), $k_{B,eV}$ is the Boltzmann constant in electron volts, and T is the absolute temperature of the material (K). We note that the electronic structure and scattering in materials can result in the underprediction of κ_e when applying the Wiedemann-Franz Law, but for most electrically-conducting materials, the Wiedemann-Franz Law provides accuracy to within ~40% at non-cryogenic temperatures [32-34]. Several mechanisms can contribute to electron scattering, including electron-electron and electron-phonon scattering [35]. In the remainder of this work, we limit further discussion of nanoscale thermal transport to phononic contributions to thermal conductivity as the majority of our nanoscale constituents and interfaces include non-conducting materials.

Phonons are quantized lattice vibrations that are best thought of as a collective set of atomic oscillations about their equilibrium positions. The oscillations are governed by the atomic mass(es) of atoms, the strength of the bonds between neighboring atoms and the material system geometry. Together, these material characteristics synchronize the modes of vibration, which are collectively termed "phonons".

The phononic contribution to thermal conductivity can be quantitatively determined using a variety of analytical, numerical and experimental techniques. Commonly used analytical techniques include solutions to the Boltzmann Transport Equation (BTE) [36, 37] and augmentations to the well-known phonon gas model [38] (more on this below). Computational simulations can be performed using molecular

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dynamics (MD) simulations [39-42], density functional theory (DFT) [43, 44] and Monte Carlo ray tracing simulations [45, 46]. Finally, nanoscale experimental techniques include electro-thermal characterization (3-ω [47], transient electro-thermal [48, 49], and scanning-probe based [50-52] systems) and optical pump-probe thermoreflectance characterization (time-domain thermoreflectance, or TDTR [53-56] frequency-domain thermoreflectance, or FDTR [57-59] and steady-state thermoreflectance, or SSTR [60]).

We use the phonon gas model [18, 61] here to illustrate the impacts of nanostructuring on the intrinsic thermal properties of Si due to its simplicity and the ability to model independent scattering parameters such that we can demonstrate their potential impacts on thermal conductivity. This model represents the phonons in our system as a gas of energetic carriers with thermal energy, speed, and mean free paths that depend on the mode of vibration given by,

$$\kappa = \frac{1}{3}\sum_j \int_0^{k_{max}} C_{v,k} \cdot v_j^2 \cdot \tau_j \, dk \tag{2}$$

where,

$$C_{v,k} = \frac{1}{2\pi^2}\sum_j \int_0^{k_{max}} \hbar \cdot \omega \cdot \frac{\partial f_{BE}}{\partial T} \cdot k^2 \, dk \tag{3}$$

In Eqn. 2, C_v is the volumetric heat capacity of the solid (J/m^3·K), ν is the phonon group velocity (or sound speed in a Debye approximation [62]) within the solid (m/s) and τ is the phonon scattering time (s). In Eqn. 3, which assumes an isotropic, spherical Brillouin zone, $\hbar$ is Planck's constant (J·s), ω is angular frequency (rad/s), $\partial f_{BE}/\partial T$ is the temperature-dependent Bose-Einstein distribution, and k is wave vector (rad/m). Note that one must incorporate contributions from all polarization branches, j, to compute the total thermal conductivity, κ, and volumetric heat capacity, C_v.

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There are several phonon scattering mechanisms that are particularly relevant to microelectronic and power electronic-based material systems. These include phonon-phonon scattering (or so-called "Umklapp" and "Normal" scattering), τ_{ph}, baseline impurity scattering, τ_{bulk}, boundary scattering, τ_b and defect scattering, τ_d. Boundary scattering refers to phonons that collide and scatter off of a physical boundary, which could be the characteristic dimension of the system (i.e., the layer thickness) or inherent boundaries within the system (i.e., grain boundaries). Likewise, the defect scattering term represents both point defects and vacancies.

Typically, the theoretical (or ideal) temperature-dependent thermal conductivity ($\kappa(T)$) for a bulk material is used to determine the magnitude impact of phonon-phonon and baseline impurity scattering by fitting Eqn. 2 to [18],

$$\tau_{bulk} = \left(A \cdot T \cdot \omega^2 \cdot e^{-B/T} + C \cdot \omega^4\right)^{-1} \quad (4)$$

where A, B and C are fitting constants. Provided these fitting constants, one can then determine the impact that characteristic length-scales, material impurities and crystalline microstructure have on thermal conductivity. We choose to demonstrate the magnitude that length-scale has on thermal conductivity for three relevant materials: Si, GaN and AlN. Using the phonon dispersion provided above each temperature-dependent thermal conductivity distribution in Fig. 5, we determine constants A, B and C for each bulk material.

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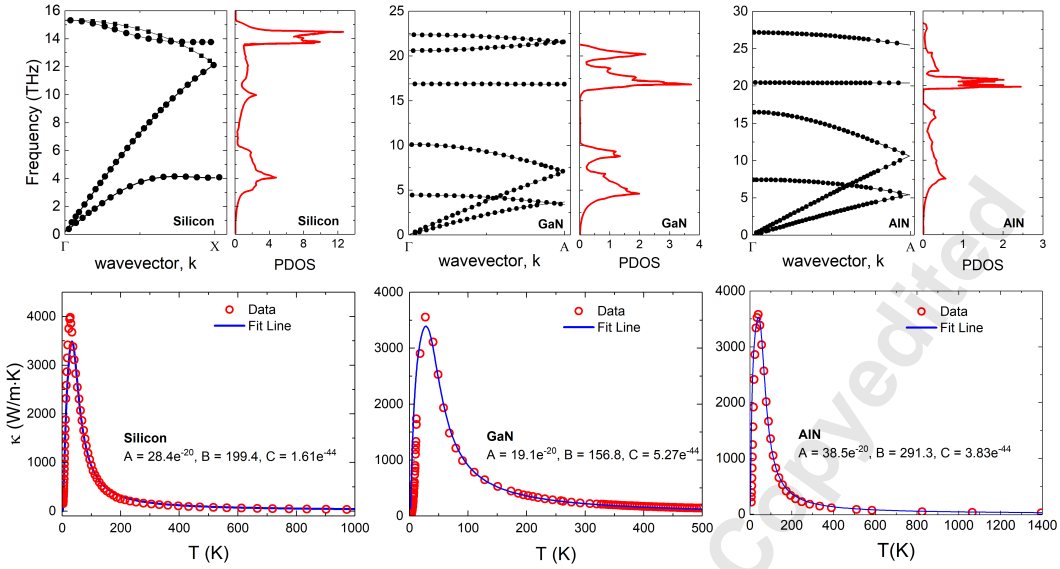

Figure 5: *Top*: Plots of phonon dispersion relations along a representative direction of high symmetry in the primitive unit cell for Si [63] (*left*), Wurtzite GaN [64] (*middle*) and Wurtzite AlN [64] (*right*) next to the phonon density of states [65] (units: States/THz-Unit Cell). Note that we assume a spherical, isotropic Brillouin Zone for the Wurtzite GaN and AlN only for instructional purposes. In a real Wurtzite material system, a more rigorous (and complex) anisotropic model must be used. *Bottom*: Temperature-dependent thermal conductivity for Si (*left*) [66], Wurtzite GaN (*middle*) [67] and Wurtzite AlN [68] (*right*) used to determine constants A [$s \cdot K^{-1}$], B [K] and C [s^3] in Eqn. 4 (blue lines represent fit lines, and red circles represent data). Note that we fit to the dispersion branches using 4th order polynomial relationships.

With knowledge of these bulk fitting parameters (A, B, and C), we can accurately estimate the impact that scattering from additional mechanisms may have on material thermal conductivity. In this work, we provide the reader with context for the impacts that the characteristic length scale (d_{film}), and the mass and concentration of defects (M_{def} and φ_{def}) have on the intrinsic thermal conductivity of the Si, GaN and AlN materials detailed in Fig. 5. To account for the impact that characteristic length scale has on thermal conductivity, we utilize [59],

$$\frac{1}{\tau_b} = \frac{\upsilon_g}{d_{film}} \tag{5}$$

where τ_b is the boundary scattering parameter (s), υ_g is the phonon group velocity (m/s) and d_{film} is the characteristic dimension (in this case the film thickness, m). Likewise, we

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quantify the impact that both defect mass and concentration have on these thermal conductivities with [22],

$$\frac{1}{\tau_d} = \omega^4 \cdot \chi_d \cdot \left[\left(\frac{\Delta M_d}{M_h} \right)^2 + 2 \cdot \left[\left(\frac{\Delta G_d}{G_h} \right) - 6.4 \cdot \gamma \cdot \left(\frac{\Delta \delta_d}{\delta_h} \right)^2 \right] \right] \quad (6)$$

where τ_d represents the defect scattering parameter, ω is the angular frequency of the phonon modes (1/s), χ_d is defect concentration, ΔM_d is the difference in mass between the defect and the average host atom (M_h), ΔG_d is the difference in shear strength between the defect and the average host atom (G_h), γ is the Grüneisen parameter and $\Delta\delta_d$ is the difference between defect and average host atom radii (δ_h).

To vary the impact of characteristic length scale, the thermal conductivity of 100 nm to 1 mm-thick films of Si is determined using Eqns. 2 and 5 in tandem. Similarly, the concentration of defects (χ_d) is changed to demonstrate its impact on thermal conductivity. Both results are reported in Fig. 6.

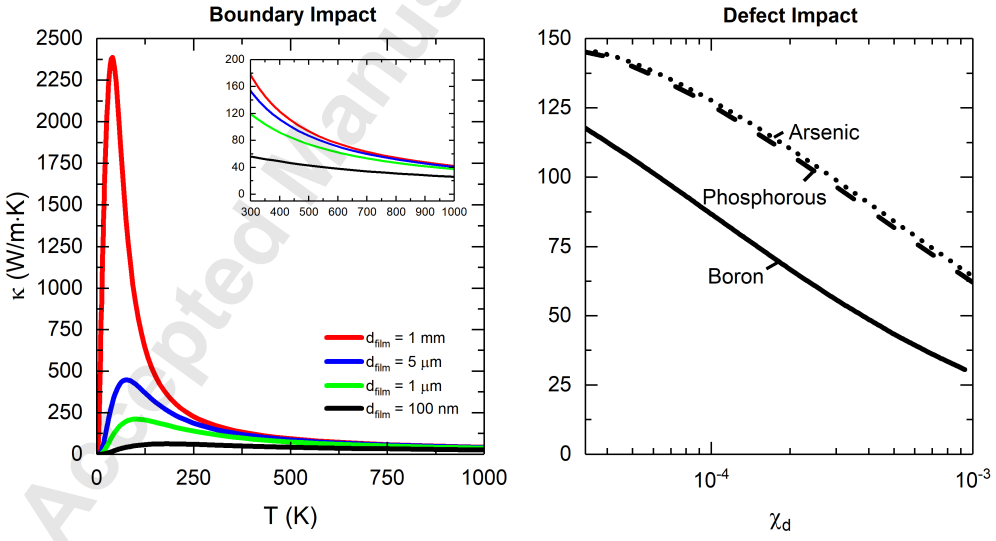

Figure 6: *Left*: Thermal conductivity of Si as a function of temperature and film thickness (red line = 1 mm thick, blue line = 5 µm thick, green line = 1 µm thick and black line = 100 nm thick; Note: inset represents the same distribution over the high temperature range exclusively), *Right*: Thermal conductivity of Si as a function of defect concentration, χ_d, for typical dopants B, P and As.

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Figure 6 clearly indicates that nanostructuring can have an extreme impact on the thermal properties of microelectronics and power electronics-based materials. In this case, thin films of materials and material defects negatively impact (i.e., reduce) the thermal conductivity of the host material(s) and therefore increase the need for more aggressive thermal abatement strategies.

A.2.ii. Thermal Transport across Nanostructured Materials

As with the thermal properties of the films themselves, thermal transport across thin-film interfaces can be impacted by nano-sized features. Critically, even perfectly bonded interfaces experience a temperature drop due to a finite thermal boundary conductance [30]. This is particularly important as device length-scales are reduced and the interfaces between materials begin to contribute more significantly to the overall thermal resistance in the device stack, rendering it difficult to remove heat at the device level. In general, this is not always a detriment; one can deliberately scatter phonons by engineering interfaces, which has proven critical for the development of advanced, nanostructured thermoelectric materials [63, 69, 70].

The conventional analytical framework for determining the so-called "thermal boundary conductance" (or h_{BD}) across a bonded interface is predicated on whether energy carrier scattering occurs diffusely or is governed by acoustic reflections of phonons at a material junction. In particular, the Diffuse Mismatch Model (DMM) and Acoustic Mismatch Model (AMM) were developed to better understand heat flow across atomically smooth interfaces [71].

The AMM treats phonon scattering as a purely specular process at an individual interface (note that the analog to this treatment is the handling of optical reflections via Snell's Law [30, 72]). In order to quantify the thermal conductance across an interface, we

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compute the difference in heat flux across the interface according to [35],

$$q''_{1\to2} = \frac{1}{4}\cdot\frac{\Gamma_{12}}{v_{j,1}^2}\cdot\sum_j\int_0^{\omega_m}\hbar\cdot\omega\cdot v_{j,1}^3\cdot f_1(\omega,T_1)\cdot D(\omega)d\omega \quad (7)$$

where $q''_{1\to2}$ is the heat flux from side (or material) 1 of the interface to side (or material) 2 of the interface (W/m^2), $\upsilon_{l,1}$ is the longitudinal speed of sound for material 1 (s), $\hbar$ is Planck's constant (J·s), $f_1(\omega,T_1)$ is the Bose-Einstein distribution for material 1 and $D(\omega)$ is the material density of states. We note that the upper bound of the integral in Eqn. 7 is the cut-off frequency of each phonon branch (where phonon cut-off frequency is related to the Debye Temperature, θ_D, and the Boltzmann Constant, k_B, via $\omega_m = k_B\cdot\theta_D/\hbar$). Additionally, Γ_{12} is represented as,

$$\Gamma_{12} = 2\cdot\int_0^{\pi/2}\tau_{12}\cdot cos\theta_1\cdot sin\theta_1 d\theta_1 \quad (8)$$

where τ_{12} is the transmission coefficient for phonon transport across the interface at a given phonon frequency. The transmission coefficient for the AMM is found according to,

$$\tau_{12} = \frac{4\cdot\rho_1\cdot\rho_2\cdot v_{l,1}^2\cdot cos(\theta_1)\cdot cos(\theta_2)}{\left(\rho_1\cdot v_{l,1}\cdot cos(\theta_2)+\rho_2\cdot v_{l,2}\cdot cos(\theta_2)\right)^2} \quad (9)$$

In Eqns. 8 and 9, ρ is material density, v_l represents longitudinal sound speed and θ represents the incident polar angle for phonons that interact with (i.e. transmit or reflect across) an interface.

One must then compute $q''_{2\to1}$ in order to calculate the net heat flux $q''_x = q''_{1\to2} - q''_{2\to1}$. Given the relationship between heat flux and thermal boundary conductance via Fourier's Law ($q''_x = h_{BD}\cdot\Delta T$, where h_{BD} is the thermal boundary conductance), and operating on a differential basis and in the limit as $\Delta T \to 0$, one obtains,

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$$h_{BD} = \frac{1}{4} \cdot \sum_j \frac{\Gamma_{1,j}}{v_{1,j}^2} \cdot \int_0^{\omega_m} \hbar \cdot \omega \cdot v_{1,j}^3 \cdot \frac{\partial f_{BE,j}}{\partial T} \cdot D(\omega) d\omega \quad (10)$$

The AMM itself is typically reserved for computations of thermal boundary conductance at extremely low temperatures where the thermal phonon wavelengths are long relative to length scales of interfacial asperities (< 7 K [30]).

For most practical applications (particularly those that operate near or above room temperature), the DMM has proven to be more effective when predicting h_{BD}. The DMM assumes that phonon interfacial scattering is diffusive. In this case, phonons that traverse the boundary have no inherent memory of magnitude and direction, and thus repopulation of phonon states can occur within the bounds of the phonon density of states for the opposing material. The DMM makes modification to the transmission coefficient in Eqn. 9, which is represented by [73-75],

$$\tau_{12} = \frac{\sum_j \int_0^{\omega_m} \hbar \cdot \omega \cdot v_{2,j} \cdot f_{BE} \cdot D(\omega) d\omega}{\sum_j \int_0^{\omega_m} \hbar \cdot \omega \cdot v_{1,j} \cdot f_{BE} \cdot D(\omega) d\omega + \sum_j \int_0^{\omega_m} \hbar \cdot \omega \cdot v_{2,j} \cdot f_{BE} \cdot D(\omega) d\omega} \quad (11)$$

A variety of works have been performed to assess the validity of the above model, with variations to the transmission coefficient made to account for a full density of states when necessary (for instance, when the elastic constants at an interface are highly anisotropic [76]). Here, we elucidate the representative magnitude of h_{BD} on the overall thermal resistance of a multilayer system (where we compute the thermal resistance across the interface as $R_{th,int} = 1/h_{BD}$) in the form of a temperature rise in Fig. 7 for GaN/diamond and GaN/Si. In these computations, we assume each layer is 5 μm thick and heat dissipation through the material system is q" = 5 kW/cm^2, consistent with future device-level thermal abatement requirements [77, 78].

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The thermal boundary conductances for each of the aforementioned interfaces are provided in Table 1 alongside experimentally determined values from literature.

Table 1. Thermal boundary conductance (h_{BD}) across GaN/diamond and GaN/Si interfaces computed with the Diffuse Mismatch Model (DMM). DMM computations are compared to experimentally measured h_{BD}s at similar material interfaces.

Interface	DMM h_{BD} ($MW/m^2 \cdot K$)	Experimental h_{BD} ($MW/m^2 \cdot K$)
GaN/Diamond	30.88	24.39 – 58.82 [79]
GaN/Si	35.07	30.3 – 128.21 [80]

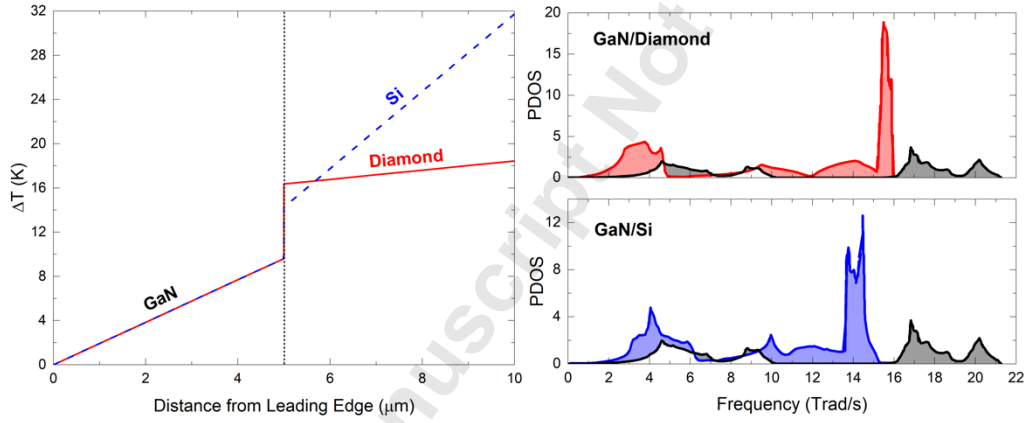

Figure 7: *Left*: Temperature distribution across GaN/substrate stacks, inclusive of the interface (represented by the dotted black line), *Right*: Phonon Density of States overlap between GaN and diamond (top) and GaN and Si (bottom). Units for PDOS are States/THz-Unit Cell.

With little overlap in the phonon density of states (white region of overlap in the right-most plots in Fig. 7) between both GaN and diamond and GaN and Si, the h_{BD} across the interface is expectedly low relative to other material combinations having greater overlap (such as Al/Si, which has a reported h_{BD} of ~ 208 $MW/m^2 \cdot K$ [81]). As a result, there is a large temperature difference across the interface shown in the left-most plot of Fig. 7. Note that we do not account for any grain gradient distribution in either the GaN or

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the diamond and instead assume a constant thermal conductivity through the thickness of each material. As will be discussed, however, many high-throughput growth techniques result in a grain gradient distribution that has significant impacts on thermal conduction through each material. Nevertheless, Fig. 7 demonstrates the importance of considering nanoscale interfacial thermal transport in electronics packaging material systems.

For the remainder of this work, the authors provide the reader with individual perspectives on the impacts of nanoscale thermal transport within and across relevant device features (such as those shown in Fig. 4). Each individual section is titled with individual author contributions, where each author in the manuscript has contributed a perspective (or series of perspectives) that reflect their area of expertise. The collection of contributing authors in this work was established with different elements of Fig. 4 in mind and within the specific context of nanoscale thermal transport.

B. DEVICE-LEVEL NANOSCALE THERMAL TRANSPORT

Mitigation of heat at the device and material level is critical to the successful development of next generation electronics devices. Substantial thermal challenges arise by: a) the selection and growth of materials and b) the interfaces between the active material and the other layers in the device. Perspectives on strategies to mitigate these challenges are presented in the next sections.

B.1. Wide Bandgap Materials for High Power Devices and RF Electronics (Wilson)

The goals of electronic materials development have primarily been focused in two directions: faster switching speed (i.e. higher frequency) [82-84] and higher power [85-90]. In communications [82-84, 91, 92] and computational electronics [11, 13-15], higher

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frequency is desirable, while higher power delivery is desired for electric vehicles [26, 88, 93], industrial and utilities [2, 94, 95], and military applications [96-98]. To move successfully in both directions, the industry must transition away from silicon, and to devices made from wide bandgap materials.

To that end, several materials have been researched to replace silicon as a semiconductor material. However, due to established procedures and architectures in place, and a lack of material that can be readily folded into existing manufacturing capabilities, silicon remains the material most widely used in semiconductor devices [88, 90], despite several important limitations in key properties for performance. These include: maximum electric field strength before breakdown, maximum operating temperature, thermal conductivity, electron mobility, and bandgap [88, 99]. Wide bandgap (WBG) materials (with bandgap greater than 1.5 eV) offer potentially viable alternatives to silicon. Viable alternatives include SiC, GaN-based devices, GaO_x, and diamond-based devices. Performance metrics either substantially surpass or rival those of silicon in each case. Figure 8 depicts a comparison of properties of wide-bandgap materials proposed as alternatives to Si. Data found in Figure 8 are from literature values at room temperature, reported in references [27, 66, 100-113].

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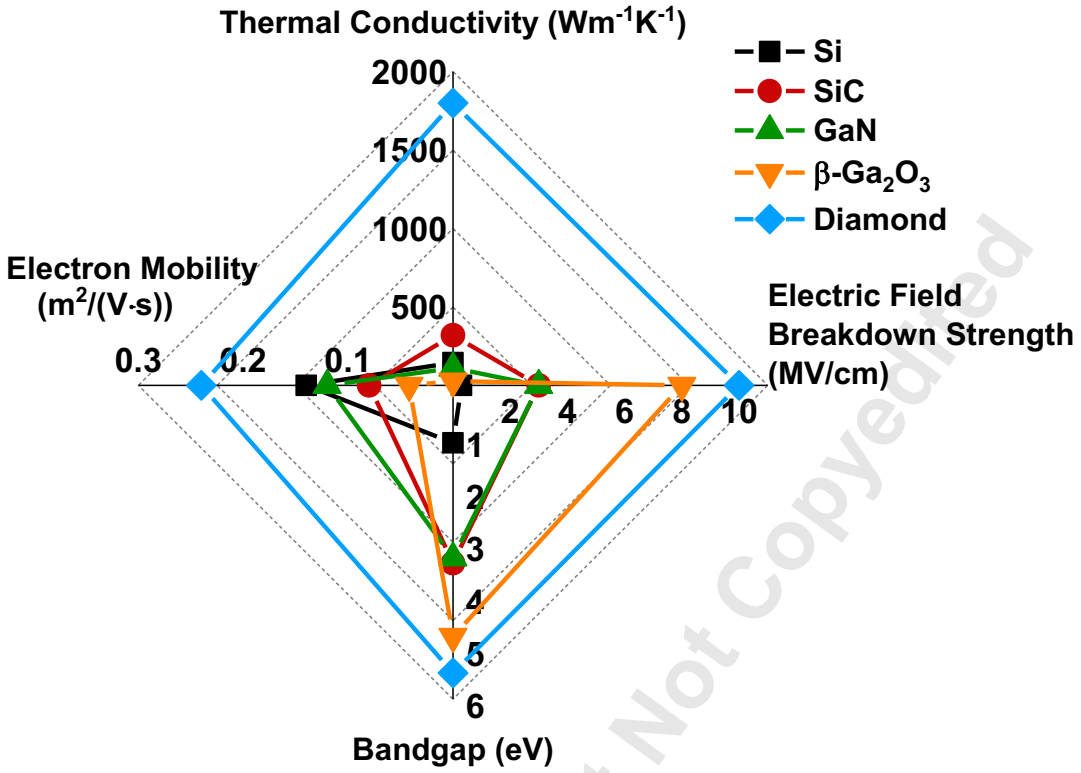

Figure 8. Web plot depicting relative strengths of several WBG electronics options

For each WBG material, the benefits, drawbacks, and current outlook are summarized. Because SiC is a well-understood material, and devices using it are mature technology, currently in use in many commercial products with advantages over Si well-established, discussion on SiC as a WBG material is skipped. For more information on SiC as a WBG material, please read [87].

B.1.i. Diamond

It can clearly be observed that diamond boasts advantage over silicon in every area in Fig. 8. Research has been heavily focused in this area, and recent demonstrations have shown that diamond can be made into an electronic material [43, 66, 102, 104, 114-121]. However, several substantial challenges with production, integration, doping, and contacts

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remain [114, 115]. For many years, diamond was regarded as an excellent choice for passive thermal regulation, but because of high processing temperatures, it was doubtful that it would be useful as an active material [94]. However, as recently as 2018, it has been shown that diamond can be made as a robust active material, with excellent electron and hole mobility [94]. Terminating the diamond with hydrogen allows for a 2-dimensional hole gas (2DHG) to form, significantly boosting maximum current (from ~1 mA/mm to ~100 mA [94]). However, it is difficult to control doping levels and device performance for both n-type and p-type diamond [94, 116]. This may potentially be remedied by hybridizing WBG materials to achieve high power, high frequency devices [122, 123].

Thermal conductivity is routinely touted as a superior characteristic of diamond, boasting a value of over 2000 $Wm^{-1}K^{-1}$[124]. However, in practice, diamond grown by chemical vapor deposition (CVD) or epitaxy is susceptible to significantly varying thermal properties in-plane versus cross-plane. While thermal conductivity is extremely high within a grain (~1800 $Wm^{-1}K^{-1}$ [66]), diamond grown by CVD tends to form a seed layer as the film begins growth. This leads to significant phonon scattering at the grain boundaries, reducing the thermal conductivity in the direction perpendicular to grain boundaries by nearly a factor of four (to ~500 $Wm^{-1}K^{-1}$) [102]. Also, due to expense, diamond is typically grown in thin-film form. Due to diamond's extremely large phonon mean free path, size effects play a significant role, even at high temperatures. Donovan & Warzoha theorize that 50nm diamond films will have thermal conductivity less than 100 $Wm^{-1}K^{-1}$ [125]. Thermal conductivity of doped diamond is also significantly reduced compared with pristine diamond; boron dopants with $>10^{19}$ concentrations have been shown to lead to thermal conductivity values of only 700-1200 $Wm^{-1}K^{-1}$ at room

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temperature [126, 127]. The literature is surprisingly sparse on thermal conductivity of doped diamond and hydrogen-terminated diamond, and this is a point of concern. Since diamond's ultra-high thermal conductivity hinges on its large phonon mean free path, it is critical to characterize the effect of adding dopants or altering termination bonds on the thermal conductivity of diamond.

Overall, the outlook on diamond electronics is quite promising. Given the progress made in the field in very recent years, diamond is well-poised to emerge as the best option among WBG semiconductors to advance power and RF electronics.

B.1.ii. Ga_2O_3

Gallium oxide (β-Ga_2O_3) has recently garnered significant attention as a WBG material, owing to its low cost, wide bandgap (4.7 eV), and advantageous electrical performance properties compared with other WBGs and especially silicon [128, 129]. Compared with Si, SiC, and GaN, β-Ga_2O_3 is projected to be much more efficient and have a much higher electric field break-down strength [130], and is thus potentially ideal for high-voltage applications.

However, β-Ga_2O_3 has relatively low electron mobility (~4.67x lower than Si), and is therefore not well-suited for high-frequency applications. Perhaps the most substantial issue with β-Ga_2O_3 is that it significantly lacks ability to conduct heat. Thermal conductivity in β-Ga_2O_3 is highly anisotropic, and is significantly lower than other WBGs and Si (~27 $Wm^{-1}K^{-1}$ in the (001) direction and ~12 $Wm^{-1}K^{-1}$ in the (100) direction)[103]. Proponents of β-Ga_2O_3 suggest that thermal conductivity matters less for β-Ga_2O_3 than other WBG materials due to substantial enhancements in efficiency, temperature stability,

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and maximum temperature operation [130]. However, devices will generate heat as they operate, and that heat will need to be dissipated, which β-Ga_2O_3 is not well-equipped to do. Interestingly, β-Ga_2O_3 shares many of the phonon scattering characteristics of GaN, which has around ten times larger thermal conductivity [131]; however, three-phonon scattering processes dominate in β-Ga_2O_3, leading to a much shorter phonon relaxation time, which manifests as a significant reduction in thermal conductivity. To mitigate this issue, β-Ga_2O_3 has been applied to higher thermal conductivity substrates (such as diamond) [132]. However, the interface thermal resistance between β-Ga_2O_3 and diamond, as well as between β-Ga_2O_3 and metal have been found to be quite large [132, 133]. This is attributable to differences in the phonon density of states between β-Ga_2O_3 and the other materials. Recently, it was demonstrated that by adding a carefully selected interlayer, thermal boundary conductance between metal and β-Ga_2O_3 can be significantly enhanced, by more than 10x [133].

The outlook on β-Ga_2O_3 is promising; however, thermal challenges will be a significant barrier to realization in a commercial device. The path to successful integration in high power electronics will be through thin layers of β-Ga_2O_3 on interfaces that have been engineered to enhance phonon transport, thereby mitigating the deleterious effects of the poor thermal properties of the material itself.

B.1.iii. GaN

GaN is exceedingly attractive for the manufacturer, especially for high voltage operation, and high switching frequencies. These devices are capable of operating at high voltage and high frequency by nature of the two-dimensional electron gas (2DEG) that is

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formed between the typical AlGaN layer deposited on GaN. This 2DEG forms due to spontaneous polarization of GaN, as well as a large discontinuity in the conduction band between the GaN and AlGaN layers. The properties of the 2DEG change significantly in the presence of electric fields. Electron mobility is extremely high for AlGaN/GaN heterostructures (>2000 $cm^2/(V \cdot s)$) [134]. There are several other practical benefits to using AlGaN-based devices as well including current density [134], boost in switching frequency [88], etc. However, the early developers of these devices did not consider thermal properties (particularly thermal resistance added at heterogeneous material interfaces) among the most important concerns. Since bulk GaN has thermal conductivity comparable to Si, substrate thermal conductivity is a severely limiting factor. Because of this, GaN device layers are frequently removed from substrate and attached to substrates of higher thermal conductivity (or grown on substrates other than Si or sapphire) [135].

Recent studies have shown that the thermal boundary resistance at heterogeneous material interfaces (especially between active material and substrate) may account for a substantial portion of the overall device thermal resistance [136-139]. Graham, et. al., have reported values recorded by them and others [137, 140-142] of GaN-based devices on various substrates and find that although substrate thermal conductivity may be vastly improved by replacing Si with SiC or diamond, interface thermal resistance may take a hit (going from a record low of 1.5 to 2 m^2K/GW for GaN on Si to ~10-100 m^2K/GW for GaN on diamond [115, 119, 143]).

Although much attention has been given to the interface between GaN and the substrate, very little attention has gone into investigating the thermal resistance that occurs between the active layers in the device and the metallization, or even the interface between

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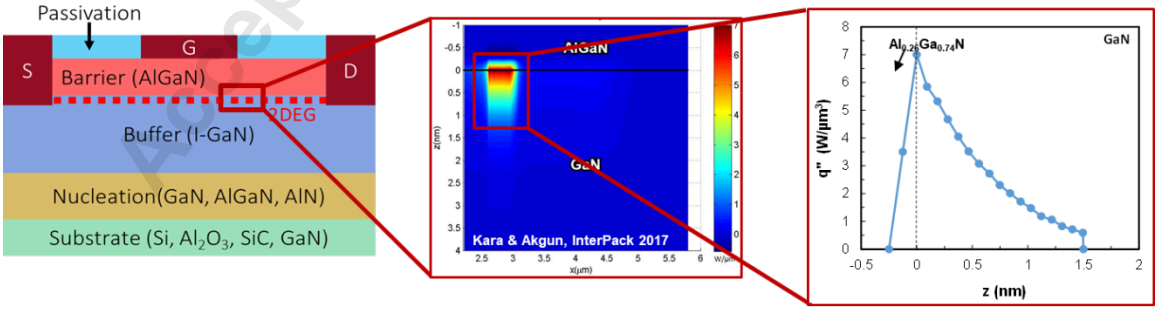
AlGaN and GaN, where the 2DEG forms. Several recent studies have proposed methodologies for probing the peak device temperature, using a combination of thermoreflectance and Raman temperature measurement techniques [144, 145]. In conjunction with multi-scale finite element and molecular dynamics models, accurate determination of the peak temperature rise in the devices for a given measured temperature rise at the surface or of the volume may be inferred [144, 146]. However, owing to the interfaces that are necessary to make a device with AlGaN on GaN, the overall thermal resistance of the devices increases, leading to peak temperature rise of up to 42% over the case where the interface is perfectly thermally conductive.

Figure 9 depicts this, based on a combination of 3DFE simulations from a phonon hydrodynamic model, and experimental measurements of the AlGaN/GaN interface via FDTR [147]. Therefore, in power electronics, material properties as well as properties of material interfaces are critically important to the development of better devices. Thermal resistance in multi-layered structures leads to significant build-up of peak temperature, while bulk thermal conductivity is the limiting factor when using substrates with lower thermal conductivity. In both cases, processing conditions, functionalization, and careful selection of interstitial layers will allow for optimal thermal performance of wide-bandgap devices to be used in power and RF electronic devices.



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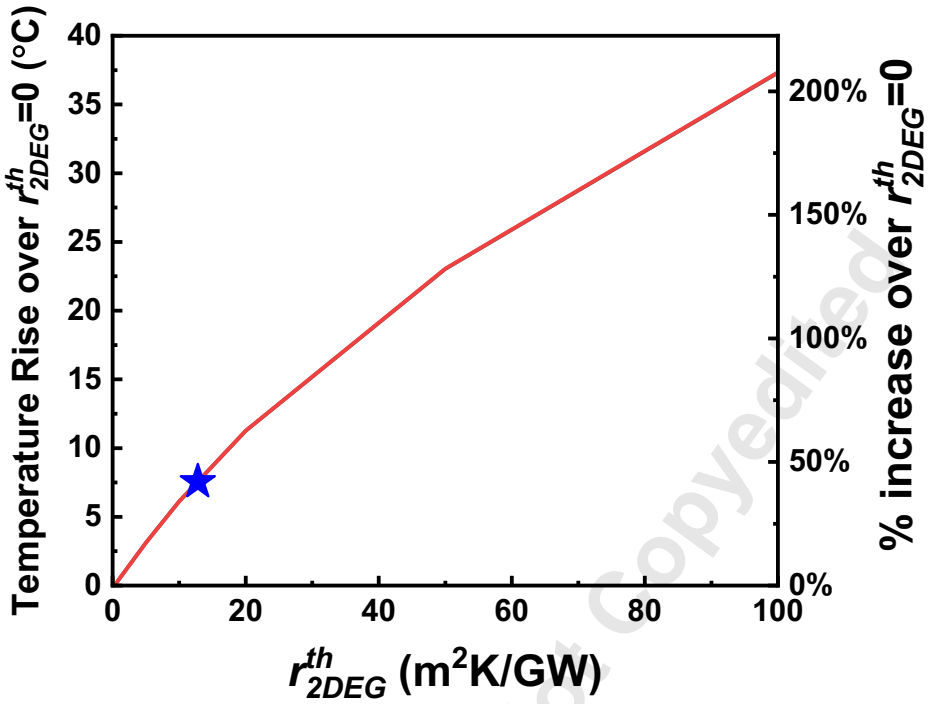

Figure 9. Effect of AlGaN/GaN interface on peak temperature in AlGaN/GaN HEMTs. Adapted from [147]with permission, ©2019 IEEE.

B.2. Nanoscopic heat flow constriction in wide bandgap (WBG) electronics (Choi)

5G wireless networks offer significant advantages over the current 4G technology, including higher speed and lower latency, suitable for serving as the backbone of the Internet of Things (IoT), connecting more than a trillion devices to the internet. However, in order to compensate for the increased energy and range demands arising from the network growth, significant improvement in the energy efficiency of base stations is necessary[83]. Approximately 60% of the total power consumption of base stations is attributed to the loss associated with radio frequency (RF) power amplifiers[91].

Gallium nitride (GaN)-based radio frequency (RF) power amplifiers, that feature broadband operation and high efficiency, are key components to realize 5G network base stations and small cell applications including mobile devices[82, 84]. However, the last

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piece of the puzzle to enable GaN for 5G is to overcome thermal reliability concerns stemming from localized extreme temperature gradients beyond predictions based on macroscale heat transfer principles such as Fourier's law of heat conduction.

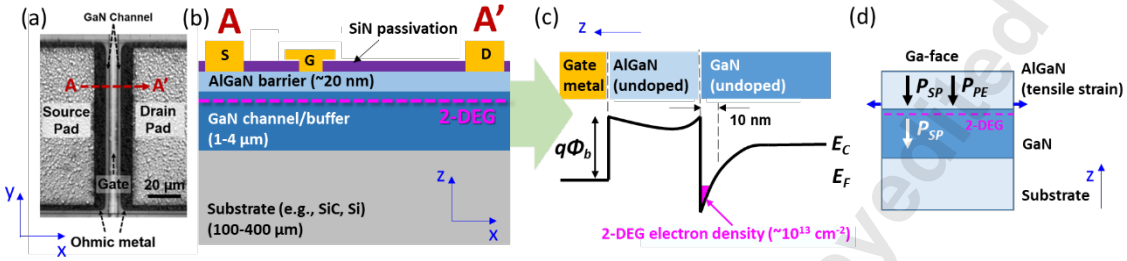

Fig. 10. (a) Top view and (b) cross-sectional structure of a GaN HEMT. (c) Conduction band (E_C) bending near the AlGaN/GaN heterointerface forms a quantum well below the Fermi level (E_F) and 2-DEG[148]. (d) Spontaneous (P_{SP}) and piezoelectric (P_{PE}) polarization effects result in massive electron accumulation in the quantum well[149].

Fig. 10 (a) and (b) show the structure of a GaN-based high electron mobility transistor (HEMT)[89, 150-154]. To construct the device, a 1-4 μm thick GaN layer is heteroepitaxially grown on a non-native substrate where the common choices are silicon (Si) and silicon carbide (SiC) substrates. Subsequently, a thin (~20 nm) aluminum gallium nitride (AlGaN) layer is pseudomorphically grown over GaN. A physical effect that governs the device behavior is the formation of a two-dimensional electron gas (2-DEG)[149] which serves as the current channel. The 2-DEG is an electron aggregate that is free to move in two dimensions (x- and y-directions in Fig. 10), but tightly confined in the third dimension (z-direction). Accumulation of the high density 2-DEG without impurity doping is due to the formation of a deep spike-shaped quantum well at the AlGaN/GaN heterointerface, where there is a large conduction-band offset (Fig. 10 (c)). A vast amount of electrons are drawn into the quantum well due to the large piezoelectric polarization induced via tensile strain built in the AlGaN layer (Fig. 10 (d)). This translates

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into a large current-carrying capability between the drain and source electrodes compared to conventional devices[149, 155]. The current level can be modulated (reduced) by applying a negative gate voltage to partially deplete the 2-DEG channel. The wide band gap (E_G=3.4 eV) of GaN results in a breakdown field of ~3 MV/cm which is an order of magnitude larger than that for conventional materials that have been used to build RF power amplifiers. This enables higher voltage operation with a smaller device footprint.

The power amplifier's role is, as the name suggests, to convert a small input signal (e.g., the gate voltage of a transistor) into a much larger power (current×voltage between the drain and source electrodes) to be delivered to the load. Therefore, GaN HEMTs, when employed as RF power amplifiers, offer high power density (=current×voltage/active area), power added efficiency, gain and ease in impedance-matching that significantly improves the overall efficiency in the RF chain. Moreover, the ability of GaN transistors to work in the high-frequency range gives promise for them to evolve from 5G base stations to small cell applications and, potentially into mobile devices.

However, this substantial improvement in size, weight, and power translates into extreme power densities (>50 kW/cm^2) in the active region of GaN HEMTs as shown in Fig. 11[92, 156]. Thermal failure (Fig. 11 (b)) and reduced component lifetime[157, 158] caused by device self-heating are major roadblocks to the successful implementation of GaN technology into 5G network components. Intense channel temperature rise caused by high voltage and power operation[159] was shown to trigger and aggravate various degradation mechanisms[160-164]. Such failure mechanisms include mechanical damage in the AlGaN barrier due to induction of thermo-elastic stress[159] and thermally-assisted inter-diffusion at the semiconductor/metal interface[165]. Although GaN HEMTs have

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been commercialized for small-scale applications (e.g., laptop chargers), questions regarding GaN device thermal reliability remain unanswered[166, 167], as evidenced by the continued research into their life expectancies[157, 168, 169].

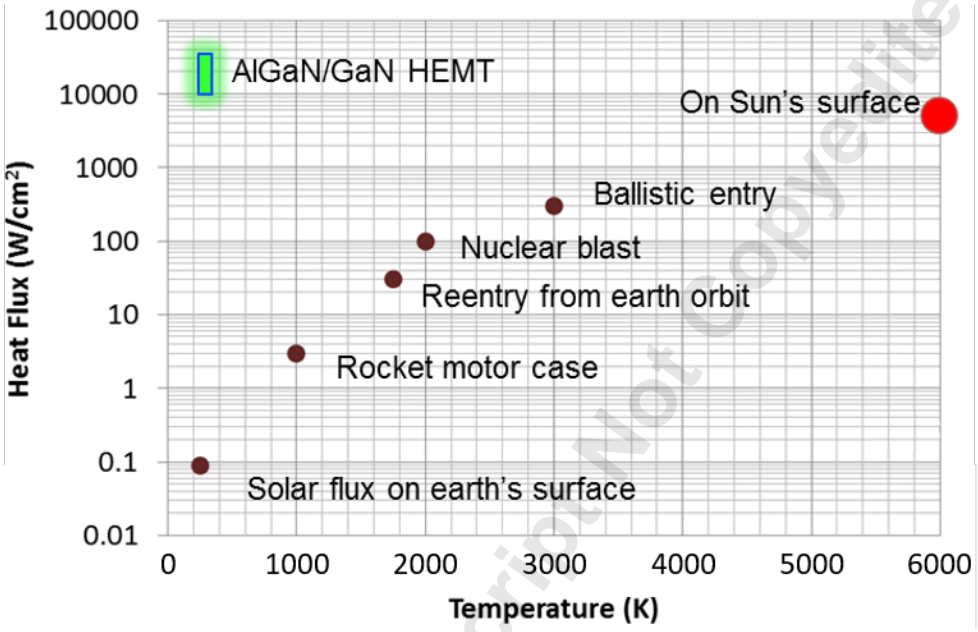

Figure 11. GaN HEMT heat flux challenge.

The industry-standard method to estimate GaN HEMT lifetime is the temperature-accelerated direct current operational-life test[170]. The Arrhenius extrapolations reported in the literature[157, 169] show extremely long predicted median times that significantly over-predict the actual device lifetime in field applications. This is a major concern in industry because such false prediction may lead to catastrophic events in reliability-critical applications[157, 168, 169]. The over-prediction of device lifetime stems from inaccurate estimation of the device peak temperature at the site of degradation/failure during the accelerated high power testing. It was shown that an error of only 2°C in the estimation of

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device peak temperature used in the temperature-accelerated life test can skew the predicted lifetime by a factor of two[166, 167].

Currently, industrial practices for device thermal analysis and accelerated direct current operational life tests[157, 169] rely on simulation data based on the simple and widely accepted Fourier's law of heat conduction. However, a limited number of pioneering theoretical studies[170-174] have suggested that a nanoscale temperature spike or a so-called "hot-spot" forms in GaN HEMTs, which can be significantly hotter than predictions based on purely diffusive thermal transport models (i.e., the Fourier's law of heat conduction). This unanswered question has inhibited the use of GaN devices for high power RF applications where demonstrated long product lifetimes are required[158, 175].

In practice, large voltages are applied between the drain and source (e.g., V_{DS}=28-48 V) of GaN RF power amplifiers to reduce or eliminate the need for step-down voltage conversion to match the operating voltage of commercial systems (e.g. wireless base station)[176]. In addition, the wide bandgap of the material allows the use of considerably shorter channel lengths (several microns) than conventional devices. This results in considerable electric field concentration within the 2-DEG channel underneath the drain side corner of the gate[177].

Fig. 12 shows heat generation profiles of a GaN HEMT under two different bias conditions resulting in an identical total power dissipation (e.g., $P_{DISS}=V_{DS}\times I_{DS}$=500 mW; P_{DISS}, V_{DS}, and I_{DS} stand for dissipated power, drain-source voltage, and drain-source current, respectively). Fig. 12 (a) shows the Joule heating is highly concentrated beneath the drain end of the gate for high voltage-low current conditions (e.g., V_{DS} = 50 V, V_{GS} = -1 V, I_{DS} = 10 mA). On the other hand, Fig. 12 (b) shows that a relatively uniform Joule

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heating distribution occurs for low voltage-high current conditions (e.g., V_{DS} = 5 V, V_{GS} = 2.5V, I_{DS} = 100 mA). For low voltage-high current conditions, the lower V_{DS} produces the same amount of power dissipation (500 mW) since the channel is fully open (manifested by a large I_{DS}). The 2-DEG current flow is not constricted, causing the heat generation profile to be relatively uniform across the entire channel. In contrast, for high voltage-low current conditions, to accomplish an identical power dissipation, I_{DS} is restricted by applying a negative voltage on the gate (V_{GS}), thereby forming a local depletion region that partially pinches off the channel. This local depletion region with high electrical resistance causes spatial confinement of the 2-DEG Joule-heating. This leads to formation of a nanoscale hotspot[170, 172-174] subject to extreme local heat flux (>1 MW/cm^2). According to fully-coupled electro-thermal simulation[158, 175, 178] shown in Fig. 12 (a), the domain size of the peak heat generation zone can be less than 10 nm×50 nm which is in agreement with theoretical predictions in literature[172, 179].

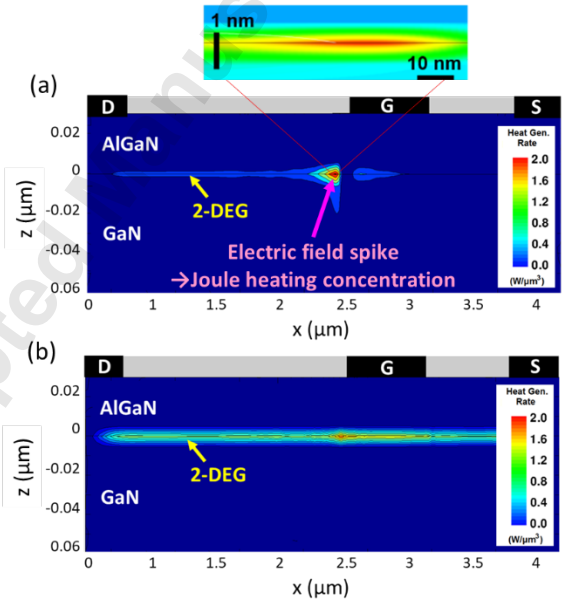

Figure 12. (a) Nanoscale spatial confinement of the heat generation zone under a high voltage-low current condition. (b) Uniformly distributed heat generation occurs under low voltage-high current open channel conditions.

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The thermal conductivity of solids can be resolved as a function of phonon mean free path[180] via a thermal conductivity accumulation (k_{accum}) function:

$$k_{accum}(\Lambda, T) = \sum_{s} \int_{0}^{\Lambda^*} \frac{1}{3} c(\Lambda, T) \cdot v(\Lambda, T) \cdot \Lambda(T) d\Lambda \tag{12}$$

where Λ is the phonon mean free path, T is the temperature, c is the volumetric heat capacity per unit phonon mean free path, v is the phonon group velocity, and s indexes the phonon polarizations (i.e., different vibrational modes). Since the integral is defined from 0 to Λ^*, k_{accum} quantifies the contribution of phonons with a mean free path less than Λ^* to the overall bulk thermal conductivity.

The thermal conductivity accumulation function of GaN[181] indicates that phonons with Λ less than 550 nm and 1000 nm contribute to ~50% of the bulk thermal conductivity of GaN at T= 415 K and 309 K, respectively. At higher temperatures, the larger phonon population results in more frequent phonon-phonon scattering events which reduce the effective mean free path of the principal heat carriers (i.e., phonons).

Under high voltage-low current operation (Fig. 12 (a)), because of the extreme heat source size reduction, heating would take place primarily over length scales less than the mean free path (MFP) of phonons tasked with energy delivery. As mentioned above, phonons with mean free paths greater than ~550 nm are responsible for more than 50% of the thermal conduction in the GaN lattice at ~400 K[182, 183]. Therefore, within the nanoscale heat source domain (< 50 nm), the opportunity to effectively transport energy away via phonons with longer mean free paths (> 550 nm) is lost, i.e., the onset of ballistic transport occurs. Thus, this nanoscopic "heat source size effect" will restrict thermal

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transport from the device hot-spot causing a net increase in channel temperature beyond predictions based on Fourier's law.

A recent study[184] has investigated the self-heating behavior of a GaN HEMT fabricated on a Si substrate operating under high V_{DS}-low I_{DS} conditions that are expected to cause non-Fourier thermal transport. A near-ultraviolet (UV) thermoreflectance imaging technique and a coupled 3D electro-thermal model[178] that accounts for ballistic-diffusive thermal transport effects were used to study amplified heating beyond predictions solely based on the Fourier's law of heat conduction.

Temperature measurement of the device channel was performed using a near-UV illumination source with a center wavelength of 365 nm. Results are shown in Fig. 13 (a). The diffraction limited lateral spatial resolution was 300 nm. Since absorption is strong near the GaN surface for near-UV illumination, the measured temperature was weighted toward the 2-DEG channel region, within ~55 nm[185-189] from the GaN surface. The coupled electro-thermal modeling scheme was similar to that in [158, 167, 178] but was extended to three dimensions. This device model was developed to validate the near-UV thermoreflectance results. The coupled modeling scheme self-consistently solved, for each mesh point, the Poisson, current continuity, and electro-hydrodynamic equations (for electronic transport), and the Boltzmann transport equation (BTE)[170, 172] (for thermal transport) to derive the electrostatic potential, electron/hole concentration and their energy/temperature distributions, heat generation, and electron/hole/lattice temperature rise. Consequently, the model accounted for the nanoscopic heat source size effect.

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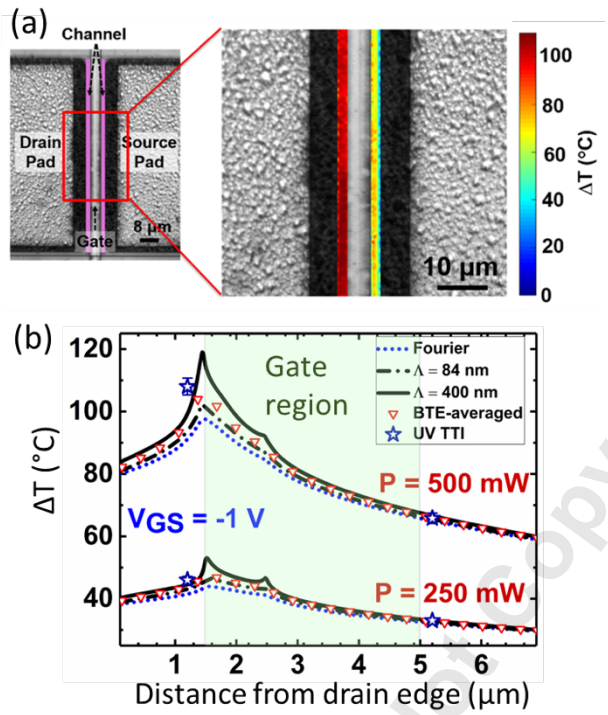

Figure 13. (a) Near-UV thermoreflectance temperature map of a device channel for V_{DS}=45 V, V_{GS}=-1 V, and P_{DISS}=500 mW. (b) Comparison of temperature profiles across the 2-DEG channel obtained by near-UV thermoreflectance, Fourier- and BTE-based simulation. Images were adapted from [184].

Channel peak temperatures were deduced from experiments and modeling for multiple bias conditions. Results are displayed in Fig. 13 (b). Measurement, Fourier-, and BTE-based simulation shown excellent agreement for low to moderate V_{DS} bias conditions for all tested power dissipation levels. In stark contrast, a large disagreement (>10%) in channel peak temperatures between the Fourier and BTE simulation results was observed for high V_{DS} conditions, for all tested power dissipation levels (Fig. 13 (b)). Moreover, experimental values shown excellent agreement with the simulated temperature profiles from the BTE gray model reflecting the mean free path spectra of GaN acoustic phonons[170, 183, 190-193]. Results of this study clearly suggest that non-Fourier thermal transport mechanisms are in play, leading to the observed amplified heating. Many laser-based pump-probe

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experiments[181, 194-200] support this experimental study. They have demonstrated that under conditions where the heat source domain size is less than the mean free path of dominant heat carriers, the heat source region exhibits a local reduction of the effective thermal conductivity compared to the bulk value.

B.3. Gallium Oxide: A Promising Ultra-wide Bandgap Material (Donmezer)

A new and exciting group of materials emerging within the electronics community is the ultra-wide bandgap (UWBG) materials. These materials, such as AlN, diamond, cubic BN and Ga_2O_3 (with bandgaps that exceed 3.4 eV), have the potential for superior performance relative to conventional and wide band-gap materials such as GaAs and GaN. Devices fabricated from these materials are still immature due to a variety of fabrication challenges and material performance limitations. The absence of readily available large-area, low-defect density, single-crystal substrates and doping control issues remain fabrication challenges for the commercialization of AlGaN/AlN and diamond based electronic devices. Despite these problems, researchers fabricated functioning electronic devices such as diamond [201] and AlN/AlGaN field effect transistors [202-204] as shown in Fig. 14.

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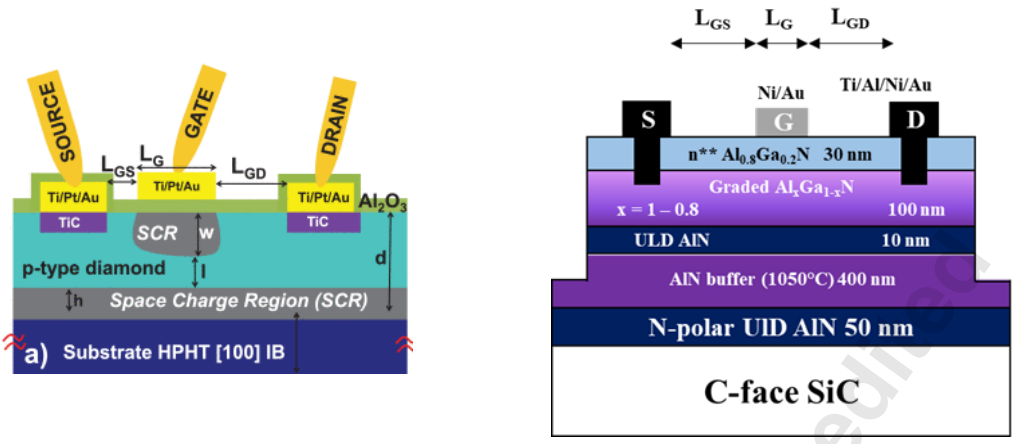

(a) (b)

Figure 14: Schematic of (a) diamond (recreated from [201]) and (b) AlGaN/AlN (recreated from [204]) field-effect transistors.

Among all UWBG materials, β-Ga_2O_3 is the most promising one since low-cost and large substrates are available for its growth [205]. β-Ga_2O_3 power devices are poised to reach the commercial sector with performance rivaling or surpassing that of GaN and SiC devices at much lower cost.

Although not investigated in detail, thermal problems observed in high-power devices are also present. Similar to AlGaN/GaN HEMT transistors and Si MOSFETs, these devices experience reliability issues associated with localized heating in their active areas. Thermal transport from the active areas is controlled by the thermal conductivity of each material and the thermal boundary conductance (h_{BD}) between individual material layers. Epitaxial material layers can have thicknesses varying between tens of nm (as in Fig. 14) to a few μm. Thus they often have thermal conductivities smaller than their bulk counterparts due to thin film size effects. Diamond, which has a much larger bulk thermal conductivity than most other substrates due to longer phonon mean free paths, suffers as a result of these size effects to an even greater extent. Alloy semiconductor layers such as AlGaN with low thermal conductivity due to additional phonon scattering events caused

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by the alloy particles also requires special attention. h_{BD} between material layers caused by the significant lattice mismatch can also play a significant role in heat transfer.

To design better performing devices, accurate thin film thermal conductivities and h_{BD}s obtained via experimental and/or theoretical approaches should be used for thermal characterization studies. Bulk β-Ga_2O_3 has low thermal conductivity (k = 15 W/m·K) and is doped in most of its functioning devices. Moreover, its thickness is often in the range of hundreds of nanometers. These factors may lead to further reduction in thermal conductivity in accordance with the physics presented within the Introduction (*Nanoscale Thermal Physics*). In the past, thermal conductivities of doped and undoped bulk and thin film β-Ga_2O_3 samples were measured at different temperatures using techniques such as 3ω and time domain thermoreflectance (TDTR) [206-208]. Thermal conductivities of 300 – 1000 nm thick AlN thin films obtained using 3ω technique are measured to be between k = 5.4 – 17.7 W/m·K [209]. Moreover, phonon thermal conductivity - mean free path spectra of UWBG materials obtained through experimental and theoretical approaches can be used the predict size dependence of thermal conductivity [181, 210]. Finally, the h_{BD}s between β-Ga_2O_3/diamond[132], β-Ga_2O_3/metal [133], and AlN/AlGaN [211] interfaces have been obtained using a variety of experimental and theoretical approaches. These findings generally show that the already low thermal conductivity of UWBG materials is further reduced in their thin film form; when combined with the low h_{BD} between these materials and their substrates, a thermal bottleneck can form and result in inadequate heat dissipation. Consequently, the impacts that nano-sized features have on thermal transport within the device and at its boundaries should be considered carefully in device analysis.

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With the help of accurate thermal conductivities and h_{BD}s, thermal characterization of devices can be performed through simulations to analyze device temperatures and provide relevant metrics for thermal solutions. Past attempts have used anisotropic thermal conductivities of Ga_2O_3 (though ignored the impact of potentially high h_{BD}s) to analyze MOSFET and MESFETs through electro-thermal simulations[212-214]. Although this remains an area under active investigation, results from previous studies highlight the importance of non-uniform Joule heating distribution and its effects on temperature, as shown in Fig. 15. Non-uniform heating distribution is also observed near Schottky junction of β-Ga_2O_3 diodes [215], in MISFETs with h-BN gate insulators [216], and expected in vertical FinFETs [217].

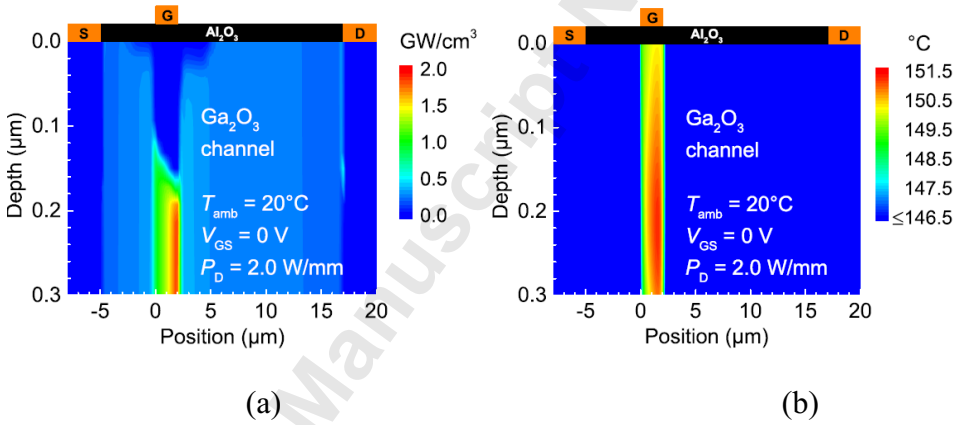

Figure 15. Simulated (a) lattice temperature and (b) heat power contours in the β-Ga_2O_3 MOSFET [212].

Electro-thermal simulations of devices are mainly performed with commercial electrical device simulators (i.e. ATLAS, Sentaurus, Silvaco etc.) which solve Fourier's heat diffusion equation to obtain temperature distribution in devices. Yet, when the heat is localized, heat transfer becomes partially ballistic in these regions. When this is the case Fourier's heat diffusion equation is no longer valid. Even though one can use size dependent thermal conductivities for material layers it won't be sufficient to characterize

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the thermal transport in localized hotspots. To obtain accurate temperatures profiles, ballistic-diffusive effects should be considered by solving the phonon Boltzmann Transport Equation (BTE) [170]. The gray phonon BTE is expressed by:

$$\nabla \cdot \left(v_g \vec{s} e\right) = \frac{e^0 - e}{\tau} + q''' \tag{13}$$

where e is the integrated energy density found by integrating the phonon energies along all frequencies and polarizations, q''' is the volumetric heat generation term that represents the Joule heating of the device, τ is the relaxation time, v_g is the phonon group velocity, and $\vec{s}$ is a unit vector pointing in the direction of the phonon group velocity [218].

Therefore, Joule heating distribution, ballistic-diffusive heat transport near hotspots, thin film thermal conductivities, and h_{BD} values should all be considered for accurate device simulations, and highlights the importance of nanoscale energy transport considerations for thermal management of high-power electronic devices. Additionally, accurate representations of the device geometry and its peripheral components with an appropriate 3D model and the proper selection of thermal boundary conditions is critical to understanding such impacts on device performance. Therefore, the development of multiphysics and multiscale simulation techniques with reasonable computational cost is crucial for the development of next-generation UWBG devices.

C. NANOSCALE ENERGY TRANSPORT ACROSS BONDED INTERFACES

The performance of high power electronics, thermoelectrics, phase change memory, and logic circuits are frequently limited by the thermal boundary resistance (R_{th}) at interfaces of devices [219, 220]. These interfaces are designed to optimize the electrical

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performances without considering thermal management at the same time. As characteristic length- and time-scales become comparable to the mean-free-paths and lifetimes of energy carriers in materials and devices, thermal resistance associated with interfaces between solids can become a major impediment and may lead to thermal breakdown of devices if heat cannot be dissipated efficiently [221]. R_{th} is sometimes comparable to (or even larger than) the thermal resistance of materials, thus contributing significantly to the overall resistance of the whole device. Therefore, increasing thermal boundary conductance ($h_{BD}=1/R_{th}$) is necessary in order to maintain reasonable device temperature to avoid thermal breakdown.

For typical crystalline interfaces where heat transfer is primarily driven by lattice vibrations, typical values of measured h_{BD} are in the range of ~20 to 300 MW/m^2·K ($R_{th} \approx 3.3 \cdot 10^{-9}$ to $50 \cdot 10^{-9}$ m^2·K/W). In addition to the fundamental properties of the energy carriers in the two solids, interfacial resistance also depends on a variety of other factors such as temperature, interfacial disorder, roughness and dislocations at the interface, and weak interfacial bonding. Experimental and simulation approaches to further understand these effects at interfaces are presented in the following sections.

C.1. Nanoscale Interfaces (Giri, Hopkins)

The understanding of the various factors dictating h_{BD} has been greatly facilitated by recent advancements in experimental metrologies used to measure h_{BD} across buried interfaces or interfaces comprised of 2D material systems and computational advances in atomistic simulations that can mimic realistic interfaces. For example, it has been shown that interfaces formed with an amorphous solid can have very high interfacial conductances (Fig. 16), which is counterintuitive to the conventional wisdom that disorder usually

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enhances thermal resistance [222, 223]. Likewise, electron-dominated thermal transport across interfaces (usually between two metals in contact, with interfacial thermal conductance typically on the order of 1 GW/m^{2}K) have been shown to possess more than an order of magnitude higher conductances than typical phonon-dominated heat flow (on the order of 100 MW/m^{2}K) across interfaces [224-226]. Moreover, epitaxial interfaces formed between materials with similar lattice constants and high quality of interfaces have also been shown to demonstrate high conductances (h_{BD} > 500 MW/m^2·K) [227-229].On the contrary, extremely low conductances have been measured for materials with highly dissimilar vibrational density of states and large mismatch in their elastic constants such as bismuth deposited on diamond substrates with reported h_{BD} of 8 MW/m^2·K. To put things into perspective and highlight the disparity in the measured h_{BD}, the resistance of bismuth/diamond interface is greater than that of a 100 nm thick amorphous SiO_2 layer, whereas the resistance measured for a TiN/MgO epitaxial interface is comparable to that of a 1 nm thick amorphous SiO_2 layer.

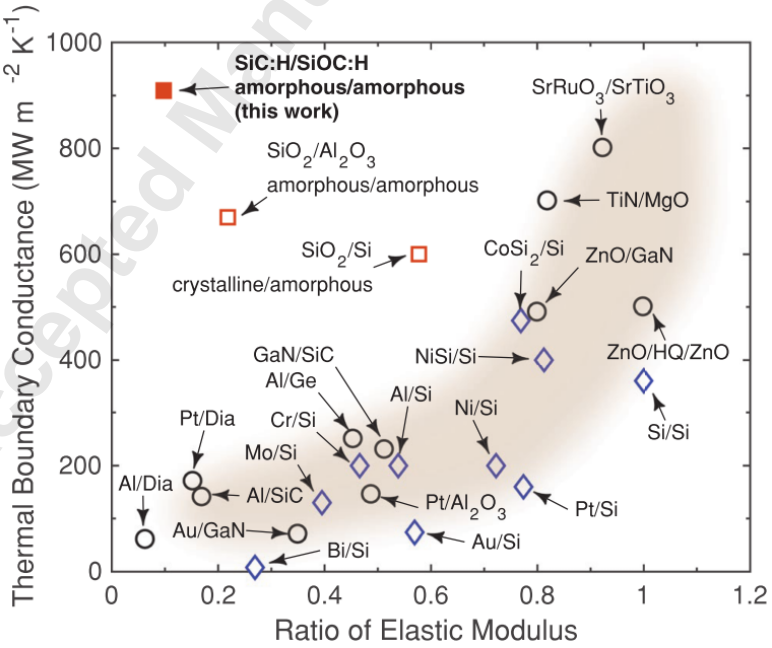

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Figure 16 - Compilation of experimental data showing conventional trend in thermal boundary conductance vs ratio of elastic modulus, showing it is possible to achieve higher thermal boundary conductance by matching to amorphous layers. Reproduced from [223] with permission.

Extrinsic factors such as pressure and nanostructuring through interfacial mixing, roughing with non-planar structures, and chemical functionalization has been shown to control and enhance h_{BD} in a wide range across various types of interfaces [230-241]. For example, Losego et al. [240] experimentally demonstrated that interfaces formed with weak van der Waals interactions can be converted to covalent bonding via self-assembled monolayers (SAMs) between Au and quartz, leading to an increase in h_{BD} by as much as 80%. Similarly, increase in the overall contact area by patterning nonplanar features of nanofabricated fin-like projections at metal/dielectric interfaces can substantially increase the measured h_{BD} [230, 231]. Stiffening the bonds at the interface via mechanical strain (performed with diamond load cells) has also been experimentally shown to be an effective way to enhance h_{BD} [119, 242]. These strategies for enhancement in thermal conductance are summarized in Fig. 17.

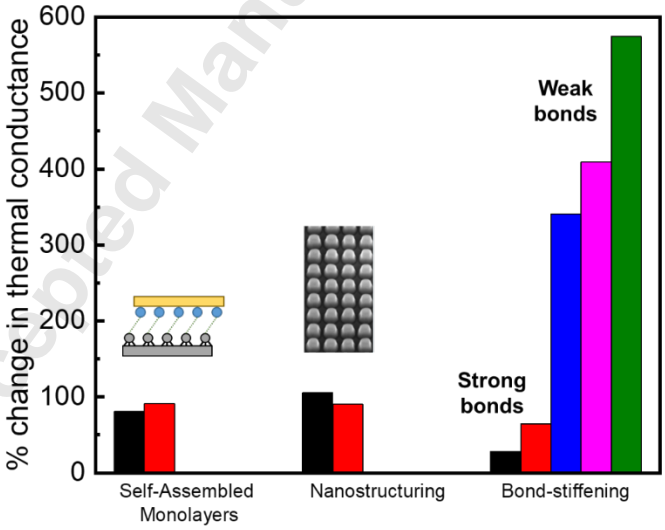

Figure 17 - % change in thermal conductance between the high conductance case and the low one, demonstrating that several strategies have significant impact on h_{BD}. Data on tailoring h_{BD} via self-assembled monolayers comes from [240, 241]; nanostructuring data is from [230, 231]; bond-stiffening data is from [119, 242].

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Along with the experimental advances, atomistic simulations based on molecular dynamics (MD) simulations have led to tremendous progress in understanding the mode- and spectral-level contributions to interfacial thermal conductance between materials[23, 118, 243-249]. Some of these works have highlighted the importance of considering localized and nondispersive interfacial modes to accurately describe h_{BD}, which are ignored while treating h_{BD} with the typical formalisms based on the phonon gas models such as the DMM and AMM as discussed above. Furthermore, the assumption of elastic scattering in the aforementioned models that hinder their applicability to realistic material interfaces at room temperature and elevated temperatures is avoided in MD simulations that inherently account for elastic as well as inelastic pathways of heat transfer due to multiple phonon interactions that can play a significant role in dictating interfacial heat transfer across solids.

The failure of the phonon gas models has also been exemplified by comparing their predictions with experimental measurements of h_{BD} on high crystalline quality nonmetallic solids as carried out in [229] for epitaxially grown ZnO/GaN interface (Fig. 18). This work directly highlights the inapplicability of the Landauer/transmission formalism-based theories by showing that the measured value of h_{BD}=490 MW/m^2·K for ZnO/GaN is nearly a factor of 2 greater than the values predicted by these theories at elevated temperatures of ~200 K and above. The disagreement points to the fact that the harmonic approximation adopted in the models could be incorrect and anharmonic channels of energy transfer could contribute to the enhancement of h_{BD} as the temperature is increased. Anharmonic channels with multiple phonon scattering events affecting the transmission of vibrational energy

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across interfaces can lead to an increase in h_{BD} by opening additional channels for interfacial heat flow [245, 250-255].

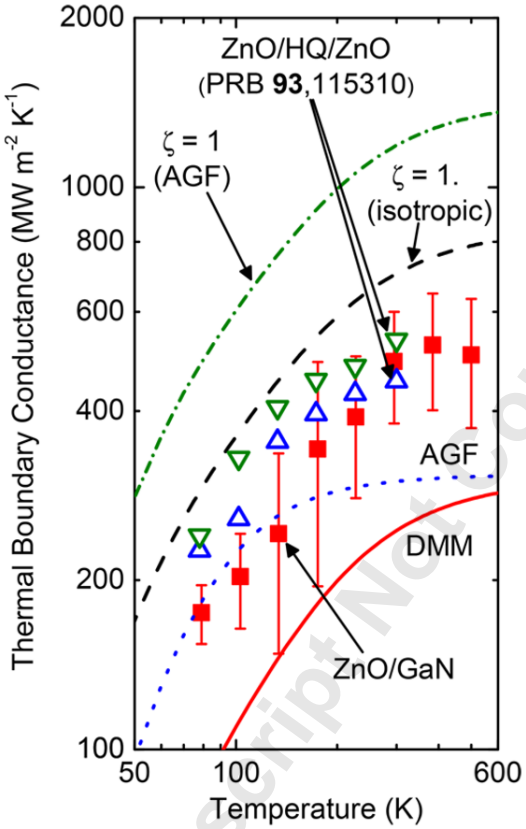

Figure 18 – Comparison of model predictions for h_{BD} to experimentally measured values. This demonstrates that atomistic simulations may prove more useful than standard phonon gas theory predictions. Reprinted from [229] with permission. © 2018 American Chemical Society.

C.2. Effect of Constituent Diffusion (Tian)

Interface roughness due to constituent diffusion commonly occurs at material interfaces [30]. Atomistic Green's function (AGF) is a powerful tool to study thermal transport across interfaces.

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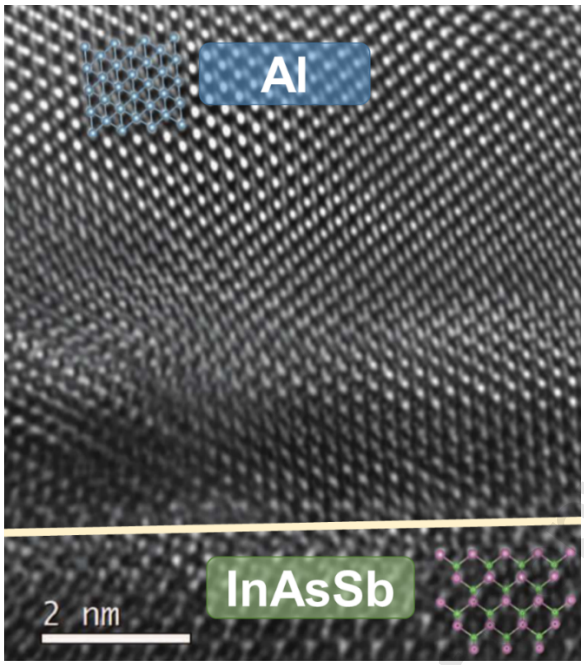

Figure 19 – Transmission electron micrograph of interfacial roughness between aluminum and indium arsenide antimonide. Reprinted from [256] with permission.

Unlike the widely-used acoustic mismatch model (AMM) and diffuse mismatch model (DMM), which only consider the material properties on both sides, AGF includes the details of the microscopic structures at the interface (as depicted in Fig. 19). Using AGF, Tian *et al.*[257] studied the effect of constituent diffusion on h_{BD} in the harmonic limit. To mimic the atomic diffusion, they created the atomic distribution at the interface to obey the half-Gaussian distribution. They found that the phonon transmission (and hence, h_{BD}) is significantly enhanced by atomic diffusion compared to a smooth interface [257], which was contrary to the conventional notion at that time (Fig. 20).

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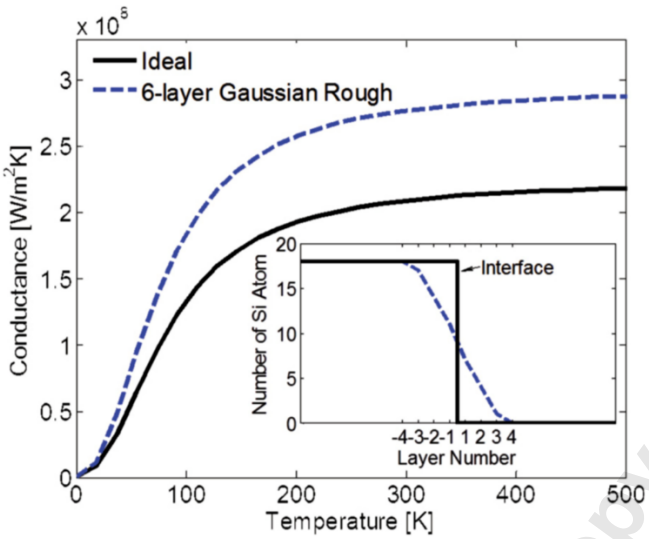

Figure 20: Demonstration of enhanced h_{BD} due to atomic diffusion at a rough surface compared with a smooth one. Reprinted from [257] with permission.

They attributed this enhancement to the effect of bridging phonon density of states of bulk leads by the mixed region. In brief, atomistic diffusion can increase phonon transmission across two dissimilar materials if the diffusion length is properly controlled. It shares the same essence with later studies on enhanced thermal interface conductance by nanopillar arrays [258] and adding a layer of impedance matcher at interface [259].

Table 2. Strategies to enhance h_{BD} with references, and degree of enhancement (at given temperature).

Enhancement Mechanism	**$h_{BD,low}$ ($MW/m^2 \cdot K$)**	**$h_{BD,enhanced}$ ($MW/m^2 \cdot K$)**
Nanopillar arrays [258]	230 (@300K)	438 (@300K)
Interlayer [259]	1012.9 (@30K)	1251.7 (@30K)
Interface roughening [257]	210 (@300K)	277 (@300K)

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C.3. Enhancement of Thermal Transport Across Power Electronics Interfaces (Shi and Graham)

To enhance the thermal transport at interfaces, we first need to understand the mechanisms leading to thermal resistance at the interface. However, there are plenty of factors which can affect the h_{BD} and R_{th} across interfaces [227] , such as inelastic phonon scattering [246, 260], interface disorder [261], different bonding strength [240, 262], crystal orientation [121, 263, 264], and electron-phonon coupling [265, 266]. Experiments and simulations are usually applied to study the contributions to thermal transport at interfaces of different mechanisms. For experiments, the time domain thermoreflectance (TDTR) method is one of the widest used and reliable methods to measure h_{BD} [28, 56, 267] . For simulations, people usually use molecular dynamics (MD) or Landauer formula with transmission functions from acoustic mismatch model (AMM), diffuse mismatch model (DMM), atomistic Green's function (AGF), or phonon wave-packet method [71, 257, 268-274]. Within the framework of MD methods, non-equilibrium MD (NEMD) [275-277] and interface conductance modal analysis (ICMA) [115, 143, 278-284] are usually applied to predict h_{BD}. The advantages of MD are that the anharmonic phonon scattering is included from the higher-order force constants of empirical interatomic potentials, and the interface structures are quite flexible, that complex interfacial details (like strong interfacial disorder and interfaces with dimensional mismatch) can be simulated. However, MD is computationally expensive and does not consider quantum effects, which will lead to inaccuracy at low temperature or small dimension. Also, MD relies on interatomic potentials and cannot be applied to systems without appropriate potentials. The advantage of Landauer approach is the consideration of quantum phonon

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statistics which is important at sub-Debye temperatures. Moreover, for Landauer method with transmission functions from AMM, DMM or AGF, phonon properties can be obtained from first-principle calculations, which means that interatomic potentials are not necessary, and for Landauer with AMM or DMM, the computational costs are not high. However, it is very difficult to include anharmonicity in Landauer approach, and the consideration of detailed interface structure or interface bonding strength in AMM or DMM is very hard to implement. Recently, there are several studies of considering anharmonicity in AGF [271, 280], but there are still some limitations like high computational costs and inaccuracy from estimated scattering rate at interfaces.

At interfaces between two crystalline materials, because of the growth limitation, the crystalline quality of one or both of the materials near the interface is usually not very good or the interfacial bonding is not very strong from different growing methods, like evaporation [263], chemical vapor deposition (CVD) [115, 281], and atomic layer deposition (ALD) [282, 285]. The low quality polycrystalline or even amorphous region near the interface will have reduced thermal conductivity compared to bulk crystal and will contribute an additional thermal resistance, and that thermal resistance might impede the thermal transport from devices, especially for high frequency applications. In a recent study of Al/sapphire interface with TDTR and Landauer approach with transmission from AGF and DMM, it is found that an ultraclean and atomically smooth interface can be obtained by growth via molecular beam epitaxy (MBE) [283]. There are several reasons that the MBE Al/sapphire interface is ultraclean: the good quality of sapphire substrate, there is no reaction between sapphire and Al during growth, and the orientation of sapphire is carefully selected to insure small lattice mismatch and similar crystalline structure. It is observed

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that the h_{BD} at the MBE-grown Al/sapphire interface is larger than all other h_{BD} measurements in literature [283]. It is also observed that at the ultraclean Al/sapphire interface, the elastic phonon scattering dominates the phonon transmission, while inelastic scattering and electron-phonon coupling are not important.

From previous studies, some strategies to enhance the thermal transport at interfaces have been developed, such as lighter atom substitution [286], patterned interface [115], and room-temperature surface-activated bonding (SAB) technique [143, 284]. From a study of h_{BD} at SiC/GaN with NEMD method, it is found that substituting Ga atoms in the GaN lattice with lighter atoms near the interface can increase the h_{BD} by up to 50% [286]. From a study at Si/diamond interface with TDTR, NEMD, and Landauer formalism, it is observed that it is possible to increase the h_{BD} at semiconductor dielectric interfaces by graphoepitaxially growing diamond on nanopatterned silicon wafers. Because of the importance of thermal transport at both semiconductor-semiconductor and semiconductor-dielectric interfaces in power electronic devices, there are studies attempting to directly bond crystalline semiconductor and dielectric materials together. If two single-crystalline materials could be directly bonded together, the material quality near the interface should be better than directly growing one material on another, and a high thermal conductivity dielectric material or semiconducting material (e.g. diamond) can be used as heat spreading material to enhance heat dissipation in the device. Although very high values of hBD are realized via MBE deposition, the growth is very slow and the process is difficult to scale in an industrial setting [143, 284]. On the other hand, if two materials are bonded at high temperature, there will be residual stress at the interface because of different thermal expansion coefficients of two materials. The stress will affect interface quality and

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introduce additional thermal resistance [143, 284]. Therefore, a room-temperature SAB technique is developed to achieve the high-quality interface of MBE with the manufacturing ease of material bonding. From the TDTR measurements, the measured h_{BD}s at both GaN/SiC and GaN/diamond room-temperature SAB interfaces are among the high values reported in the literatures. Fig. 21 reports the results of this study.

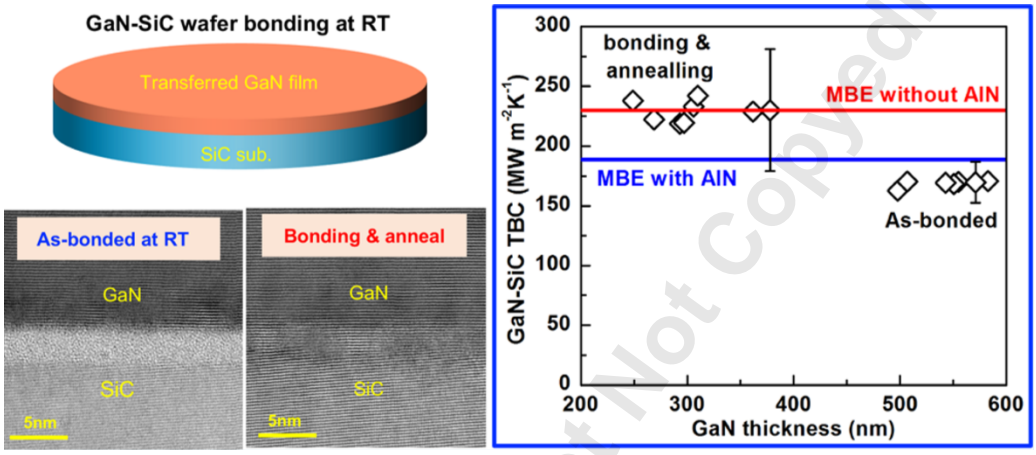

Figure 21: Graphical depiction of enhancement of thermal boundary conductance by surface bonding, demonstrating that it is possible to achieve similar h_{BD} values as epitaxially grown films. Reprinted from [284] with permission. ©2019, American Chemical Society.

D. NANOSCALE HEAT CONDUCTION IN 2D MATERIALS (DONMEZER)

Two-dimensional materials have drawn the attention of the electronics community over the last decade. Among them, graphene has been the most researched material due to its superior physical properties, such as high thermal conductivity (≈2000-5000 W/m·K)[287] and electron mobility [288]. Graphene has been used in modern electronics applications such as flexible organic light emitting diodes [288], field effect transistors [289], and as heat spreaders [290]. To open an energy gap in graphene and achieve functionality, various techniques such as chemical functionalization, quantum confinement

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(in nanoribbons), and electric field application (to bilayer and trilayer structures) [291] have been developed. Single layer hexagonal boron-nitride (h-BN) that shares similar lattice parameters [292] with graphene is also a good candidate for electronic applications, due to its favorable properties such as high thermal/chemical stability and dielectric nature [293]. Yet monolayer h-BN has a much lower thermal conductivity (≈500 W/m·K) compared to that of graphene [294].

Alongside the advancements in graphene and h-BN world, new functional 2D materials (2DMs) have also emerged. These materials, such as TMDs (transition metal dichalcogenides) [289], phosphorene, and others, have superior semiconductor performances due to their diverse, tunable electronic structures [291] and large bandgaps. In a very short period of time, the use of these materials in electronic and optoelectronic applications such as field effect transistors (FETs) and infrared detectors has been demonstrated. Emerging 2DMs also opened new horizons in the transistor community right when the physical limitations (i.e. source-drain tunneling below 5nm) of Moore's law started to reveal themselves [289]. Today, industries' interests in continuing gate length scaling has begun to diminish since there is increasing demand for logic and memory chips with low power consumption, e.g., for mobile applications. It has been proven that ultrathin channels provide improved electrostatic gate control and reduced short-channel effects, which results in better geometric scaling and less power consumption [295]. To achieve this, 2DMs are considered as future channel materials for next generation transistors. Among the future channel materials, MoS_2, a type of TMD, has been investigated more than others due to its geological availability, environmental stability (even when present in

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monolayer form), as well as its conformity to low resistance contacts for electron injection [296].

Understanding heat transport mechanisms in emerging devices with 2DMs (whether used as channel materials or heat spreaders) is crucial for understanding and improving device reliability. Since heat dissipation in devices is significantly affected by the thermal conductivity of the materials close to the active regions and h_{BD} between material layers, the first group of studies focused on this. Researchers found that both monolayer h-BN [297] and graphene [298-300] exhibit higher thermal conductivities than that of the corresponding bulk structures due to a reduction in phonon-phonon scattering events. Thermal conductivity of monolayer MoS_2, which is lower than the bulk thermal conductivity of MoS_2, [301] has been investigated through simulations and experiments, as well. Ab-initio simulations calculated the thermal conductivity of 1 μm sized suspended monolayers of MoS_2 (83 W/m·K) at room temperature [302]. Molecular dynamics simulations predict a much smaller in-plane thermal conductivity for MoS_2 (1.35 W/m·K), three orders of magnitude lower than that of graphene, which is due to additional phonon scattering events caused by the sample size [303]. Experimental results obtained using the Raman technique agree with the former also prove that lateral sample size, temperature, and the presence of isotopes, imperfections, and/or defects strongly effect the in-plane thermal conductivity of MoS_2 monolayers [301, 304]. Phonon thermal conductivity mean free path accumulation information obtained through theoretical calculations 2DMs [294] can be used to understand the changes in in-plane thermal conductivity of materials due to boundary scattering events in devices with small lateral dimensions.

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In the majority of the above studies, investigated 2DMs were in suspended form. Yet, it is known that in real applications these layers are often in contact with substrate and/or other material layers. Thus, not only the thermal conductivities of material layers should be investigated in the presence of other layers in close vicinity but also the h_{BD} between material layers should be studied. A previous study measuring the thermal conductivity of supported MoS_2 films on SiO_2 / Si substrates using Raman spectroscopy proves the strong dependence of thermal conductivity on temperature [304, 305]. There are studies calculating the thermal conductivity of monolayer MoS_2 / $MoSe_2$ [306] and h-BN/graphene [294] heterostructures, which have potential use for electronic applications, using classical molecular dynamics and ab-initio simulations, respectively. Finally, h_{BD} between monolayer MOS_2 and graphene grown on SiO_2/Si substrates are obtained by analyzing the electrical thermometry results with 3D finite element analysis is found to be 20.3-33.5 MW/m^2K, much larger than the ones predicted by earlier Raman-based measurements [307]. A more recent study using a similar Raman based approach obtains a h_{BD} between MoS_2 and SiO_2 and AlN substrates as 15 MW/m^2K, with reasonable agreement to latter study given the uncertainty of experiments [308]. It is expected that both the low in-plane thermal conductivity of MoS_2 and the h_{BD} values of 2DMs in these ranges will limit energy dissipation from device active layers.

To understand the effect of these thermal properties on device temperature distribution and electrical performance, temperature characterization studies should also be performed. Past modeling efforts for device thermal characterization include ab-initio modeling studies [309] and multiscale modeling studies where active areas in which nanoscale heat transfer effects are modeled through molecular dynamics simulations and

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the rest of the device being modeled through 3D finite element simulations [310]. There are also studies modeling the entire 2D field-effect transistor (FET) structure by solving a quasi-ballistic heat transfer of phonons [311, 312]. Temperature characterization can also be performed experimentally using high resolution thermography techniques. For example, previously temperature distribution of the monolayer MoS_2 transistors is obtained using Raman thermometry with ~0.3μm spatial resolution determined by the laser spot size [308]. These studies show that thermal breakdown of such devices occurs at the drain side of the channel where highest temperatures are observed.

The results of previous studies reveal the importance of thermal analysis in improvement of the 2D electronic devices. To perform accurate thermal analysis studies and suggest thermal solutions for devices, correct use of thermophysical properties for the active areas of the devices, multiphysics/multiscale thermal modeling techniques, and high resolution thermography techniques are required.

E. 2D MATERIAL INTERFACES (GIRI & HOPKINS)

As incorporation of 2D materials in devices such as in photovoltaics and field-effect tunneling transistors becomes ubiquitous [313, 314], it becomes highly imperative to study the thermal conductance across 2D/3D material systems. In this regard, experimental methods such as Raman spectroscopy [308, 315-317], pump-probe thermoreflectance [318-320], 3ω technique [321, 322], and electrical thermometries [307, 323] have been utilized to measure the thermal conductance across interfaces comprised of 2D materials. A large proportion of these studies have measured very low thermal boundary conductances in the range of 20-35 $MWm^{-2}K^{-1}$ across graphene on SiO_2 and AlN substrates

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[307, 319, 320, 324, 325]. Moreover, Freedy et. al. [326] have shown that one needs to be careful when describing heat flow across graphene interfaces since the thermal resistance across Ti/Gr/SiO_2 contacts are largely dependent on the oxide composition at the contacts.

Both atomistic simulations [327-330] and analytical frameworks have ascribed the low conductances associated with 2D material interfaces to the coupling between flexural acoustic phonons of the 2D material and the substrate [76, 260, 331-335]. Along with the importance of flexural modes, Foss et. al. [331] highlighted the role of the substrate properties such as sound speed and the mass density to be important factors while considering the heat transfer across 2D/3D interfaces.

F. THERMAL INTERFACE MATERIALS AND NANOSCALE HEAT FLOW

Heat flow across thermal interface materials (TIMs) is fast becoming the largest source of thermal resistance in conventional electronics packaging systems [28, 29, 115, 219, 336]. This is principally due to: (1) improvements in the thermal properties of electronic materials and (2) reductions in the size of heat spreading components and heat sinks. In this section we highlight recent advancements made in (and corresponding measurements of) thermal transport across TIM junctions via nanostructuring.

F.1. Nanoparticle-based TIMs (Warzoha)

A variety of works have proposed the inclusion of nanoparticles in conventional TIMs to improve their thermal conductivity [337-339]. However, the disordered nature of nanoparticles often results in significant thermal contact resistance between adjacent

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nanoparticles [340] or between the nanoparticles and the surrounding matrix material [341, 342]. As a result, it is often difficult to achieve theoretical improvements using effective medium approximations.

To reduce disorder, several studies have proposed the use of aligned nanostructures [343-345] having high thermal conductivity. These structures are often found to provide higher thermal conductivity than randomly dispersed nanoparticle-laden materials, but still suffer from poor thermal contact at relevant packaging interfaces and therefore do little to mitigate the large temperature drops that occur across interfaces.

The most promising advancements in TIM performance have been made via nanoparticle sintering and surface functionalization, where the contact thermal resistance between nanoparticles is reduced due to the formations of strong atomic bonds at nanoparticle boundaries [346, 347]. The use of nanoparticles in these materials has less to do with taking advantage of any ultra-high thermal properties that have been measured (principally due to the presence of phonon boundary scattering in application), but because the use of nanoparticles offers an opportunity for increases surface-to-volume ratios and a reduction in the thickness of films that can be fabricated using commercial techniques. The reduction in film thickness corresponds to a direct reduction in the overall thermal resistance across the TIM, which is represented in Eqn. 14 as:

$$R_T = \frac{t_{film}}{\kappa_{film}} + 2 \cdot R_C \tag{14}$$

In Eqn. 14, R_T is the total thermal resistance across the TIM and its adjacent interfaces, t_{film} is the thickness of the film, κ_{film} is the thermal conductivity of the TIM film, and R_C is the thermal contact resistance across the bonded interfaces (which is typically assumed to be equal on each side of the interface [348] and is usually sufficient to describe thermal contact

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resistance when the TIM is surrounded by similar materials that have been machined in the same way). Based on Eqn. 14, the thickness of the film is as important as its thermal conductivity, though there are practical limits to what can be achieved in common electronics packaging systems.

DARPA's recent Nano Thermal Interfaces (NTI) program established a goal for next-generation TIMs based on a required thermal resistance across bonded interfaces [349, 350]. The program's initial goal was to reduce the total thermal resistance (R_T) to values below 1 $mm^2 \cdot K/W$, with a future goal of values that fall below 0.1 $mm^2 \cdot K/W$. Two recent studies are highlighted to demonstrate the improvements that have been made with nanoparticle-based TIMs, including those based on sintered silver nanoparticles [351] and boron nitride (BN) nanoparticle/copper TIMs [352]. The first study utilizes newly developed steady-state experimental techniques [351] to demonstrate that an overall thermal resistance of < 0.5 $mm^2 \cdot K/W$ across copper-sintered silver-copper interfaces. The authors find that the contact thermal resistance is well below 0.1 $mm^2 \cdot K/W$ with measurement uncertainty of less than 10%. In this case, the target goal of < 1 $mm^2 \cdot K/W$ is reached through a combination of reductions in thickness of the bonded material (< 10 μm) and improvements in TIM thermal conductivity (> 300 W/m·K due to the sintering of nanoparticles and a corresponding reduction in phonon boundary scattering). The low contact thermal resistance at the interface is also critical to the reduction in R_T, where Evaporated Nickel-Gold (ENIG) plating is used to provide for enhancements in the bond strength between the copper and the TIM itself. In the second study, BN nanoparticles are embedded within a copper matrix material and cross-linked to the Cu via soft organic linkers [352]. The material is fabricated using an electrodeposition technique and the total

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thermal resistance across a Si/TIM interface ranges between 0.2 and 0.4 $mm^2 \cdot K/W$ as measured using a modified frequency-domain thermoreflectance technique. The authors widely attribute the reduction in total thermal resistance to enhanced heat flow through the copper matrix due to a reduction in phonon boundary scattering at the BN/Cu interfaces. These TIMs also have relatively high thermal conductivity (~250 W/m·K) and are thin relative to other TIMs (30 – 50 μm). Ultralow thermal contact resistance (R_C) was also achieved by alleviating mismatches in phonon density of states between Si and Cu due to the presence of the soft ligands on the surface of the TIM. In both studies, nanoscale thermal transport is considered at a fundamental level and demonstrates the need for engineering heat flow at nm length scales to achieve further enhancements in heat dissipation through this level of the package.

F.2. CNT/Polymer Composites (Tian)

TIMs with high thermal conductivity are in great demand for efficient heat removal from electronic devices. Polymers are widely used as TIMs due to their gap-filling, pliable, and adhesion characteristics, but they typically have low thermal conductivity (~0.1-0.4 W/(m·K) [236, 353-356]). High-thermal conductivity fillers, such as carbon nanotubes (CNTs), have been used to enhance the effective thermal conductivity of TIMs [354-359]. Due to the significant thermal interface resistance, however, the thermal conductivity of CNT/polymer composites only shows a moderate enhancement of 2-3 times larger than that of amorphous polymers [360-364]. Vertically aligned CNTs (VACNTs) have also been proposed as constituents for thermal conductivity enhancement of polymers. Using CNTs alone, the non-uniform heights across the CNTs create a large thermal contact

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resistance at adjacent interfaces [345, 365]. Aligning CNTs in an amorphous polymer matrix, however, can significantly reduce the thermal contact resistance at VACNT interfaces. Marconnet et al. have demonstrated an enhancement of polymer thermal conductivity up to 4.9 W/(m·K) with the inclusion of VACNTs [366]. Liao *et al.* [367] showed that aligned CNT-PE composites could have a thermal conductivity of ~99.5 W/(m·K) with a length of 320 nm, although the cross-section of CNT is heavily distorted. Ma and Tian [356] studied vertically aligned CNTs and polyethylene (PE) chains based on equilibrium molecular dynamics. They found that the thermal conductivity of CNT/PE composite along the alignment direction can be as high as 470.1±45.1 W/(m·K), which is about 40% of that of CNT and about 16 times larger than that of PE. This can be well explained by their vibrational density of states. The ultrahigh thermal conductivity of aligned CNT/PE composite may open up exciting opportunities towards enhancing the cross-plane thermal conductivity of polymer-based thermal interface materials for efficient microelectronics cooling.

G. NANOSCALE ENERGY TRANSPORT IN NEXT-GENERATION MICROELECTRONIC SYSTEMS

Understanding nanoscale thermal transport at both device and integration levels is particularly important for advanced devices whose functionality relies on the thermal modification of material behavior. This section provides an overview of emerging nanoscale devices based on two classes of materials where thermal effects play an integral role in device function: chalcogenide-based phase change materials (PCMs) and thin film metal-oxides.

G.1. Phase Change Materials for Memory and Data Storage (Ruppalt)

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Chalcogenide PCMs derive their useful properties from their ability to reversibly, and non-volatilely, transition between amorphous and (poly)crystalline solid phases by application of appropriate heat profiles. When the phases exhibit strong electrical or optical contrast, as is the case for many alloys of the Ge-Sb-Te and In-Ag-Sb-Te systems [368], PCMs can be used to realize a variety of low-power, high performance, switchable or adaptive components. Used for decades as the functional material in optical storage media (e.g., CDs and DVDs) [368], chalcogenide PCMs have more recently emerged as a critical material component for digital electronic storage [369, 370], analog RF devices [371, 372], and neuromorphic systems [373, 374], as well as for other nascent electronic and optoelectronic applications [375-377].

G.1.i. PCM-based Memory

The most technologically-mature electrical use of chalcogenide PCMs is in digital memory devices, with memory products incorporating PCM-based cells already commercially available. For example, 3D X-Point, the memory technology underlying Intel's recently released Optane™ storage-class memory product, is widely reported to be PCM-based [378, 379].

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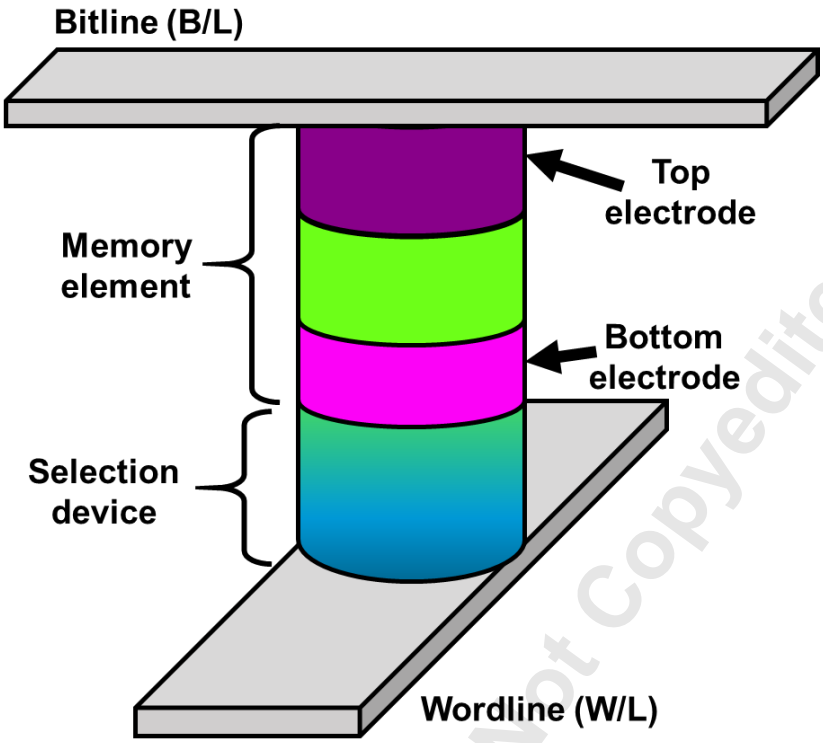

Figure 22. Basic PCM memory cross-bar array. The junction of each wordline and bitline includes a PCM memory element and a selection device. The memory element includes a single PCM cell sandwiched between top and bottom electrodes.

The most common PCM memory architecture integrates a multilayer cross-bar contact array with a single PCM cell at each junction (Fig. 22). Write operations are accomplished by applying an appropriate voltage across the cell, causing Joule heating to occur, which raises the temperature of the PCM sufficiently to switch it into either an electrically conductive polycrystalline phase, or a resistive amorphous phase. Subsequent read operations are possible by applying a low-voltage interrogation pulse, which checks resistance of the PCM. Typically, integration of selection devices at each junction is necessary to limit the effects of leakage current during operations on adjacent cells [378]. Electronic memory devices have been demonstrated using a wide variety of PCMs, with Ge-Sb-Te alloys, particularly $Ge_2Sb_2Te_5$, by far the most well-developed [369, 380].

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Already, commercialized PCM memory products are reported to outperform non-volatile NAND-based memory in terms of speed and endurance, and rival volatile DRAM's high device densities [378], with potential for even further performance improvement.

As the device's switching behavior depends critically on the temperature field within the PCM cell, understanding and controlling thermal transport at the nanoscale is critical for optimizing PCM-based digital memory, particularly as technologists push towards greater device densities to extend the performance of current technologies. Scaling device dimensions to the single-nanometer regime requires enhanced thermal confinement within the PCM cell to reduce heat loss through the electrodes [381]. Indeed, improving efficiency in ultra-small devices may require integrating atomically-thin layers, such as graphene or MoS_2, to act as a thermal barrier between the PCM and electrical contacts [382, 383]. Furthermore, the thermal gradient within the cell, as well as the impact of non-Joule heating effects, such as thermoelectric heating, can change substantially as device dimensions shrink, new materials are introduced, and interfacial effects increase in significance [384-387]. Characterizing and leveraging the thermal transport in small devices will be especially critical to achieving multi-level memory, which requires the ability to precisely and reproducibly control the temperature profile within the PCM cell to modulate the volume fraction of the cell which is crystallized or amorphized on each write step [388-390]. These challenges, among many facing PCM memory devices, require an intimate understanding of thermal transport at the nanoscale.

G.1.ii. PCM-based RF Devices

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Chalcogenide PCMs also offer advantages for switchable analog electronic devices. One notable example is the realization of high-performance, non-volatile RF switches based on GeTe [371, 391]. The prototypical PCM-based RF switch includes a PCM segment inserted into a gap in the RF signal line, where the PCM layer can be switched between an insulating amorphous (OFF) state and a conductive polycrystalline (ON) state by applying an electrical pulse to a buried refractory metal heater separated by a dielectric thermal barrier (Fig. 23(a)). A short, high-temperature pulse with a fast fall-time (i.e., quench) raises the PCM temperature above its amorphization temperature and quenches the material into an amorphous phase, while a longer, lower-temperature pulse raises the PCM temperature above its crystallization temperature, providing sufficient time and energy for the constituent atoms to organize into a polycrystalline phase (Fig. 23(b)). Using GeTe as the PCM segment, RF switches with insertion losses on the order of 0.1 dB [392] and cut-off frequencies higher than 10 THz [393] have been demonstrated.

The utility of PCM-based devices in adaptive RF architectures has already been shown by the demonstration of various reconfigurable RF circuits incorporating GeTe switches, including a reconfigurable bandpass filter [393] and a multiband receiver [394].

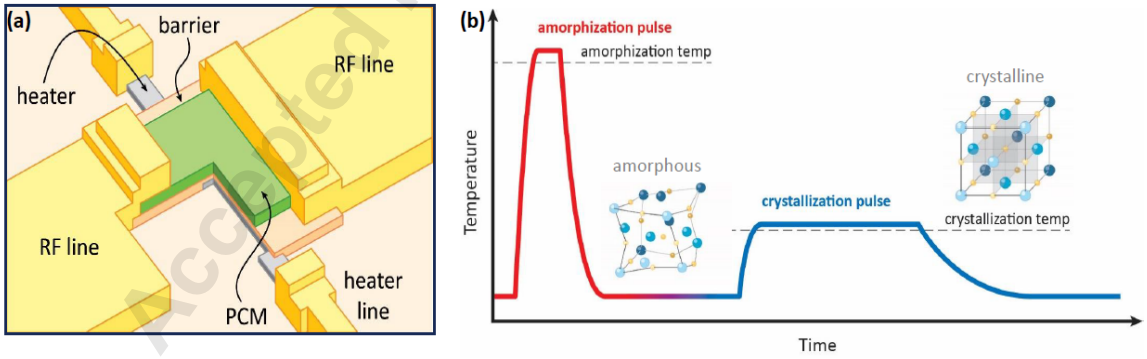

Figure 23. (a) Prototypical PCM-based RF switch, with a PCM segment inserted into a gap in the RF signal line and a buried metallic heater for supplying thermal energy to the PCM segment. (b) Schematic of the thermal profiles required to transition the PCM segment between amorphous and crystalline phases. A short, high temperature heat pulse followed by a quench amorphizes the PCM, while a longer, lower-temperature pulse crystallizes the PCM.

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Furthermore, considering the inherently high linearity [372] and low (i.e., zero) stand-by power of these devices, PCM-based RF switches are viewed as promising components for variety of RF applications requiring low insertion loss, broadband, and power-limited operations. While indirect heating using a buried heater is the most commonly-used architecture, PCM-based RF switches have also been demonstrated using direct Joule heating [395] and optically-induced phase transformation [396].

As the thermal energy necessary to induce phase transition in the PCM segment typically drives the device's power consumption, switching time, and lifetime, current research efforts in PCM-based RF devices are largely directed at lowering the thermal power required for switching. Indeed, thermal engineering by appropriate material selection and device design may be critical to being able to integrate PCM-based RF switches with the reduced power consumption, faster switching speeds, and increased lifetimes required for the most stressing applications. For example, substitution of more thermally conductive AlN for SiN or SiO_2 dielectric thermal layers has been shown to reduce device capacitance [397] and enable integration on arbitrary substrates [398]. Additionally, incorporation of more complex active layers, including quarternary PCMs with optimized electrical properties [399] or interfacial (or superlattice) PCMs with enhanced crystallization due to interface-mediated nucleation [400, 401], may be required to increase switching speeds and lower switching power while retaining RF performance. Modeling of thermal transport in PCM-based RF components, including precise characterization of material properties and interfacial effects [59], will be critical for evaluating trade-offs in material selection and device design in these multilayer structures [402, 403].

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G.1.iii. PCM-based Neuromorphic Electronics

The emerging field of neuromorphic computing offers another venue for leveraging the thermally-mediated properties of chalcogenide PCMs. Broadly, neuromorphic computing approaches aim to transcend the limitations of conventional, deterministic Von Neumann frameworks by implementing devices and architectures that mimic biological function to achieve adaptive, energy-efficient computing [373]. The potential for low-power operation and high device density, as well as the ability to co-locate memory and processing, make PCMs particularly attractive for neuromorphic platforms [374], and a variety of PCM-based biomimetic devices have already been demonstrated or simulated, including artificial synapses that possess tunable electrical weights [404, 405], and artificial integrate-and-fire neurons for generating electrical spiking signals, such as that shown in Fig. 24 [406-408].

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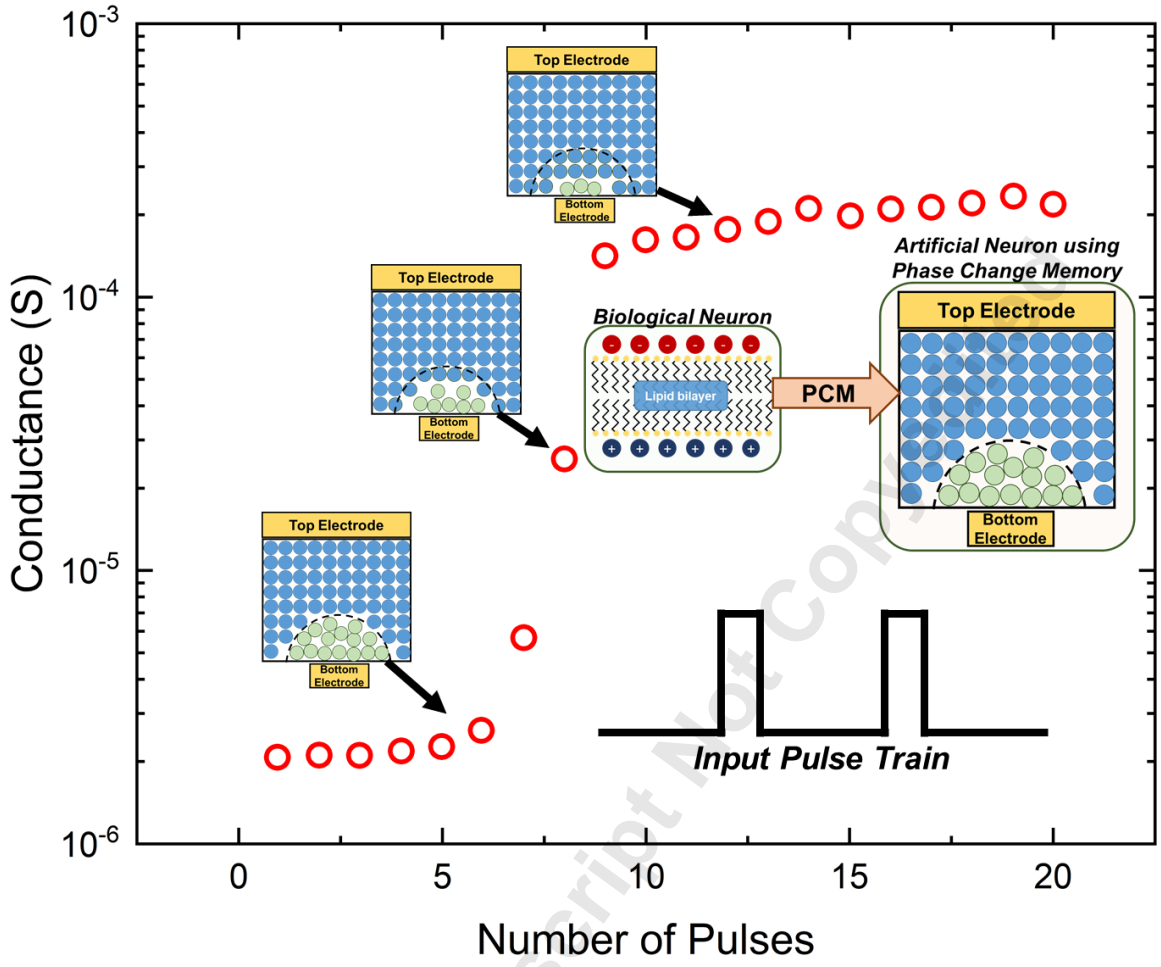

Figure 24: A representation of a PCM-based artificial integrate-and-fire neuron, where the PCM cell mimics a neuronal membrane by storing the membrane potential in the cell's phase state. Signal integration by the PCM cell portion of the artificial neuron is illustrated by the schematics and data. The rate at which the neuron reaches its integrate-and-fire threshold is determined by the power and duration of the input pulses. Data taken from [406].

Numerous groups have already demonstrated or emulated spike-timing dependent plasticity (STDP), a key behavior for many neuromorphic computing paradigms, in PCM-based systems [404, 409], and simulations and hardware implementations have shown the utility of PCM-based devices for neuromorphic computing tasks such as visual pattern extraction [410] and temporal correlation detection [411]. Though the field is in its infancy, the thermal challenges in developing PCM-based neuromorphic electronics mirror those in developing other PCM-based technologies. Device scaling, the introduction of thermally-

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optimized materials, and the use of thermal modeling to direct material selection and device design to control and direct thermal transport will be critical for realizing the dense functional networks necessary to support artificial intelligence and other advanced applications.

G.2. Nanoscale Thermal Transport in Oxides for Neuromorphic Computing (Pahinkar, Graham)

Three terminal Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have been the fundamental building block of modern electrical circuits. They are demonstrated to be extremely scalable and to follow Moore's law of scaling [412]. However, as more MOSFETs are packed into a smaller space, thermal management of these devices becomes difficult and a new challenge emerges to remove the generated heat and keep the device performance competitive at variable loads. It has been widely reported that electrical design of high density and high-performance electronic devices is possible, yet their fabrication has stalled due to packaging and heat removal constraints at nanometer length scales [413, 414]

Therefore, alternative semiconductor technologies, such as memristors, are gaining attention from the wider scientific community. Unlike conventional MOSFETs, the semiconductor materials used for these devices are transition metal oxides, such as TaO_2 [415-418], HfO_2 [419-425], VO_2 [426, 427], NbO_2 [428-430], and $LiNbO_2$ [431]. The electrical resistances of these oxides depend on the process of redox reactions, in some cases compounded with temperature assisted hopping [432]. Typically, these devices have two electrode terminals (a sample HfO_2 memristor shown in Fig. 25) and the voltage applied at one of the terminals is enough to manipulate the electrical resistance of the oxide

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material. Such design makes the individual transistor and the complete miniaturized assembly simple and compact by eliminating the third terminal entirely and by making 3-D packaging of the devices convenient at the nanoscale.

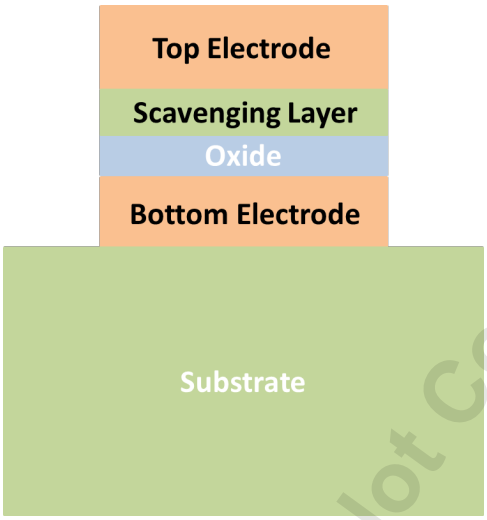

Figure 25: Schematic of a two-terminal memristor device.

However, the actual operation of the oxide devices is complex and is a topic of extensive ongoing research. As an example, in case of a fresh HfO_2 device, a positive voltage is applied at the top electrode resulting in reduction of the HfO_2 molecules in the oxide layer. The oxygen ions that are removed from the oxide layer are attracted toward the positive electrode (TE) and are stored in the scavenging layer. The scavenging layer can be synthesized with Ti or Hf, which allows movement of oxygen ions. This ion movement leaves behind a filament of positively charged oxygen vacancies, and vacancies or a metal-like filament facilitate the flow of electrons through the oxide layer. This is the on-state of the device, also known as set stage [420]. If the top electrode is subsequently biased with negative voltage, a handful of previously removed oxygen ions drift into the filament and neutralize a few monolayers' worth of vacancies, thereby reducing the electrical conductivity of the filament. In this process, oxygen ions are repelled toward the

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filament due to drift (downward in Fig. 26(a)), whereas the heat generated in the filament pushes the oxygen ions outward in the direction of the TE due to thermophoresis [415, 419]. This set of counteracting phenomena results in a controlled movement of ions and therefore a controlled change in the electrical resistance of the filament (also known as reset), thereby making the resistance a function of the applied voltage only. A sample I-V plot is shown in Fig. 26(b), which depicts the reset stage on the left and set stage on the right of V = 0.

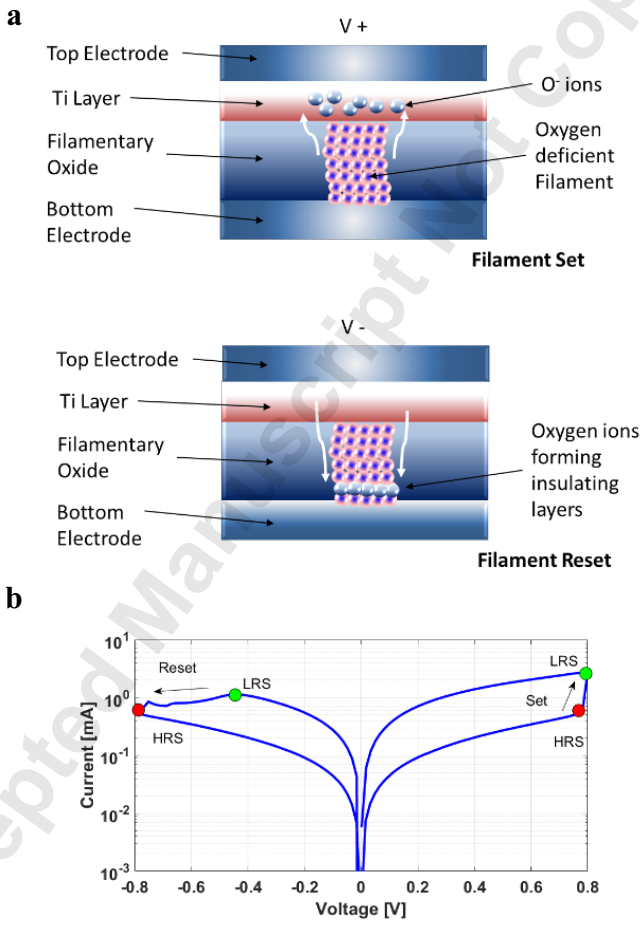

Figure 26: (a). Schematic of set and reset of the filamentary memristors. (b) A sample I-V plot showing memory window of these devices. Adapted from [433] with permission. Copyright 2019 IEEE.

For this type of memristive oxide, current flows through a conducting filament with diameter of the order of 5 – 10 nm. For a 5 nm thick oxide layer conducting 1 mA of current

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at 0.5 V (point B in Figure 26(b)), the volumetric heat dissipation through the filament (assuming that it is cylindrical) is greater than 10^{20} Wm^{-3}. This results in temperatures as high as 1500 K. As resistance of the device is increased due to ion movement, the current drops and further reduces the temperature of the filament, which severely impedes the ion mobility. The reset process is therefore self-limiting and decelerates at high negative voltages. Consequently, the thermal environment of the nanoscale filament and surrounding layers strongly affects the electrical properties of the device. In the memristor community, a device is said to be performing well if the memory window (ratio of the highest resistance to the lowest resistance) is large. This is possible if additional ions are relocated during the reset stage, which depends on continued presence of favorable thermal fields. Therefore, heat must remain trapped inside the device, despite the drop in current as the oxygen ions move. Hence, nanoscale heat transfer in the context of device fabrication must be critically assessed for the development of efficient memristor devices.

There have been several attempts in the past to manipulate the device design by changing the electrode materials, scavenging layer material (Ti), initial oxygen deficiency in the oxide layer, layer thicknesses, substrate materials and substrate thicknesses. Kim et *al.* [415] studied the effect of electrode metals such as Palladium, Rubidium and Tungsten (thermal conductivities of 72, 117, 173 W m^{-1} K^{-1}, respectively) on the current and temperature variation of TaO_x (x represents a number less than 2, which means oxygen deficiency) memristors. They reported that the use of low thermal conductivity material top electrode results in high temperature within the filament, which accelerates ion movement. When the Tungsten electrode is replaced by Palladium, the resistance ratio between reset and for 10 pulses changes from 1.37 to 1.67, which is attributed to the heat

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spreading in the top electrode. A similar effect was observed when the scavenging layer of TaO_x was varied in the thickness. A 55% decrease in the thickness of this layer resulted in a 30% increase in the resistance ratio between set and reset for TaO_x. While these devices were designed to be only 105 nm thick, the effect of substrate was not considered extensively. Pahinkar et *al.* [433] reported the effect of substrate materials on the I-V curves for HfO_x devices. It was found that the use of a low thermal conductivity substrate like glass can result in a wider memory window for these memristors as a result of more trapped heat. This result was also validated with surface temperature measurement using transient thermal imaging techniques.

With some exceptions, the studies documenting the electrical performance of oxide memristors primarily involve the selection of an oxide material, device fabrication and metallographic analyses without much emphasis on the effect of packaging and thermal management of these devices. This is because making reliable devices that can compete with the conventional MOSFETs in terms of reliability, power density and commercial presence is still a distant target. Therefore, most of the studies focus on identifying current transport mechanisms and experimentally validating the same owing to the nascent stage of the relevant research. Hence, there is a tremendous opportunity to understand nanoscale thermal transport within these devices to improve their performance in application. Techniques such as manipulating the development of the oxygen-deficient filament by preferential thermophoresis using low thermal conductivity membranes between electrodes [434], passive or second order thermal activation of several filaments [435], initial oxygen vacancy concentration [435, 436], multiple combinations of oxide layers and scavenging

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layers can be potential avenues to improve device performance as neuromorphic computing research matures.

H. CONCLUSION

In this this review, the authors demonstrate why nanoscale thermal transport is critical to the development of electronics systems across a wide array of applications. These include wide-bandgap materials and devices, neuromorphic computing, tailorable interface thermal conductance, 2D materials and interfaces and thermal interface materials in electronics packaging. We show that each application is substantially impacted by nanoscale thermal transport and argue for its incorporation in the design of future devices. The perspectives presented by the authors in this review represent key areas where a firm understanding and ability to manipulate thermal transport is crucial, and will play an important role in the continued development of electronic systems. In the coming years, the ability to tune, control, and manipulate heat at the nanoscale will become increasingly important as electronics continue to scale down in size, and increase power consumption and operational frequency.

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Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Prior Authors

REFERENCES

[1] P. Naphon, S. Wiriyasart, and S. Wongwises, "Thermal cooling enhancement techniques for electronic components," *International Communications in Heat and Mass Transfer,* vol. 61, pp. 140-145, 2015.

[2] T. Lu, "Thermal management of high power electronics with phase change cooling," *International Journal of Heat and Mass Transfer,* vol. 43, pp. 2245-2256, 2000.

[3] H. Wu, S. Xiong, S. Canchi, E. Schreck, and D. Bogy, "Nanoscale heat transfer in the head-disk interface for heat assisted magnetic recording," *Applied Physics Letters,* vol. 108, p. 093106, 2016.

[4] K. Ebrahimi, G. F. Jones, and A. S. Fleischer, "A review of data center cooling technology, operating conditions and the corresponding low-grade waste heat recovery opportunities," *Renewable and Sustainable Energy Reviews,* vol. 31, pp. 622-638, 2014.

[5] S. V. Patankar, "Airflow and cooling in a data center," *Journal of Heat transfer,* vol. 132, p. 073001, 2010.

[6] R. Schmidt. (2005, Liquid Cooling is Back. *Electronics Cooling*.

[7] J. D. Carr, "An examination of CPU cooling technologies," *DSI Ventures, Inc., Tyler, TX, USA,* 2014.

[8] B. Tekinerdogan, *Engineering connected intelligence: a socio-technical perspective*: Wageningen University & Research, 2017.

[9] K. König and A. Ostendorf, *Optically induced nanostructures: biomedical and technical applications*: Walter de Gruyter GmbH & Co KG, 2015.

[10] S. N. Truong, K. Van Pham, W. Yang, and K.-S. Min, "Memristor circuits and systems for future computing and bio-inspired information processing," in *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2016, pp. 456-459.

[11] J. Wu, Y.-L. Shen, K. Reinhardt, H. Szu, and B. Dong, "A Nanotechnology Enhancement to Moore's Law," *Applied Computational Intelligence and Soft Computing,* vol. 2013, pp. 1-13, 2013.

[12] I. L. Markov, "Limits on fundamental limits to computation," *Nature,* vol. 512, pp. 147-54, Aug 14 2014.

[13] J. R. Powell, "The quantum limit to Moore's law," *Proceedings of the IEEE,* vol. 96, pp. 1247-1248, 2008.

[14] J. Shalf, "HPC Interconnects at the End of Moore's Law," in *2019 Optical Fiber Communications Conference and Exhibition (OFC)*, 2019, pp. 1-3.

[15] S. E. Thompson and S. Parthasarathy, "Moore's law: the future of Si microelectronics," *Materials today,* vol. 9, pp. 20-25, 2006.

[16] V. Thirunavukkarasu, Y.-R. Jhan, Y.-B. Liu, and Y.-C. Wu, "Performance of inversion, accumulation, and junctionless mode n-type and p-type bulk silicon FinFETs with 3-nm gate length," *IEEE Electron Device Letters,* vol. 36, pp. 645-647, 2015.

[17] Y. Ju and K. Goodson, "Phonon scattering in silicon films with thickness of order 100 nm," *Applied Physics Letters,* vol. 74, pp. 3005-3007, 1999.

[18] G. Chen, *Nanoscale energy transport and conversion: a parallel treatment of electrons, molecules, phonons, and photons*: Oxford University Press, 2005.

Accepted Manuscript Not Copyedited

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Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Rest Authors

[19] G. Froehlicher and S. Berciaud, "Raman spectroscopy of electrochemically gated graphene transistors: Geometrical capacitance, electron-phonon, electron-electron, and electron-defect scattering," *Physical Review B,* vol. 91, p. 205413, 2015.

[20] B. C. Gundrum, D. G. Cahill, and R. S. Averback, "Thermal conductance of metal-metal interfaces," *Physical Review B,* vol. 72, p. 245426, 2005.

[21] J. Parrott, "Heat conduction mechanisms in semiconducting materials," *Revue Internationale Des Hautes Temperatures Et Des Refractaires,* vol. 16, pp. 393-403, 1979.

[22] B. F. Donovan, D. M. Long, A. Moballegh, N. Creange, E. C. Dickey, and P. E. Hopkins, "Impact of intrinsic point defect concentration on thermal transport in titanium dioxide," *Acta Materialia,* vol. 127, pp. 491-497, 2017.

[23] Y. Zhou and M. Hu, "Full quantification of frequency-dependent interfacial thermal conductance contributed by two- and three-phonon scattering processes from nonequilibrium molecular dynamics simulations," *Physical Review B,* vol. 95, 2017.

[24] A. Giri, J. L. Braun, and P. E. Hopkins, "Effect of crystalline/amorphous interfaces on thermal transport across confined thin films and superlattices," *Journal of Applied Physics,* vol. 119, p. 235305, 2016.

[25] P. E. Hopkins, J. C. Duda, C. W. Petz, and J. A. Floro, "Controlling thermal conductance through quantum dot roughening at interfaces," *Physical Review B,* vol. 84, p. 035438, 2011.

[26] S. Narumanchi, M. Mihalic, K. Kelly, and G. L. Eesley, "Thermal interface materials for power electronics applications," in *2008 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2008.

[27] W. D. Hu, X. S. Chen, Z. J. Quan, C. S. Xia, W. Lu, and P. D. Ye, "Self-heating simulation of GaN-based metal-oxide-semiconductor high-electron-mobility transistors including hot electron and quantum effects," *Journal of Applied Physics,* vol. 100, p. 074501, 2006.

[28] D. G. Cahill, W. K. Ford, K. E. Goodson, G. D. Mahan, A. Majumdar, H. J. Maris*, et al.*, "Nanoscale thermal transport," *Journal of applied physics,* vol. 93, pp. 793-818, 2003.

[29] D. G. Cahill, P. V. Braun, G. Chen, D. R. Clarke, S. Fan, K. E. Goodson*, et al.*, "Nanoscale thermal transport. II. 2003–2012," *Applied physics reviews,* vol. 1, p. 011305, 2014.

[30] P. E. Hopkins, "Thermal transport across solid interfaces with nanoscale imperfections: effects of roughness, disorder, dislocations, and bonding on thermal boundary conductance," *ISRN Mechanical Engineering,* vol. 2013, 2013.

[31] R. Franz and G. Wiedemann, "Ueber die Wärme-Leitungsfähigkeit der Metalle," *Annalen der Physik,* vol. 165, pp. 497-531, 1853.

[32] Q. Zheng, A. B. Mei, M. Tuteja, D. G. Sangiovanni, L. Hultman, I. Petrov*, et al.*, "Phonon and electron contributions to the thermal conductivity of V N x epitaxial layers," *Physical Review Materials,* vol. 1, p. 065002, 2017.

[33] W. S. WILLIAMS, "High-temperature thermal conductivity of transition metal carbides and nitrides," *Journal of the American Ceramic Society,* vol. 49, pp. 156-159, 1966.

Accepted Manuscript Not Copyedited

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Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Rep Authors

[34] W. S. Williams, "The thermal conductivity of metallic ceramics," *JOM,* vol. 50, pp. 62-66, 1998.
[35] Z. M. Zhang, *Nano/microscale heat transfer*, 2007.
[36] W. Li, J. Carrete, N. A. Katcho, and N. Mingo, "ShengBTE: A solver of the Boltzmann transport equation for phonons," *Computer Physics Communications,* vol. 185, pp. 1747-1758, 2014.
[37] A. J. McGaughey and M. Kaviany, "Quantitative validation of the Boltzmann transport equation phonon thermal conductivity model under the single-mode relaxation time approximation," *Physical Review B,* vol. 69, p. 094303, 2004.
[38] G. Chen, "Phonon heat conduction in nanostructures," *International journal of thermal sciences,* vol. 39, pp. 471-480, 2000.
[39] A. Henry and G. Chen, "High thermal conductivity of single polyethylene chains using molecular dynamics simulations," *Physical review letters,* vol. 101, p. 235502, 2008.
[40] F. Müller-Plathe, "A simple nonequilibrium molecular dynamics method for calculating the thermal conductivity," *The Journal of chemical physics,* vol. 106, pp. 6082-6085, 1997.
[41] D. P. Sellan, E. S. Landry, J. Turney, A. J. McGaughey, and C. H. Amon, "Size effects in molecular dynamics thermal conductivity predictions," *Physical Review B,* vol. 81, p. 214305, 2010.
[42] S. G. Volz and G. Chen, "Molecular dynamics simulation of thermal conductivity of silicon nanowires," *Applied Physics Letters,* vol. 75, pp. 2056-2058, 1999.
[43] A. Ward, D. Broido, D. A. Stewart, and G. Deinzer, "Ab initio theory of the lattice thermal conductivity in diamond," *Physical Review B,* vol. 80, p. 125203, 2009.
[44] N. Shulumba, O. Hellman, and A. J. Minnich, "Lattice Thermal Conductivity of Polyethylene Molecular Crystals from First-Principles Including Nuclear Quantum Effects," *Physical review letters,* vol. 119, p. 185901, 2017.
[45] Z. Wei, G. Wehmeyer, C. Dames, and Y. Chen, "Geometric tuning of thermal conductivity in three-dimensional anisotropic phononic crystals," *Nanoscale,* vol. 8, pp. 16612-16620, 2016.
[46] Z. Yu, L. Ferrer-Argemi, and J. Lee, "Investigation of thermal conduction in symmetric and asymmetric nanoporous structures," *Journal of applied physics,* vol. 122, p. 244305, 2017.
[47] D. G. Cahill, "Thermal conductivity measurement from 30 to 750 K: the 3ω method," *Review of Scientific Instruments,* vol. 61, pp. 802-808, 1990.
[48] T. Wang, X. Wang, J. Guo, Z. Luo, and K. Cen, "Characterization of thermal diffusivity of micro/nanoscale wires by transient photo-electro-thermal technique," *Applied Physics A,* vol. 87, pp. 599-605, 2007.
[49] C. Dames, "Measuring the thermal conductivity of thin films: 3 omega and related electrothermal methods," *Annual Review of Heat Transfer,* vol. 16, 2013.
[50] A. A. Wilson, "Scanning thermal probe calibration for accurate measurement of thermal conductivity of ultrathin films," *MRS Communications,* vol. 9, pp. 650-656, 2019.
[51] A. Majumdar, "Scanning thermal microscopy," *Annual Review of Materials Science,* vol. 29, pp. 505-585, 1999.

Accepted Manuscript, Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Rep Authors

[52] A. A. Wilson and T. Borca-Tasciuc, "Quantifying non-contact tip-sample thermal exchange parameters for accurate scanning thermal microscopy with heated microprobes," *Rev Sci Instrum,* vol. 88, p. 074903, Jul 2017.

[53] D. G. Cahill, H. E. Fischer, T. Klitsner, E. Swartz, and R. Pohl, "Thermal conductivity of thin films: Measurements and understanding," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 7, pp. 1259-1266, 1989.

[54] P. M. Norris, A. P. Caffrey, R. J. Stevens, J. M. Klopf, J. T. McLeskey Jr, and A. N. Smith, "Femtosecond pump–probe nondestructive examination of materials," *Review of scientific instruments,* vol. 74, pp. 400-406, 2003.

[55] A. N. Smith, J. L. Hostetler, and P. M. Norris, "Thermal boundary resistance measurements using a transient thermoreflectance technique," *Microscale Thermophysical Engineering,* vol. 4, pp. 51-60, 2000.

[56] P. Jiang, X. Qian, and R. Yang, "Tutorial: Time-domain thermoreflectance (TDTR) for thermal property characterization of bulk and thin film materials," *Journal of Applied Physics,* vol. 124, p. 161103, 2018.

[57] A. J. Schmidt, R. Cheaito, and M. Chiesa, "A frequency-domain thermoreflectance method for the characterization of thermal properties," *Review of scientific instruments,* vol. 80, p. 094901, 2009.

[58] A. J. Schmidt, R. Cheaito, and M. Chiesa, "Characterization of thin metal films via frequency-domain thermoreflectance," *Journal of Applied Physics,* vol. 107, p. 024908, 2010.

[59] R. J. Warzoha, B. F. Donovan, N. T. Vu, J. G. Champlain, S. Mack, and L. B. Ruppalt, "Nanoscale thermal transport in amorphous and crystalline GeTe thin-films," *Applied Physics Letters,* vol. 115, p. 023104, 2019.

[60] J. L. Braun, D. H. Olson, J. T. Gaskins, and P. E. Hopkins, "A steady-state thermoreflectance method to measure thermal conductivity," *Review of Scientific Instruments,* vol. 90, p. 024905, 2019.

[61] R. Peierls, "Zur kinetischen theorie der wärmeleitung in kristallen," *Annalen der Physik,* vol. 395, pp. 1055-1101, 1929.

[62] D. G. Cahill and R. Pohl, "Heat flow and lattice vibrations in glasses," *Solid State Communications,* vol. 70, pp. 927-930, 1989.

[63] A. Ward and D. Broido, "Intrinsic lattice thermal conductivity of Si/Ge and GaAs/AlAs superlattices," *Physical Review B,* vol. 77, p. 245328, 2008.

[64] V. Y. Davydov, Y. E. Kitaev, I. Goncharuk, A. Smirnov, J. Graul, O. Semchinova*, et al.*, "Phonon dispersion and Raman scattering in hexagonal GaN and AlN," *Physical Review B,* vol. 58, p. 12899, 1998.

[65] M. Schowalter, A. Rosenauer, J. Titantah, and D. Lamoen, "Temperature-dependent Debye–Waller factors for semiconductors with the wurtzite-type structure," *Acta Crystallographica Section A: Foundations of Crystallography,* vol. 65, pp. 227-231, 2009.

[66] G. A. Slack, "Thermal Conductivity of Pure and Impure Silicon, Silicon Carbide, and Diamond," *Journal of Applied Physics,* vol. 35, pp. 3460-3466, 1964.

[67] J. Garg, T. Luo, and G. Chen, "Spectral concentration of thermal conductivity in GaN—A first-principles study," *Applied Physics Letters,* vol. 112, p. 252101, 2018.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[68] G. A. Slack, R. A. Tanzilli, R. Pohl, and J. Vandersande, "The intrinsic thermal conductivity of AIN," *Journal of Physics and Chemistry of Solids,* vol. 48, pp. 641-647, 1987.

[69] S.-M. Lee, D. G. Cahill, and R. Venkatasubramanian, "Thermal conductivity of Si–Ge superlattices," *Applied physics letters,* vol. 70, pp. 2957-2959, 1997.

[70] M. Simkin and G. Mahan, "Minimum thermal conductivity of superlattices," *Physical Review Letters,* vol. 84, p. 927, 2000.

[71] E. T. Swartz and R. O. Pohl, "Thermal boundary resistance," *Reviews of modern physics,* vol. 61, p. 605, 1989.

[72] R. Peterson and A. Anderson, "Acoustic-mismatch model of the Kaptiza resistance," *Physics Letters A,* vol. 40, pp. 317-319, 1972.

[73] E. Swartz and R. Pohl, "Thermal resistance at interfaces," *Applied Physics Letters,* vol. 51, pp. 2200-2202, 1987.

[74] L. D. Bellis, P. E. Phelan, and R. S. Prasher, "Variations of acoustic and diffuse mismatch models in predicting thermal-boundary resistance," *Journal of thermophysics and heat transfer,* vol. 14, pp. 144-150, 2000.

[75] P. Reddy, K. Castelino, and A. Majumdar, "Diffuse mismatch model of thermal boundary conductance using exact phonon dispersion," *Applied Physics Letters,* vol. 87, p. 211908, 2005.

[76] J. C. Duda, J. L. Smoyer, P. M. Norris, and P. E. Hopkins, "Extension of the diffuse mismatch model for thermal boundary conductance between isotropic and anisotropic materials," *Applied Physics Letters,* vol. 95, p. 031912, 2009.

[77] S. J. Pearton and F. Ren, "GaN electronics," *Advanced Materials,* vol. 12, pp. 1571-1580, 2000.

[78] K. W. Jung, C. R. Kharangate, H. Lee, J. Palko, F. Zhou, M. Asheghi*, et al.*, "Microchannel cooling strategies for high heat flux (1 kW/cm 2) power electronic applications," in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2017, pp. 98-104.

[79] J. W. Pomeroy, R. B. Simon, H. Sun, D. Francis, F. Faili, D. J. Twitchen*, et al.*, "Contactless thermal boundary resistance measurement of GaN-on-diamond wafers," *IEEE Electron Device Letters,* vol. 35, pp. 1007-1009, 2014.

[80] T. L. Bougher, L. Yates, C.-F. Lo, W. Johnson, S. Graham, and B. A. Cola, "Thermal boundary resistance in GaN films measured by time domain thermoreflectance with robust Monte Carlo uncertainty estimation," *Nanoscale and Microscale Thermophysical Engineering,* vol. 20, pp. 22-32, 2016.

[81] R. Cheaito, J. T. Gaskins, M. E. Caplan, B. F. Donovan, B. M. Foley, A. Giri*, et al.*, "Thermal boundary conductance accumulation and interfacial phonon transmission: Measurements and theory," *Physical Review B,* vol. 91, p. 035432, 2015.

[82] T. Kaneko, K. Shiikuma, and K. Kunihiro, "GaN HEMT high efficiency power amplifiers for 4G/5G mobile communication base stations," in *2014 Asia-Pacific Microwave Conference*, 2014, pp. 994-997.

[83] M. Yao, M. M. Sohul, X. Ma, V. Marojevic, and J. H. Reed, "Sustainable green networking: exploiting degrees of freedom towards energy-efficient 5G systems," *Wireless Networks,* vol. 25, pp. 951-960, 2017.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[84] K. Yuk, G. Branner, and C. Cui, "Future directions for GaN in 5G and satellite communications," in *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2017, pp. 803-806.

[85] P. Ivanov and V. Chelnokov, "Recent developments in SiC single-crystal electronics," *Semiconductor science and technology,* vol. 7, p. 863, 1992.

[86] M. Khan, G. Simin, S. Pytel, A. Monti, E. Santi, and J. Hudgins, "New developments in gallium nitride and the impact on power electronics," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 15-26.

[87] J. Casady and R. W. Johnson, "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid-State Electronics,* vol. 39, pp. 1409-1422, 1996.

[88] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics,* vol. 29, pp. 2155-2163, 2014.

[89] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics-a role for wide bandgap semiconductors?," *Proceedings of the IEEE,* vol. 90, pp. 1065-1076, 2002.

[90] B. Ozpineci and L. M. Tolbert, *Comparison of wide-bandgap semiconductors for power electronics applications*: United States. Department of Energy, 2004.

[91] G. Auer, V. Giannini, C. Desset, I. Godor, P. Skillermark, M. Olsson*, et al.*, "How much energy is needed to run a wireless network?," *IEEE Wireless Communications,* vol. 18, pp. 40-49, 2011.

[92] A. Bar-Cohen, J. J. Maurer, and A. Sivananthan, "Near-junction microfluidic thermal management of RF power amplifiers," in *2015 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS)*, 2015, pp. 1-8.

[93] K. Cheng, Y. Feng, C. Lv, S. Zhang, J. Qin, and W. Bao, "Performance Evaluation of Waste Heat Recovery Systems Based on Semiconductor Thermoelectric Generators for Hypersonic Vehicles," *Energies,* vol. 10, p. 570, 2017.

[94] M. N. Hasan, E. Swinnich, and J.-H. Seo, "Recent Progress in Gallium Oxide and Diamond Based High Power and High-Frequency Electronics," *International Journal of High Speed Electronics and Systems,* vol. 28, p. 1940004, 2019.

[95] H. Jain, S. Rajawat, and P. Agrawal, "Comparision of wide band gap semiconductors for power electronics applications," in *2008 International Conference on Recent Advances in Microwave Theory and Applications*, 2008, pp. 878-881.

[96] L. M. Boteler, V. A. Niemann, D. P. Urciuoli, and S. M. Miner, "Stacked power module with integrated thermal management," in *2017 IEEE International Workshop on Integrated Power Packaging (IWIPP)*, 2017, pp. 1-5.

[97] L. M. Boteler and D. P. Urciuoli, "Stacked power module with integrated thermal management," ed: Google Patents, 2019.

[98] D. G. Pahinkar, L. Boteler, D. Ibitayo, S. Narumanchi, P. Paret, D. DeVoto*, et al.*, "Liquid-Cooled Aluminum Silicon Carbide Heat Sinks for Reliable Power Electronics Packages," *Journal of Electronic Packaging,* vol. 141, 2019.

[99] P. Roussel, "SiC market and industry update," in *Int. SiC Power Electron. Appl. Workshop, Kista, Sweden*, 2011.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[100] C. J. Glassbrenner and G. A. Slack, "Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point," *Physical Review,* vol. 134, pp. A1058-A1069, 1964.
[101] J. Zou, D. Kotchetkov, A. A. Balandin, D. I. Florescu, and F. H. Pollak, "Thermal conductivity of GaN films: Effects of impurities and dislocations," *Journal of Applied Physics,* vol. 92, pp. 2534-2539, 2002.
[102] K. Belay, Z. Etzel, D. G. Onn, and T. R. Anthony, "The thermal conductivity of polycrystalline diamond films: Effects of isotope content," *Journal of Applied Physics,* vol. 79, pp. 8336-8340, 1996.
[103] Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui*, et al.*, "Anisotropic thermal conductivity in single crystal β-gallium oxide," *Applied Physics Letters,* vol. 106, p. 111909, 2015.
[104] J. Pernot, C. Tavares, E. Gheeraert, E. Bustarret, M. Katagiri, and S. Koizumi, "Hall electron mobility in diamond," *Applied Physics Letters,* vol. 89, p. 122111, 2006.
[105] D. R. Lide, *CRC handbook of chemistry and physics* vol. 85: CRC press, 2004.
[106] P. Patnaik, *Handbook of inorganic chemicals* vol. 529: McGraw-Hill New York, 2003.
[107] P. Y. Yu and M. Cardona, *Fundamentals of semiconductors: physics and materials properties*: Springer, 1996.
[108] M. Roschke and F. Schwierz, "Electron mobility models for 4H, 6H, and 3C SiC [MESFETs]," *IEEE Transactions on Electron Devices,* vol. 48, pp. 1442-1447, 2001.
[109] Y. Zhang, A. Neal, Z. Xia, C. Joishi, J. M. Johnson, Y. Zheng*, et al.*, "Demonstration of high mobility and quantum transport in modulation-doped β-(AlxGa1-x) 2O3/Ga2O3 heterostructures," *Applied Physics Letters,* vol. 112, p. 173502, 2018.
[110] C. Yuan, J. W. Pomeroy, and M. Kuball, "Above bandgap thermoreflectance for non-invasive thermal characterization of GaN-based wafers," *Applied Physics Letters,* vol. 113, p. 102101, 2018.
[111] C. Kittel, P. McEuen, and P. McEuen, *Introduction to solid state physics* vol. 8: Wiley New York, 1996.
[112] B. G. Streetman and S. Banerjee, *Solid state electronic devices*: Prentice-Hall of India, 2001.
[113] S. Pearton, F. Ren, M. Tadjer, and J. Kim, "Perspective: Ga2O3 for ultra-high power rectifiers and MOSFETS," *Journal of Applied Physics,* vol. 124, p. 220901, 2018.
[114] A. Aleksov, M. Kubovic, N. Kaeb, U. Spitzberg, A. Bergmaier, G. Dollinger*, et al.*, "Diamond field effect transistors—concepts and challenges," *Diamond and Related Materials,* vol. 12, pp. 391-398, 2003.
[115] Z. Cheng, T. Bai, J. Shi, T. Feng, Y. Wang, M. Mecklenburg*, et al.*, "Tunable Thermal Energy Transport across Diamond Membranes and Diamond-Si Interfaces by Nanoscale Graphoepitaxy," *ACS Appl Mater Interfaces,* vol. 11, pp. 18517-18527, May 22 2019.
[116] K. G. Crawford, D. Qi, J. McGlynn, T. G. Ivanov, P. B. Shah, J. Weil*, et al.*, "Thermally Stable, High Performance Transfer Doping of Diamond using Transition Metal Oxides," *Sci Rep,* vol. 8, p. 3342, Feb 20 2018.

Accepted Manuscript Not Corrected

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Rep Authors

[117] N. Donato, N. Rouger, J. Pernot, G. Longobardi, and F. Udrea, "Diamond power devices: state of the art, modelling, figures of merit and future perspective," *Journal of Physics D: Applied Physics,* vol. 53, p. 093001, 2020.
[118] A. Giri and P. E. Hopkins, "Role of interfacial mode coupling of optical phonons on thermal boundary conductance," *Sci Rep,* vol. 7, p. 11011, Sep 8 2017.
[119] G. T. Hohensee, R. B. Wilson, and D. G. Cahill, "Thermal conductance of metal-diamond interfaces at high pressure," *Nat Commun,* vol. 6, p. 6578, Mar 6 2015.
[120] D. A. Macdonald, K. G. Crawford, A. Tallaire, R. Issaoui, and D. A. J. Moran, "Performance Enhancement of Al2O3/H-Diamond MOSFETs Utilizing Vacuum Annealing and V2O5 as a Surface Electron Acceptor," *IEEE Electron Device Letters,* vol. 39, pp. 1354-1357, 2018.
[121] C. Monachon and L. Weber, "Effect of diamond surface orientation on the thermal boundary conductance between diamond and aluminum," *Diamond and Related Materials,* vol. 39, pp. 8-13, 2013.
[122] A. W. Saxler, "Semiconductor devices having a hybrid channel layer, current aperture transistors and methods of fabricating same," ed: Google Patents, 2006.
[123] H.-C. Shin, Y. Jang, T.-H. Kim, J.-H. Lee, D.-H. Oh, S. J. Ahn*, et al.*, "Epitaxial growth of a single-crystal hybridized boron nitride and graphene layer on a wide-band gap semiconductor," *Journal of the American Chemical Society,* vol. 137, pp. 6897-6905, 2015.
[124] L. Wei, P. K. Kuo, R. L. Thomas, T. R. Anthony, and W. F. Banholzer, "Thermal conductivity of isotopically modified single crystal diamond," *Phys Rev Lett,* vol. 70, pp. 3764-3767, Jun 14 1993.
[125] B. F. Donovan and R. J. Warzoha, "A Theoretical Paradigm for Thermal Rectification via Phonon Filtering and Energy Carrier Confinement," *arXiv preprint arXiv:1908.03048,* 2019.
[126] G. Williams, J. A. Calvo, F. Faili, J. Dodson, T. Obeloer, and D. J. Twitchen, "Thermal Conductivity of Electrically Conductive Highly Boron Doped Diamond and its Applications at High Frequencies," in *2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2018, pp. 235-239.
[127] M. Ding, Y. Liu, X. Lu, Y. Li, and W. Tang, "Boron doped diamond films: A microwave attenuation material with high thermal conductivity," *Applied Physics Letters,* vol. 114, p. 162901, 2019.
[128] S. B. Reese, T. Remo, J. Green, and A. Zakutayev, "Gallium oxide power electronics: Towards silicon cost and silicon carbide performance," *Joule,* vol. 3, p. 903, 2019.
[129] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Development of gallium oxide power devices," *physica status solidi (a),* vol. 211, pp. 21-26, 2014.
[130] M. Higashiwaki, A. Kuramata, H. Murakami, and Y. Kumagai, "State-of-the-art technologies of gallium oxide power devices," *Journal of Physics D: Applied Physics,* vol. 50, p. 333002, 2017.
[131] E. Sichel, "Thermal conductivity of GaN, 25-360 K," *J. Phys. Chem. Solids,* vol. 38, pp. 330-330, 1977.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Peer Authors

[132] Z. Cheng, L. Yates, J. Shi, M. J. Tadjer, K. D. Hobart, and S. Graham, "Thermal conductance across β-Ga2O3-diamond van der Waals heterogeneous interfaces," *APL Materials,* vol. 7, p. 031118, 2019.

[133] H. Aller, X. Yu, A. J. Gellman, J. A. Malen, and A. J. McGaughey, "Thermal Conductance of β-Ga 2 O 3/Metal Interfaces," in *2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2018, pp. 567-571.

[134] G. Simin, X. Hu, N. Ilinskaya, A. Kumar, A. Koudymov, J. Zhang*, et al.*, "7.5 kW/mm2 current switch using AlGaN/GaN metal-oxide-semiconductor heterostructure field effect transistors on SiC substrates," *Electronics Letters,* vol. 36, pp. 2043-2044, 2000.

[135] H. C. Nochetto, N. R. Jankowski, and A. Bar-Cohen, "GaN HEMT junction temperature dependence on diamond substrate anisotropy and thermal boundary resistance," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2012.

[136] B. F. Donovan, C. J. Szwejkowski, J. C. Duda, R. Cheaito, J. T. Gaskins, C. Y. Peter Yang*, et al.*, "Thermal boundary conductance across metal-gallium nitride interfaces from 80 to 450 K," *Applied Physics Letters,* vol. 105, p. 203502, 2014.

[137] A. Sarua, H. Ji, K. P. Hilton, D. J. Wallis, M. J. Uren, T. Martin*, et al.*, "Thermal Boundary Resistance Between GaN and Substrate in AlGaN/GaN Electronic Devices," *IEEE Transactions on Electron Devices,* vol. 54, pp. 3152-3158, 2007.

[138] A. Manoi, J. W. Pomeroy, N. Killat, and M. Kuball, "Benchmarking of Thermal Boundary Resistance in AlGaN/GaN HEMTs on SiC Substrates: Implications of the Nucleation Layer Microstructure," *IEEE Electron Device Letters,* vol. 31, pp. 1395-1397, 2010.

[139] N. Killat, M. Montes, J. W. Pomeroy, T. Paskova, K. R. Evans, J. Leach*, et al.*, "Thermal Properties of AlGaN/GaN HFETs on Bulk GaN Substrates," *IEEE Electron Device Letters,* vol. 33, pp. 366-368, 2012.

[140] J. Kuzmík, S. Bychikhin, D. Pogany, C. Gaquière, E. Pichonat, and E. Morvan, "Investigation of the thermal boundary resistance at the III-Nitride/substrate interface using optical methods," *Journal of Applied Physics,* vol. 101, p. 054508, 2007.

[141] G. J. Riedel, J. W. Pomeroy, K. P. Hilton, J. O. Maclean, D. J. Wallis, M. J. Uren*, et al.*, "Reducing thermal resistance of AlGaN/GaN electronic devices using novel nucleation layers," *IEEE Electron Device Letters,* vol. 30, pp. 103-106, 2008.

[142] N. G. Sahoo, S. Rana, J. W. Cho, L. Li, and S. H. Chan, "Polymer nanocomposites based on functionalized carbon nanotubes," *Progress in Polymer Science,* vol. 35, pp. 837-867, 2010.

[143] Z. Cheng, F. Mu, L. Yates, T. Suga, and S. Graham, "Interfacial Thermal Conductance across Room-Temperature Bonded GaN-Diamond Interfaces for GaN-on-Diamond Devices," *arXiv preprint arXiv:1909.01556,* 2019.

[144] C. Dundar and N. Donmezer, "Thermal Characterization of Field Plated AlGaN/GaN HEMTs," in *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2019, pp. 755-760.

Accepted Manuscript. Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Prior Authors

[145] B. C. Daly, H. J. Maris, A. V. Nurmikko, M. Kuball, and J. Han, "Optical pump-and-probe measurement of the thermal conductivity of nitride thin films," *Journal of Applied Physics,* vol. 92, pp. 3820-3824, 2002.

[146] F. N. Donmezer, M. Islam, S. Graham, and D. Yoder, "Modeling the hotspot temperature in AlGaN/GaN high electron mobility transistors using a non-gray phonon BTE solver," in *ASME 2012 International Mechanical Engineering Congress and Exposition*, 2012, pp. 1175-1188.

[147] A. A. Wilson, N. R. Jankowski, F. L. Nouketcha, and R. Tompkins, "Kapitza resistance at the two-dimensional electron gas interface," presented at the 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, Las Vegas, NV, USA, 2019.

[148] R. Trew, G. Bilbro, W. Kuang, Y. Liu, and H. Yin, "Microwave AlGaN/GaN HFETs," *IEEE Microwave Magazine,* vol. 6, pp. 56-66, 2005.

[149] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy*, et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 85, pp. 3222-3233, 1999.

[150] M. Asif Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, "High electron mobility transistor based on a GaN-AlxGa1−xN heterojunction," *Applied Physics Letters,* vol. 63, pp. 1214-1215, 1993.

[151] M. Meneghini, G. Meneghesso, and E. Zanoni, *Power GaN Devices*: Springer, 2017.

[152] P. Ning, Z. Liang, and F. Wang, "Power module and cooling system thermal performance evaluation for HEV application," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 2, pp. 487-495, 2014.

[153] Y.-F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices,* vol. 48, pp. 586-590, 2001.

[154] Y.-F. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar*, et al.*, "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Letters,* vol. 25, pp. 117-119, 2004.

[155] Y. C. Chou, D. Leung, I. Smorchkova, M. Wojtowicz, R. Grundbacher, L. Callejo*, et al.*, "Degradation of AlGaN/GaN HEMTs under elevated temperature lifetesting," *Microelectronics Reliability,* vol. 44, pp. 1033-1038, 2004.

[156] A. Bar-Cohen, J. J. Maurer, and A. Sivananthan, "Near-junction microfluidic cooling for wide bandgap devices," *MRS Advances,* vol. 1, pp. 181-195, 2016.

[157] S. Lee, R. Vetury, J. D. Brown, S. R. Gibb, W. Z. Cai, J. Sun*, et al.*, "Reliability assessment of AlGaN/GaN HEMT technology on SiC for 48V applications," in *2008 IEEE International Reliability Physics Symposium*, 2008, pp. 446-449.

[158] S. Choi, E. R. Heller, D. Dorsey, R. Vetury, and S. Graham, "The impact of bias conditions on self-heating in AlGaN/GaN HEMTs," *IEEE transactions on electron devices,* vol. 60, pp. 159-162, 2012.

[159] S. Choi, E. Heller, D. Dorsey, R. Vetury, and S. Graham, "The impact of mechanical stress on the degradation of AlGaN/GaN high electron mobility transistors," *Journal of Applied Physics,* vol. 114, p. 164501, 2013.

Accepted Manuscript Not Copyedited

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Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[160] M. Kuball, M. Ťapajna, R. J. T. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes," *Microelectronics Reliability,* vol. 51, pp. 195-200, 2011.

[161] H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang, and D. Y. Peide, "High-Performance Depletion/Enhancement-ode $\beta $-Ga2O3 on Insulator (GOOI) Field-Effect Transistors With Record Drain Currents of 600/450 mA/mm," *IEEE Electron Device Letters,* vol. 38, pp. 103-106, 2016.

[162] M. James, "Thermal challenges in power electronics," in *IEE Colloquium on Thermal Management in Power Electronics Systems*, 1993, pp. 1/1-1/2.

[163] D. Dibra, M. Stecher, S. Decker, A. Lindemann, J. Lutz, and C. Kadow, "On the origin of thermal runaway in a trench power MOSFET," *IEEE Transactions on Electron Devices,* vol. 58, pp. 3477-3484, 2011.

[164] C. Buttay, C. Raynaud, H. Morel, G. Civrac, M.-L. Locatelli, and F. Morel, "Thermal stability of silicon carbide power diodes," *IEEE Transactions on electron devices,* vol. 59, pp. 761-769, 2012.

[165] E. Douglas, C. Chang, B. Gila, M. Holzworth, K. Jones, L. Liu*, et al.*, "Investigation of the effect of temperature during off-state degradation of AlGaN/GaN high electron mobility transistors," *Microelectronics Reliability,* vol. 52, pp. 23-28, 2012.

[166] Y. Wu, C.-Y. Chen, and J. A. del Alamo, "Activation energy of drain-current degradation in GaN HEMTs under high-power DC stress," *Microelectronics Reliability,* vol. 54, pp. 2668-2674, 2014.

[167] E. R. Heller and A. Crespo, "Electro-thermal modeling of multifinger AlGaN/GaN HEMT device operation including thermal substrate effects," *Microelectronics Reliability,* vol. 48, pp. 45-50, 2008.

[168] Y. Wu, C.-Y. Chen, and J. A. Del Alamo, "Temperature-accelerated degradation of GaN HEMTs under high-power stress: Activation energy of drain-current degradation," in *JEDEC ROCS Workshop*, 2014, pp. 69-73.

[169] R. A. Coutu, R. A. Lake, B. D. Christiansen, E. R. Heller, C. A. Bozada, B. S. Poling*, et al.*, "Benefits of Considering More than Temperature Acceleration for GaN HEMT Life Testing," *Electronics,* vol. 5, p. 32, 2016.

[170] N. Donmezer and S. Graham, "The impact of noncontinuum thermal transport on the temperature of AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices,* vol. 61, pp. 2041-2048, 2014.

[171] A. Christensen and S. Graham, "Multiscale modeling of hot spots in GaN high electron mobility transistors," in *ASME 2009 InterPACK Conference collocated with the ASME 2009 Summer Heat Transfer Conference and the ASME 2009 3rd International Conference on Energy Sustainability*, 2009, pp. 535-541.

[172] N. Donmezer, M. Islam, P. D. Yoder, and S. Graham, "The impact of nongray thermal transport on the temperature of AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices,* vol. 62, pp. 2437-2444, 2015.

[173] Q. Hao, H. Zhao, Y. Xiao, and M. B. Kronenfeld, "Electrothermal studies of GaN-based high electron mobility transistors with improved thermal designs," *International Journal of Heat and Mass Transfer,* vol. 116, pp. 496-506, 2018.

Accepted manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[174] Q. Hao, H. Zhao, and Y. Xiao, "A hybrid simulation technique for electrothermal studies of two-dimensional GaN-on-SiC high electron mobility transistors," *Journal of Applied Physics,* vol. 121, p. 204501, 2017.
[175] E. Heller, S. Choi, D. Dorsey, R. Vetury, and S. Graham, "Electrical and structural dependence of operating temperature of AlGaN/GaN HEMTs," *Microelectronics Reliability,* vol. 53, pp. 872-877, 2013.
[176] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE,* vol. 90, pp. 1022-1031, 2002.
[177] B. D. Tierney, S. Choi, S. DasGupta, J. R. Dickerson, S. Reza, R. J. Kaplar*, et al.*, "Evaluation of a "Field Cage" for Electric Field Control in GaN-Based HEMTs That Extends the Scalability of Breakdown Into the kV Regime," *IEEE Transactions on Electron Devices,* vol. 64, pp. 3740-3747, 2017.
[178] B. Chatterjee, J. Lundh, J. Dallas, H. Kim, and S. Choi, "Electro-thermal reliability study of GaN high electron mobility transistors," in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2017, pp. 1247-1252.
[179] A. Venkatachalam, W. James, and S. Graham, "Electro-thermo-mechanical modeling of GaN-based HFETs and MOSHFETs," *Semiconductor science and technology,* vol. 26, p. 085027, 2011.
[180] F. Yang and C. Dames, "Mean free path spectra as a tool to understand thermal conductivity in bulk and nanostructures," *Physical Review B,* vol. 87, p. 035437, 2013.
[181] J. P. Freedman, J. H. Leach, E. A. Preble, Z. Sitar, R. F. Davis, and J. A. Malen, "Universal phonon mean free path spectra in crystalline semiconductors at high temperature," *Scientific reports,* vol. 3, pp. 1-6, 2013.
[182] T. E. Beechem, A. E. McDonald, E. J. Fuller, A. A. Talin, C. M. Rost, J.-P. Maria*, et al.*, "Size dictated thermal conductivity of GaN," *Journal of Applied Physics,* vol. 120, p. 095104, 2016.
[183] E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, and A. J. Schmidt, "Thickness dependent thermal conductivity of gallium nitride," *Applied Physics Letters,* vol. 110, p. 031903, 2017.
[184] B. Chatterjee, C. Dundar, T. E. Beechem, E. Heller, D. Kendig, H. Kim*, et al.*, "Nanoscale electro-thermal interactions in AlGaN/GaN high electron mobility transistors," *Journal of Applied Physics,* vol. 127, p. 044502, 2020.
[185] J. Muth, J. D. Brown, M. Johnson, Z. Yu, R. Kolbas, J. Cook*, et al.*, "Absorption coefficient and refractive index of GaN, AlN and AlGaN alloys," *Materials Research Society Internet Journal of Nitride Semiconductor Research,* vol. 4, pp. 502-507, 1999.
[186] J. Hsieh, J. Hwang, H. Hwang, O. Breitschädel, and H. Schweizer, "Defect depth profiling using photoluminescence and cathodoluminescence spectroscopy: the role of oxygen on reactive ion beam etching of GaN in O2/Ar plasmas," *Applied surface science,* vol. 175, pp. 450-455, 2001.
[187] D. Brunner, H. Angerer, E. Bustarret, F. Freudenberg, R. Höpler, R. Dimitrov*, et al.*, "Optical constants of epitaxial AlGaN films and their temperature dependence," *Journal of applied physics,* vol. 82, pp. 5090-5096, 1997.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[188] T. Kawashima, H. Yoshikawa, S. Adachi, S. Fuke, and K. Ohtsuka, "Optical properties of hexagonal GaN," *Journal of applied physics,* vol. 82, pp. 3528-3535, 1997.
[189] E. D. Palik, *Handbook of optical constants of solids* vol. 3: Academic press, 1998.
[190] S. Volz, R. Carminati, P. Chantrenne, S. Dilhaire, S. Gomez, N. Trannoy*, et al.*, *Microscale and nanoscale heat transfer*: Springer, 2007.
[191] F. Donmezer, "Multiscale electro-thermal modeling of AlGaN/GaN heterostructure field effect transistors," Georgia Institute of Technology, 2013.
[192] F. N. Donmezer and S. Graham, "Phonon Mean Free Path and Thermal Conductivity Relation for Gallium Nitride," *ASTFE Digital Library,* 2015.
[193] Y. Jiang, S. Cai, Y. Tao, Z. Wei, K. Bi, and Y. Chen, "Phonon transport properties of bulk and monolayer GaN from first-principles calculations," *Computational Materials Science,* vol. 138, pp. 419-425, 2017.
[194] A. J. Minnich, J. A. Johnson, A. J. Schmidt, K. Esfarjani, M. S. Dresselhaus, K. A. Nelson*, et al.*, "Thermal conductivity spectroscopy technique to measure phonon mean free paths," *Physical review letters,* vol. 107, p. 095901, 2011.
[195] A. Minnich, "Advances in the measurement and computation of thermal phonon transport properties," *Journal of Physics: Condensed Matter,* vol. 27, p. 053202, 2015.
[196] K. T. Regner, J. P. Freedman, and J. A. Malen, "Advances in studying phonon mean free path dependent contributions to thermal conductivity," *Nanoscale and Microscale Thermophysical Engineering,* vol. 19, pp. 183-205, 2015.
[197] J. A. Johnson, A. Maznev, J. Cuffe, J. K. Eliason, A. J. Minnich, T. Kehoe*, et al.*, "Direct measurement of room-temperature nondiffusive thermal transport over micron distances in a silicon membrane," *Physical review letters,* vol. 110, p. 025901, 2013.
[198] Y. K. Koh and D. G. Cahill, "Frequency dependence of the thermal conductivity of semiconductor alloys," *Physical Review B,* vol. 76, p. 075207, 2007.
[199] K. T. Regner, D. P. Sellan, Z. Su, C. H. Amon, A. J. McGaughey, and J. A. Malen, "Broadband phonon mean free path contributions to thermal conductivity measured using frequency domain thermoreflectance," *Nature communications,* vol. 4, pp. 1-7, 2013.
[200] Y. Hu, L. Zeng, A. J. Minnich, M. S. Dresselhaus, and G. Chen, "Spectral mapping of thermal conductivity through nanoscale ballistic transport," *Nature nanotechnology,* vol. 10, pp. 701-706, 2015.
[201] T.-T. Pham, J. Pernot, G. Perez, D. Eon, E. Gheeraert, and N. Rouger, "Deep-depletion mode boron-doped monocrystalline diamond metal oxide semiconductor field effect transistor," *IEEE Electron Device Letters,* vol. 38, pp. 1571-1574, 2017.
[202] A. G. Baca, B. A. Klein, J. R. Wendt, S. M. Lepkowski, C. D. Nordquist, A. M. Armstrong*, et al.*, "RF performance of Al 0.85 Ga 0.15 N/Al 0.70 Ga 0.30 N high electron mobility transistors with 80-nm gates," *IEEE Electron Device Letters,* vol. 40, pp. 17-20, 2018.
[203] S. Muhtadi, S. M. Hwang, A. Coleman, F. Asif, G. Simin, M. Chandrashekhar*, et al.*, "High electron mobility transistors with Al 0.65 Ga 0.35 N channel layers on thick AlN/sapphire templates," *IEEE Electron Device Letters,* vol. 38, pp. 914-917, 2017.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Prior Authors

[204] J. Lemettinen, H. Okumura, T. Palacios, and S. Suihkonen, "N-polar AlN buffer growth by metal–organic vapor phase epitaxy for transistor applications," *Applied Physics Express,* vol. 11, p. 101002, 2018.
[205] S. B. Reese, T. Remo, J. Green, and A. Zakutayev, "How much will gallium oxide power electronics cost?," *Joule,* vol. 3, pp. 903-907, 2019.
[206] M. Handwerg, R. Mitdank, Z. Galazka, and S. Fischer, "Temperature-dependent thermal conductivity and diffusivity of a Mg-doped insulating β-Ga2O3 single crystal along [100],[010] and [001]," *Semiconductor Science and Technology,* vol. 31, p. 125006, 2016.
[207] C. J. Szwejkowski, N. C. Creange, K. Sun, A. Giri, B. F. Donovan, C. Constantin*, et al.*, "Size effects in the thermal conductivity of gallium oxide (β-Ga2O3) films grown via open-atmosphere annealing of gallium nitride," *Journal of Applied Physics,* vol. 117, p. 084308, 2015.
[208] M. Slomski, N. Blumenschein, P. Paskov, J. Muth, and T. Paskova, "Anisotropic thermal conductivity of β-Ga2O3 at elevated temperatures: Effect of Sn and Fe dopants," *Journal of Applied Physics,* vol. 121, p. 235104, 2017.
[209] M. Bogner, A. Hofer, G. Benstetter, H. Gruber, and R. Y. Fu, "Differential 3ω method for measuring thermal conductivity of AlN and Si3N4 thin films," *Thin Solid Films,* vol. 591, pp. 267-270, 2015.
[210] I. Albar and N. Donmezer, "Phonon Mean Free Path-Thermal Conductivity Relation in AlN," in *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2019, pp. 127-130.
[211] L. Zhang, H. Yan, G. Zhu, S. Liu, Z. Gan, and Z. Zhang, "Effect of Substrate Surface on Deposition of AlGaN: A Molecular Dynamics Simulation," *Crystals,* vol. 8, p. 279, 2018.
[212] M. H. Wong, Y. Morikawa, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Characterization of channel temperature in Ga2O3 metal-oxide-semiconductor field-effect transistors by electrical measurements and thermal modeling," *Applied Physics Letters,* vol. 109, p. 193503, 2016.
[213] N. Kumar, C. Joishi, Z. Xia, S. Rajan, and S. Kumar, "Electro-Thermal Simulation of Delta-Doped $\boldsymbol {\beta} $-Ga 2 O 3 Field Effect Transistors," in *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2019, pp. 370-375.
[214] S. A. Russell, A. Pérez-Tomás, C. F. McConville, C. A. Fisher, D. P. Hamilton, P. A. Mawby*, et al.*, "Heteroepitaxial beta-Ga 2 O 3 on 4H-SiC for an FET with reduced self heating," *IEEE Journal of the Electron Devices Society,* vol. 5, pp. 256-261, 2017.
[215] B. Chatterjee, A. Jayawardena, E. Heller, D. W. Snyder, S. Dhar, and S. Choi, "Thermal characterization of gallium oxide Schottky barrier diodes," *Review of Scientific Instruments,* vol. 89, p. 114903, 2018.
[216] S. Jo, G. Yoo, and J. Heo, "Modeling and Simulation Study of Reduced Self-Heating in Bottom-Gate β-Ga 2 O 3 MISFETs with a h-BN Gate Insulator," *Journal of the Korean Physical Society,* vol. 74, pp. 1171-1175, 2019.
[217] Z. Hu, K. Nomoto, W. Li, R. Jinno, T. Nakamura, D. Jena*, et al.*, "1.6 kV vertical Ga 2 O 3 FinFETs with source-connected field plates and normally-off operation,"

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Prior Authors

in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, pp. 483-486.

[218] F. N. Donmezer, W. James, and S. Graham, "The thermal response of gallium nitride HFET devices grown on silicon and SiC substrates," *ECS Transactions,* vol. 41, p. 13, 2011.

[219] A. Giri and P. E. Hopkins, "A Review of Experimental and Computational Advances in Thermal Boundary Conductance and Nanoscale Thermal Transport across Solid Interfaces," *Advanced Functional Materials,* p. 1903857, 2019.

[220] K. E. Goodson and Y. S. Ju, "Heat conduction in novel electronic films," *Annual Review of Materials Science,* vol. 29, pp. 261-293, 1999.

[221] A. Sood, E. Pop, M. Asheghi, and K. E. Goodson, "The heat conduction renaissance," presented at the IEEE ITHERM, San Diego, California, USA, 2018.

[222] J. Kimling, A. Philippi-Kobs, J. Jacobsohn, H. P. Oepen, and D. G. Cahill, "Thermal conductance of interfaces with amorphous SiO2 measured by time-resolved magneto-optic Kerr-effect thermometry," *Physical Review B,* vol. 95, 2017.

[223] A. Giri, S. W. King, W. A. Lanford, A. B. Mei, D. Merrill, L. Li*, et al.*, "Interfacial Defect Vibrations Enhance Thermal Transport in Amorphous Multilayers with Ultrahigh Thermal Boundary Conductance," *Adv Mater,* vol. 30, p. e1804097, Nov 2018.

[224] B. C. Gundrum, D. G. Cahill, and R. S. Averback, "Thermal conductance of metal-metal interfaces," *Physical Review B,* vol. 72, 2005.

[225] R. B. Wilson and D. G. Cahill, "Experimental validation of the interfacial form of the Wiedemann-Franz law," *Phys Rev Lett,* vol. 108, p. 255901, Jun 22 2012.

[226] R. Cheaito, K. Hattar, J. T. Gaskins, A. K. Yadav, J. C. Duda, T. E. Beechem*, et al.*, "Thermal flux limited electron Kapitza conductance in copper-niobium multilayers," *Applied Physics Letters,* vol. 106, p. 093114, 2015.

[227] R. M. Costescu, M. A. Wall, and D. G. Cahill, "Thermal conductance of epitaxial interfaces," *Physical Review B,* vol. 67, 2003.

[228] R. B. Wilson, B. A. Apgar, W.-P. Hsieh, L. W. Martin, and D. G. Cahill, "Thermal conductance of strongly bonded metal-oxide interfaces," *Physical Review B,* vol. 91, 2015.

[229] J. T. Gaskins, G. Kotsonis, A. Giri, S. Ju, A. Rohskopf, Y. Wang*, et al.*, "Thermal Boundary Conductance Across Heteroepitaxial ZnO/GaN Interfaces: Assessment of the Phonon Gas Model," *Nano Lett,* vol. 18, pp. 7469-7477, Dec 12 2018.

[230] W. Park, A. Sood, J. Park, M. Asheghi, R. Sinclair, and K. E. Goodson, "Enhanced thermal conduction through nanostructured interfaces," *Nanoscale and Microscale Thermophysical Engineering,* vol. 21, pp. 134-144, 2017.

[231] E. Lee, T. Zhang, T. Yoo, Z. Guo, and T. Luo, "Nanostructures Significantly Enhance Thermal Transport across Solid Interfaces," *ACS Appl Mater Interfaces,* vol. 8, pp. 35505-35512, Dec 28 2016.

[232] T. S. English, J. C. Duda, J. L. Smoyer, D. A. Jordan, P. M. Norris, and L. V. Zhigilei, "Enhancing and tuning phonon transport at vibrationally mismatched solid-solid interfaces," *Physical Review B,* vol. 85, 2012.

[233] Z. Ge, D. G. Cahill, and P. V. Braun, "Thermal conductance of hydrophilic and hydrophobic interfaces," *Phys Rev Lett,* vol. 96, p. 186101, May 12 2006.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[234] H. Harikrishna, W. A. Ducker, and S. T. Huxtable, "The influence of interface bonding on thermal transport through solid–liquid interfaces," *Applied Physics Letters,* vol. 102, p. 251606, 2013.
[235] A. Giri and P. E. Hopkins, "Spectral analysis of thermal boundary conductance across solid/classical liquid interfaces: A molecular dynamics study," *Applied Physics Letters,* vol. 105, p. 033106, 22 July 2014 2014.
[236] S. Shenogin, A. Bodapati, P. Keblinski, and A. J. H. McGaughey, "Predicting the thermal conductivity of inorganic and polymeric glasses: The role of anharmonicity," *Journal of Applied Physics,* vol. 105, p. 034906, 2009.
[237] Y. Wang and P. Keblinski, "Role of wetting and nanoscale roughness on thermal conductance at liquid-solid interface," *Applied Physics Letters,* vol. 99, p. 073112, 19 Aug 2011 2011.
[238] K. Saaskilahti, J. Oksanen, J. Tulkki, and S. Volz, "Spectral mapping of heat transfer mechanisms at liquid-solid interfaces," *Phys Rev E,* vol. 93, p. 052141, May 2016.
[239] D. Huang, R. Ma, T. Zhang, and T. Luo, "Origin of Hydrophilic Surface Functionalization-Induced Thermal Conductance Enhancement across Solid-Water Interfaces," *ACS Appl Mater Interfaces,* vol. 10, pp. 28159-28165, Aug 22 2018.
[240] M. D. Losego, M. E. Grady, N. R. Sottos, D. G. Cahill, and P. V. Braun, "Effects of chemical bonding on heat transport across interfaces," *Nat Mater,* vol. 11, pp. 502-6, Apr 22 2012.
[241] S. Majumdar, J. A. Sierra-Suarez, S. N. Schiffres, W. L. Ong, C. F. Higgs, 3rd, A. J. McGaughey*, et al.*, "Vibrational mismatch of metal leads controls thermal conductance of self-assembled monolayer junctions," *Nano Lett,* vol. 15, pp. 2985-91, May 13 2015.
[242] W.-P. Hsieh, A. S. Lyons, E. Pop, P. Keblinski, and D. G. Cahill, "Pressure tuning of the thermal conductance of weak interfaces," *Physical Review B,* vol. 84, 2011.
[243] Y. Chalopin and S. Volz, "A microscopic formulation of the phonon transmission at the nanoscale," *Applied Physics Letters,* vol. 103, p. 051602, 2013.
[244] Y. Chalopin, N. Mingo, J. Diao, D. Srivastava, and S. Volz, "Large effects of pressure induced inelastic channels on interface thermal conductance," *Applied Physics Letters,* vol. 101, p. 221903, 2012.
[245] K. Sääskilahti, J. Oksanen, J. Tulkki, and S. Volz, "Role of anharmonic phonon scattering in the spectrally decomposed thermal conductance at planar interfaces," *Physical Review B,* vol. 90, 2014.
[246] T. Feng, Y. Zhong, J. Shi, and X. Ruan, "Unexpected high inelastic phonon transport across solid-solid interface: Modal nonequilibrium molecular dynamics simulations and Landauer analysis," *Physical Review B,* vol. 99, 2019.
[247] K. Gordiz and A. Henry, "Phonon Transport at Crystalline Si/Ge Interfaces: The Role of Interfacial Modes of Vibration," *Sci Rep,* vol. 6, p. 23139, Mar 16 2016.
[248] A. Giri, J. L. Braun, and P. E. Hopkins, "Implications of Interfacial Bond Strength on the Spectral Contributions to Thermal Boundary Conductance across Solid, Liquid, and Gas Interfaces: A Molecular Dynamics Study," *The Journal of Physical Chemistry C,* vol. 120, pp. 24847-24856, 2016.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[249] T. Murakami, T. Hori, T. Shiga, and J. Shiomi, "Probing and tuning inelastic phonon conductance across finite-thickness interface," *Applied Physics Express,* vol. 7, p. 121801, 2014.
[250] P. E. Hopkins, J. C. Duda, and P. M. Norris, "Anharmonic Phonon Interactions at Interfaces and Contributions to Thermal Boundary Conductance," *Journal of Heat Transfer,* vol. 133, 2011.
[251] J. C. Duda, P. M. Norris, and P. E. Hopkins, "On the Linear Temperature Dependence of Phonon Thermal Boundary Conductance in the Classical Limit," *Journal of Heat Transfer,* vol. 133, 2011.
[252] P. E. Hopkins, "Multiple phonon processes contributing to inelastic scattering during thermal boundary conductance at solid interfaces," *Journal of Applied Physics,* vol. 106, p. 013528, 2009.
[253] R. J. Stevens, A. N. Smith, and P. M. Norris, "Measurement of Thermal Boundary Conductance of a Series of Metal-Dielectric Interfaces by the Transient Thermoreflectance Technique," *Journal of Heat Transfer,* vol. 127, pp. 315-322, 2005.
[254] M. A. Panzer, H. M. Duong, J. Okawa, J. Shiomi, B. L. Wardle, S. Maruyama*, et al.*, "Temperature-dependent phonon conduction and nanotube engagement in metalized single wall carbon nanotube films," *Nano Lett,* vol. 10, pp. 2395-400, Jul 14 2010.
[255] H.-K. Lyeo and D. G. Cahill, "Thermal conductance of interfaces between highly dissimilar materials," *Physical Review B,* vol. 73, 2006.
[256] W. Mayer, W. F. Schiela, J. Yuan, M. Hatefipour, W. L. Sarney, S. P. Svensson*, et al.*, "Superconducting proximity effect in InAsSb surface quantum wells with in-situ Al contact," *arXiv preprint arXiv:1909.12571,* 2019.
[257] Z. Tian, K. Esfarjani, and G. Chen, "Enhancing phonon transmission across a Si/Ge interface by atomic roughness: First-principles study with the Green's function method," *Physical Review B,* vol. 86, p. 235304, 2012.
[258] E. Lee, T. Zhang, T. Yoo, Z. Guo, and T. Luo, "Nanostructures significantly enhance thermal transport across solid interfaces," *ACS applied materials & interfaces,* vol. 8, pp. 35505-35512, 2016.
[259] C. A. Polanco, R. Rastgarkafshgarkolaei, J. Zhang, N. Q. Le, P. M. Norris, and A. W. Ghosh, "Design rules for interfacial thermal conductance: Building better bridges," *Physical Review B,* vol. 95, p. 195303, 2017.
[260] J. C. Duda, P. E. Hopkins, T. E. Beechem, J. L. Smoyer, and P. M. Norris, "Inelastic phonon interactions at solid–graphite interfaces," *Superlattices and Microstructures,* vol. 47, pp. 550-555, 2010.
[261] D. Kechrakos, "The role of interface disorder in the thermal boundary conductivity between two crystals," *Journal of Physics: Condensed Matter,* vol. 3, pp. 1443-1452, 1991.
[262] J. Shi, Y. Dong, T. Fisher, and X. Ruan, "Thermal transport across carbon nanotube-graphene covalent and van der Waals junctions," *Journal of Applied Physics,* vol. 118, p. 044302, 2015.
[263] P. E. Hopkins, T. Beechem, J. C. Duda, K. Hattar, J. F. Ihlefeld, M. A. Rodriguez*, et al.*, "Influence of anisotropy on thermal boundary conductance at solid interfaces," *Physical Review B,* vol. 84, 2011.

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Accepted Manuscript Not Copyedited

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[264] M. Li, J. S. Kang, H. D. Nguyen, H. Wu, T. Aoki, and Y. Hu, "Anisotropic Thermal Boundary Resistance across 2D Black Phosphorus: Experiment and Atomistic Modeling of Interfacial Energy Transport," *Adv Mater,* vol. 31, p. e1901021, Aug 2019.

[265] A. Sergeev, "Electronic Kapitza conductance due to inelastic electron-boundary scattering," *Physical Review B,* vol. 58, pp. 199-202, 1999.

[266] Z. Lu, Y. Wang, and X. Ruan, "Metal/dielectric thermal interfacial transport considering cross-interface electron-phonon coupling: Theory, two-temperature molecular dynamics, and thermal circuit," *Physical Review B,* vol. 93, 2016.

[267] W. S. Capinski and H. J. Maris, "Improved apparatus for picosecond pump-and-probe optical measurements," *Review of Scientific Instruments,* vol. 67, pp. 2720-2726, 1996.

[268] R. Landauer, "Spatial variation of currents and fields due to localized scatterers in metallic conduction," *IBM Journal of Research and Development,* vol. 1, pp. 223-231, 1957.

[269] W. Little, "The transport of heat between dissimilar solids at low temperatures," *Canadian Journal of Physics,* vol. 37, pp. 334-349, 1959.

[270] S. Simons, "On the thermal contact resistance between insulators," *Journal of Physics C: Solid State Physics,* vol. 7, p. 4048, 1974.

[271] Y. Chu, J. Shi, K. Miao, Y. Zhong, P. Sarangapani, T. S. Fisher*, et al.*, "Thermal boundary resistance predictions with non-equilibrium Green's function and molecular dynamics simulations," *Applied Physics Letters,* vol. 115, p. 231601, 2019.

[272] P. K. Schelling, S. R. Phillpot, and P. Keblinski, "Phonon wave-packet dynamics at semiconductor interfaces by molecular-dynamics simulation," *Applied Physics Letters,* vol. 80, pp. 2484-2486, 2002.

[273] Z. T. Tian, B. E. White, and Y. Sun, "Phonon wave-packet interference and phonon tunneling based energy transport across nanostructured thin films," *Applied Physics Letters,* vol. 96, p. 263113, 2010.

[274] J. Shi, J. Lee, Y. Dong, A. Roy, T. S. Fisher, and X. Ruan, "Dominant phonon polarization conversion across dimensionally mismatched interfaces: Carbon-nanotube–graphene junction," *Physical Review B,* vol. 97, 2018.

[275] M. Hu, P. Keblinski, and P. K. Schelling, "Kapitza conductance of silicon–amorphous polyethylene interfaces by molecular dynamics simulations," *Physical Review B,* vol. 79, 2009.

[276] R. J. Stevens, L. V. Zhigilei, and P. M. Norris, "Effects of temperature and disorder on thermal boundary conductance at solid–solid interfaces: Nonequilibrium molecular dynamics simulations," *International Journal of Heat and Mass Transfer,* vol. 50, pp. 3977-3989, 2007.

[277] J. Shi, Y. Zhong, T. S. Fisher, and X. Ruan, "Decomposition of the Thermal Boundary Resistance across Carbon Nanotube-Graphene Junctions to Different Mechanisms," *ACS Appl Mater Interfaces,* vol. 10, pp. 15226-15231, May 2 2018.

[278] K. Gordiz, M. G. Muraleedharan, and A. Henry, "Interface conductance modal analysis of a crystalline Si-amorphous SiO2interface," *Journal of Applied Physics,* vol. 125, p. 135102, 2019.

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Accepted Manuscript. Not Copyedited

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[279] K. Gordiz and A. Henry, "A formalism for calculating the modal contributions to thermal interface conductance," *New Journal of Physics,* vol. 17, p. 103002, 2015.
[280] J. Dai and Z. Tian, "Anharmonicity strongly enhancing thermal interface conductance: A new anharmonic atomistic Green's function formalism," *arXiv preprint arXiv:1910.01266,* 2019.
[281] Z. Cheng, B. M. Foley, T. Bougher, L. Yates, B. A. Cola, and S. Graham, "Thermal rectification in thin films driven by gradient grain microstructure," *Journal of Applied Physics,* vol. 123, p. 095114, 2018.
[282] Z. Cheng, V. D. Wheeler, T. Bai, J. Shi, M. J. Tadjer, T. Feygelson*, et al.*, "Integration of Atomic Layer Epitaxy Crystalline Ga2O3 on Diamond for Thermal Management," *arXiv preprint arXiv:1908.08665,* 2019.
[283] Z. Cheng, Y. R. Koh, H. Ahmad, R. Hu, J. Shi, M. E. Liao*, et al.*, "Thermal Conductance Across Harmonic-matched Epitaxial Al-sapphire Heterointerfaces: A Benchmark for Metal-nonmetal Interfaces," *arXiv preprint arXiv:1906.05484,* 2019.
[284] F. Mu, Z. Cheng, J. Shi, S. Shin, B. Xu, J. Shiomi*, et al.*, "High Thermal Boundary Conductance across Bonded Heterogeneous GaN-SiC Interfaces," *ACS Appl Mater Interfaces,* vol. 11, pp. 33428-33434, Sep 11 2019.
[285] M. E. DeCoster, K. E. Meyer, B. D. Piercy, J. T. Gaskins, B. F. Donovan, A. Giri*, et al.*, "Density and size effects on the thermal conductivity of atomic layer deposited TiO2 and Al2O3 thin films," *Thin Solid Films,* vol. 650, pp. 71-77, 2018.
[286] R. Li, K. Gordiz, A. Henry, P. E. Hopkins, E. Lee, and T. Luo, "Effect of light atoms on thermal transport across solid-solid interfaces," *Phys Chem Chem Phys,* vol. 21, pp. 17029-17035, Aug 21 2019.
[287] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao*, et al.*, "Superior thermal conductivity of single-layer graphene," *Nano letters,* vol. 8, pp. 902-907, 2008.
[288] T.-H. Han, H. Kim, S.-J. Kwon, and T.-W. Lee, "Graphene-based flexible electronic devices," *Materials Science and Engineering: R: Reports,* vol. 118, pp. 1-43, 2017.
[289] F. Schwierz, J. Pezoldt, and R. Granzner, "Two-dimensional materials and their prospects in transistor electronics," *Nanoscale,* vol. 7, pp. 8261-8283, 2015.
[290] Z. Yan, D. L. Nika, and A. A. Balandin, "Thermal properties of graphene and few-layer graphene: applications in electronics," *IET Circuits, Devices & Systems,* vol. 9, pp. 4-12, 2015.
[291] Y. Zhang, A. Rubio, and G. Le Lay, "Emergent elemental two-dimensional materials beyond graphene," *Journal of Physics D: Applied Physics,* vol. 50, p. 053004, 2017.
[292] W. Paszkowicz, J. Pelka, M. Knapp, T. Szyszko, and S. Podsiadlo, "Lattice parameters and anisotropic thermal expansion of hexagonal boron nitride in the 10–297.5 K temperature range," *Applied Physics A,* vol. 75, pp. 431-435, 2002.
[293] J. Bao, K. Jeppson, M. Edwards, Y. Fu, L. Ye, X. Lu*, et al.*, "Synthesis and applications of two-dimensional hexagonal boron nitride in electronics manufacturing," *Electronic Materials Letters,* vol. 12, pp. 1-16, 2016.

Accepted Manuscript Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Prior Authors

[294] H. Gholivand and N. Donmezer, "Phonon mean free path in few layer graphene, hexagonal boron nitride, and composite bilayer h-BN/graphene," *IEEE Transactions on Nanotechnology,* vol. 16, pp. 752-758, 2017.
[295] S. Wachter, D. K. Polyushkin, O. Bethge, and T. Mueller, "A microprocessor based on a two-dimensional semiconductor," *Nature communications,* vol. 8, pp. 1-6, 2017.
[296] S. Larentis, B. Fallahazad, H. C. Movva, K. Kim, A. Rai, T. Taniguchi*, et al.*, "Reconfigurable complementary monolayer MoTe2 field-effect transistors for integrated circuits," *ACS nano,* vol. 11, pp. 4832-4839, 2017.
[297] L. Lindsay and D. Broido, "Enhanced thermal conductivity and isotope effect in single-layer hexagonal boron nitride," *Physical Review B,* vol. 84, p. 155421, 2011.
[298] L. Lindsay, D. Broido, and N. Mingo, "Flexural phonons and thermal transport in graphene," *Physical Review B,* vol. 82, p. 115427, 2010.
[299] W. Cai, A. L. Moore, Y. Zhu, X. Li, S. Chen, L. Shi*, et al.*, "Thermal transport in suspended and supported monolayer graphene grown by chemical vapor deposition," *Nano letters,* vol. 10, pp. 1645-1651, 2010.
[300] d. Ghosh, I. Calizo, D. Teweldebrhan, E. P. Pokatilov, D. L. Nika, A. A. Balandin*, et al.*, "Extremely high thermal conductivity of graphene: Prospects for thermal management applications in nanoelectronic circuits," *Applied Physics Letters,* vol. 92, p. 151911, 2008.
[301] J. J. Bae, H. Y. Jeong, G. H. Han, J. Kim, H. Kim, M. S. Kim*, et al.*, "Thickness-dependent in-plane thermal conductivity of suspended MoS2 grown by chemical vapor deposition," *Nanoscale,* vol. 9, pp. 2541-2547, 2017.
[302] W. Li, J. Carrete, and N. Mingo, "Thermal conductivity and phonon linewidths of monolayer MoS2 from first principles," *Applied Physics Letters,* vol. 103, p. 253103, 2013.
[303] A. Moridi, L. Zhang, W. Liu, S. Duvall, A. Brawley, Z. Jiang*, et al.*, "Characterisation of high thermal conductivity thin-film substrate systems and their interface thermal resistance," *Surface and Coatings Technology,* vol. 334, pp. 233-242, 2018.
[304] X. Li, J. Zhang, A. A. Puretzky, A. Yoshimura, X. Sang, Q. Cui*, et al.*, "Isotope-Engineering the Thermal Conductivity of Two-Dimensional MoS2," *ACS nano,* vol. 13, pp. 2481-2489, 2019.
[305] A. Taube, J. Judek, A. Łapińska, and M. Zdrojek, "Temperature-dependent thermal properties of supported MoS2 monolayers," *ACS applied materials & interfaces,* vol. 7, pp. 5061-5065, 2015.
[306] J. Zhang, Y. Hong, X. Wang, Y. Yue, D. Xie, J. Jiang*, et al.*, "Phonon Thermal Properties of Transition-Metal Dichalcogenides MoS2 and MoSe2 Heterostructure," *The Journal of Physical Chemistry C,* vol. 121, pp. 10336-10344, 2017.
[307] P. Yasaei, C. J. Foss, K. Karis, A. Behranginia, A. I. El-Ghandour, A. Fathizadeh*, et al.*, "Interfacial Thermal Transport in Monolayer MoS2-and Graphene-Based Devices," *Advanced Materials Interfaces,* vol. 4, p. 1700334, 2017.
[308] E. Yalon, O. B. Aslan, K. K. H. Smithe, C. J. McClellan, S. V. Suryavanshi, F. Xiong*, et al.*, "Temperature-Dependent Thermal Boundary Conductance of

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

Monolayer MoS2 by Raman Thermometry," *ACS Appl Mater Interfaces,* vol. 9, pp. 43013-43020, Dec 13 2017.

[309] C. Stieger, A. Szabo, T. Bunjaku, and M. Luisier, "Ab-initio modeling of self-heating in single-layer MoS 2 transistors," in *2017 75th Annual Device Research Conference (DRC)*, 2017, pp. 1-2.

[310] H. Zhang, H. Wang, S. Xiong, H. Han, S. Volz, and Y. Ni, "Multiscale modeling of heat dissipation in 2D transistors based on phosphorene and silicene," *The Journal of Physical Chemistry C,* vol. 122, pp. 2641-2647, 2018.

[311] F. Nasri, M. F. B. Aissa, and H. Belmabrouk, "Nanoheat conduction performance of black phosphorus field-effect transistor," *IEEE Transactions on Electron Devices,* vol. 64, pp. 2765-2769, 2017.

[312] M. F. B. Aissa, H. Rezgui, F. Nasri, H. Belmabrouk, and A. Guizani, "Thermal transport in graphene field-effect transistors with ultrashort channel length," *Superlattices and Microstructures,* vol. 128, pp. 265-273, 2019.

[313] W. Zhang, Q. Wang, Y. Chen, Z. Wang, and A. T. S. Wee, "Van der Waals stacked 2D layered materials for optoelectronics," *2D Materials,* vol. 3, p. 022001, 2016.

[314] L. Britnell, R. Gorbachev, R. Jalil, B. Belle, F. Schedin, A. Mishchenko*, et al.*, "Field-effect tunneling transistor based on vertical graphene heterostructures," *Science,* vol. 335, pp. 947-950, 2012.

[315] A. Behranginia, Z. Hemmat, A. K. Majee, C. J. Foss, P. Yasaei, Z. Aksamija*, et al.*, "Power Dissipation of WSe2 Field-Effect Transistors Probed by Low-Frequency Raman Thermometry," *ACS Appl Mater Interfaces,* vol. 10, pp. 24892-24898, Jul 25 2018.

[316] E. Yalon, C. J. McClellan, K. K. H. Smithe, M. Munoz Rojo, R. L. Xu, S. V. Suryavanshi*, et al.*, "Energy Dissipation in Monolayer MoS2 Electronics," *Nano Lett,* vol. 17, pp. 3429-3433, Jun 14 2017.

[317] S. Vaziri, E. Yalon, M. M. Rojo, S. V. Suryavanshi, H. Zhang, C. J. McClellan*, et al.*, "Ultrahigh thermal isolation across heterogeneously layered two-dimensional materials," *Science advances,* vol. 5, p. eaax1325, 2019.

[318] B. M. Foley, S. C. Hernandez, J. C. Duda, J. T. Robinson, S. G. Walton, and P. E. Hopkins, "Modifying Surface Energy of Graphene via Plasma-Based Chemical Functionalization to Tune Thermal and Electrical Transport at Metal Interfaces," *Nano Lett,* vol. 15, pp. 4876-82, Aug 12 2015.

[319] Y. K. Koh, M. H. Bae, D. G. Cahill, and E. Pop, "Heat conduction across monolayer and few-layer graphenes," *Nano Lett,* vol. 10, pp. 4363-8, Nov 10 2010.

[320] P. E. Hopkins, M. Baraket, E. V. Barnat, T. E. Beechem, S. P. Kearney, J. C. Duda*, et al.*, "Manipulating thermal conductance at metal-graphene contacts via chemical functionalization," *Nano Lett,* vol. 12, pp. 590-5, Feb 8 2012.

[321] Z. Chen, W. Jang, W. Bao, C. N. Lau, and C. Dames, "Thermal contact resistance between graphene and silicon dioxide," *Applied Physics Letters,* vol. 95, p. 161910, 2009.

[322] X. Li, Y. Yan, L. Dong, J. Guo, A. Aiyiti, X. Xu*, et al.*, "Thermal conduction across a boron nitride and SiO2interface," *Journal of Physics D: Applied Physics,* vol. 50, p. 104002, 2017.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Prior Authors

[323] P. Yasaei, Z. Hemmat, C. J. Foss, S. J. Li, L. Hong, A. Behranginia, *et al.*, "Enhanced Thermal Boundary Conductance in Few-Layer Ti3 C2 MXene with Encapsulation," *Adv Mater,* vol. 30, p. e1801629, Oct 2018.

[324] P. Yasaei, A. Behranginia, Z. Hemmat, A. I. El-Ghandour, C. D. Foster, and A. Salehi-Khojin, "Quantifying the limits of through-plane thermal dissipation in 2D-material-based systems," *2D Materials,* vol. 4, p. 035027, 2017.

[325] J. Yang, E. Ziade, C. Maragliano, R. Crowder, X. Wang, M. Stefancich, *et al.*, "Thermal conductance imaging of graphene contacts," *Journal of Applied Physics,* vol. 116, p. 023515, Sep 2014.

[326] K. M. Freedy, A. Giri, B. M. Foley, M. R. Barone, P. E. Hopkins, and S. McDonnell, "Titanium contacts to graphene: process-induced variability in electronic and thermal transport," *Nanotechnology,* vol. 29, p. 145201, Apr 6 2018.

[327] Z.-Y. Ong, B. Qiu, S. Xu, X. Ruan, and E. Pop, "Flexural resonance mechanism of thermal transport across graphene-SiO2 interfaces," *Journal of Applied Physics,* vol. 123, p. 115107, 2018.

[328] T. Feng, W. Yao, Z. Wang, J. Shi, C. Li, B. Cao, *et al.*, "Spectral analysis of nonequilibrium molecular dynamics: Spectral phonon temperature and local nonequilibrium in thin films and across interfaces," *Physical Review B,* vol. 95, 2017.

[329] Z. Xu and M. J. Buehler, "Heat dissipation at a graphene-substrate interface," *J Phys Condens Matter,* vol. 24, p. 475305, Nov 28 2012.

[330] H. Wang, J. Gong, Y. Pei, and Z. Xu, "Thermal transfer in graphene-interfaced materials: contact resistance and interface engineering," *ACS Appl Mater Interfaces,* vol. 5, pp. 2599-603, Apr 10 2013.

[331] C. J. Foss and Z. Aksamija, "Quantifying thermal boundary conductance of 2D–3D interfaces," *2D Materials,* vol. 6, p. 025019, 2019.

[332] G. C. Correa, C. J. Foss, and Z. Aksamija, "Interface thermal conductance of van der Waals monolayers on amorphous substrates," *Nanotechnology,* vol. 28, p. 135402, Mar 1 2017.

[333] B. N. Persson, A. I. Volokitin, and H. Ueba, "Phononic heat transfer across an interface: thermal boundary resistance," *J Phys Condens Matter,* vol. 23, p. 045009, Feb 2 2011.

[334] B. N. Persson and H. Ueba, "Heat transfer between graphene and amorphous SiO2," *J Phys Condens Matter,* vol. 22, p. 462201, Nov 24 2010.

[335] Z.-Y. Ong, Y. Cai, and G. Zhang, "Theory of substrate-directed heat dissipation for single-layer graphene and other two-dimensional crystals," *Physical Review B,* vol. 94, 2016.

[336] J. Dulhani and B. J. Lee, "Phonon Transport through Nanoscale Contact in Tip-Based Thermal Analysis of Nanomaterials," *Nanomaterials (Basel),* vol. 7, Jul 28 2017.

[337] R. Prasher, "Thermal interface materials: historical perspective, status, and future directions," *Proceedings of the IEEE,* vol. 94, pp. 1571-1586, 2006.

[338] K.-S. Moon, H. Dong, R. Maric, S. Pothukuchi, A. Hunt, Y. Li, *et al.*, "Thermal behavior of silver nanoparticles for low-temperature interconnect applications," *Journal of electronic materials,* vol. 34, pp. 168-175, 2005.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[339] J. Xiang and L. T. Drzal, "Electron and phonon transport in Au nanoparticle decorated graphene nanoplatelet nanostructured paper," *ACS applied materials & interfaces,* vol. 3, pp. 1325-1332, 2011.

[340] R. J. Warzoha, D. Zhang, G. Feng, and A. S. Fleischer, "Engineering interfaces in carbon nanostructured mats for the creation of energy efficient thermal interface materials," *Carbon,* vol. 61, pp. 441-457, 2013.

[341] R. J. Warzoha and A. S. Fleischer, "Heat flow at nanoparticle interfaces," *Nano Energy,* vol. 6, pp. 137-158, 2014.

[342] R. J. Warzoha and A. S. Fleischer, "Effect of graphene layer thickness and mechanical compliance on interfacial heat flow and thermal conduction in solid–liquid phase change materials," *ACS applied materials & interfaces,* vol. 6, pp. 12868-12876, 2014.

[343] T. Tong, Y. Zhao, L. Delzeit, A. Kashani, M. Meyyappan, and A. Majumdar, "Dense vertically aligned multiwalled carbon nanotube arrays as thermal interface materials," *IEEE Transactions on Components and Packaging Technologies,* vol. 30, pp. 92-100, 2007.

[344] Q. Ngo, B. A. Cruden, A. M. Cassell, G. Sims, M. Meyyappan, J. Li*, et al.*, "Thermal interface properties of Cu-filled vertically aligned carbon nanofiber arrays," *Nano Letters,* vol. 4, pp. 2403-2407, 2004.

[345] M. Panzer, G. Zhang, D. Mann, X. Hu, E. Pop, H. Dai*, et al.*, "Thermal properties of metal-coated vertically aligned single-wall nanotube arrays," *Journal of Heat Transfer,* vol. 130, p. 052401, 2008.

[346] H. Yu, L. Li, and Y. Zhang, "Silver nanoparticle-based thermal interface materials with ultra-low thermal resistance for power electronics applications," *Scripta Materialia,* vol. 66, pp. 931-934, 2012.

[347] B. Płatek, T. Fałat, P. Matkowski, J. Felba, and A. Mościcki, "Heat transfer through the interface containing sintered nanoAg based thermal interface material," in *Proceedings of the 5th Electronics System-integration Technology Conference (ESTC)*, 2014, pp. 1-4.

[348] R. S. Prasher and J. C. Matayabas, "Thermal contact resistance of cured gel polymeric thermal interface material," *IEEE Transactions on Components and Packaging Technologies,* vol. 27, pp. 702-709, 2004.

[349] A. N. Smith, N. R. Jankowski, and L. M. Boteler, "Measurement of high-performance thermal interfaces using a reduced scale steady-state tester and infrared microscopy," *Journal of Heat Transfer,* vol. 138, 2016.

[350] A. Bar-Cohen, K. Matin, and S. Narumanchi, "Nanothermal interface materials: technology review and recent results," *Journal of Electronic Packaging,* vol. 137, 2015.

[351] R. J. Warzoha, L. Boteler, A. N. Smith, E. Getto, and B. F. Donovan, "Steady-state measurements of thermal transport across highly conductive interfaces," *International Journal of Heat and Mass Transfer,* vol. 130, pp. 874-881, 2019.

[352] C. Yegin, N. Nagabandi, X. Feng, C. King, M. Catalano, J. K. Oh*, et al.*, "Metal–Organic–Inorganic Nanocomposite Thermal Interface Materials with Ultralow Thermal Resistances," *ACS applied materials & interfaces,* vol. 9, pp. 10120-10127, 2017.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Prior Authors

[353] N. Balachander, I. Seshadri, R. J. Mehta, L. S. Schadler, T. Borca-Tasciuc, P. Keblinski*, et al.*, "Nanowire-filled polymer composites with ultrahigh thermal conductivity," *Applied Physics Letters,* vol. 102, p. 093117, 2013.

[354] Z. Han and A. Fina, "Thermal conductivity of carbon nanotubes and their polymer nanocomposites: A review," *Progress in Polymer Science,* vol. 36, pp. 914-944, 2011.

[355] Y. Liu and S. Kumar, "Polymer/carbon nanotube nano composite fibers--a review," *ACS Appl Mater Interfaces,* vol. 6, pp. 6069-87, May 14 2014.

[356] H. Ma and Z. Tian, "Toward enhancing thermal conductivity of polymer-based thin films for microelectronics cooling," in *2017 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2017, pp. 390-393.

[357] O. Bubnova, Z. U. Khan, A. Malti, S. Braun, M. Fahlman, M. Berggren*, et al.*, "Optimization of the thermoelectric figure of merit in the conducting polymer poly(3,4-ethylenedioxythiophene)," *Nat Mater,* vol. 10, pp. 429-33, Jun 2011.

[358] A. A. Wilson, M. Munoz Rojo, B. Abad, J. A. Perez, J. Maiz, J. Schomacker*, et al.*, "Thermal conductivity measurements of high and low thermal conductivity films using a scanning hot probe method in the 3omega mode and novel calibration strategies," *Nanoscale,* vol. 7, pp. 15404-12, Oct 7 2015.

[359] K. Zhang, M. Davis, J. Qiu, L. Hope-Weeks, and S. Wang, "Thermoelectric properties of porous multi-walled carbon nanotube/polyaniline core/shell nanocomposites," *Nanotechnology,* vol. 23, p. 385701, Sep 28 2012.

[360] P. Bonnet, D. Sireude, B. Garnier, and O. Chauvet, "Thermal properties and percolation in carbon nanotube-polymer composites," *Applied Physics Letters,* vol. 91, p. 201910, 2007.

[361] F. H. Gojny, M. H. Wichmann, B. Fiedler, I. A. Kinloch, W. Bauhofer, A. H. Windle*, et al.*, "Evaluation and identification of electrical and thermal conduction mechanisms in carbon nanotube/epoxy composites," *Polymer,* vol. 47, pp. 2036-2045, 2006.

[362] C. Guthy, F. Du, S. Brand, K. I. Winey, and J. E. Fischer, "Thermal conductivity of single-walled carbon nanotube/PMMA nanocomposites," *Journal of heat transfer,* vol. 129, pp. 1096-1099, 2007.

[363] R. Haggenmueller, C. Guthy, J. R. Lukes, J. E. Fischer, and K. I. Winey, "Single wall carbon nanotube/polyethylene nanocomposites: thermal and electrical conductivity," *Macromolecules,* vol. 40, pp. 2417-2421, 2007.

[364] A. A. Wilson, T. Borca-Tasciuc, H. Wang, and C. Yu, "Thermal conductivity of double-wall carbon nanotube-polyanaline composites measured by a non-contact scanning hot probe technique. ," presented at the 16th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), Orlando, Florida, USA, 2017.

[365] B. A. Cola, "Carbon nanotubes as high performance thermal interface materials," *Electron. Cooling Mag,* vol. 16, pp. 10-15, 2010.

[366] A. M. Marconnet, N. Yamamoto, M. A. Panzer, B. L. Wardle, and K. E. Goodson, "Thermal conduction in aligned carbon nanotube–polymer nanocomposites with high packing density," *ACS nano,* vol. 5, pp. 4818-4825, 2011.

Accepted manuscript. Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Prior Authors

[367] Q. Liao, Z. Liu, W. Liu, C. Deng, and N. Yang, "Extremely high thermal conductivity of aligned carbon nanotube-polyethylene composites," *Scientific reports,* vol. 5, p. 16543, 2015.
[368] M. Wuttig and N. Yamanda, "Phase-change materials for rewriteable data storage," *Nature Materials,* vol. 6, p. 824, 2007.
[369] G. W. Burr, M. J. BrightSky, A. Sebastian, H.-Y. Cheng, J.-Y. Wu, S. Kim*, et al.*, "Recent Progress in Phase-ChangeMemory Technology," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,* vol. 6, pp. 146-162, 2016.
[370] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y. C. Chen, R. M. Shelby*, et al.*, "Phase-change random access memory: A scalable technology," *IBM Journal of Research and Development,* vol. 52, p. 465, 2008.
[371] R. M. Young, P. Borodulin, N. El-Hinnawy, A. Ezis, M. R. King, V. Luu*, et al.*, "Improvements in GeTe-based Phase Change RF Switches," presented at the 2018 IEEE/MTT-S International Microwave Symposium- IMS, 2018.
[372] N. El-Hinnawy, P. Borodulin, B. Wagner, M. R. King, J. S. Mason, E. B. Jones*, et al.*, "A Four-Terminal, Inline, Chalcogenide Phase-Change RF Switch Using an Independent Resistive Heater for Thermal Actuation," *IEEE Electron Device Letters,* vol. 34, pp. 1313-1315, 2013.
[373] G. W. Burr, R. M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler*, et al.*, "Neuromorphic computing using non-volatile memor," *Advances in Physics X,* vol. 2, p. 89, 2017.
[374] A. Sebastian, M. Le Gallo, G. W. Burr, S. Kim, M. BrightSky, and E. Eleftheriou, "Tutorial: Brain-inspired computing using phase-change memory devices," *Journal of Applied Physics,* vol. 124, p. 111101, 2018.
[375] M. Wuttig, H. Bhaskaran, and T. Taubner, "Phase-change materials for non-volatile photonic applications," *Nature Photonics,* vol. 11, pp. 465-476, 2017.
[376] B. Gholipour, "The promise of phase-change materials," *Science,* vol. 366, pp. 186-187, 2019.
[377] C.-Y. Hwang, G. H. Kim, J.-H. Yang, C.-S. Hwang, S. M. Cho, W.-J. Lee*, et al.*, "Rewritable full-color computer-generated holograms based on color-selective diffractive optical components including phase-change materials," *Nanoscale,* vol. 10, pp. 21648-21655, 2018.
[378] H.-Y. Cheng, F. Carta, W.-C. Chien, H.-L. Lung, and M. J. BrightSky, "3D cross-point phase-change memory for storage-class memory," *Journal of Physics D: Applied Physics,* vol. 52, p. 473002, 2019.
[379] J. Choe, "Intel 3D Xpoint memory die removed from Intel Optane," *Tech Insights,* vol. 18, 2017.
[380] P. Guo, A. Sarangan, and I. Agha, "A Review of Germanium-Antimony-Telluride Phase Change Materials for Non-Volatile Memories and Optical Modulators," *Applied Sciences,* vol. 9, p. 530, 2019.
[381] H. Hayat, K. I. Kohary, and C. D. Wright, "Can conventional phase-change memory devices be scaled down to single-nanometre dimensions?," *Nanotechnology,* vol. 28, p. 035202, 2017.
[382] C. Ahn, S. W. Fong, Y. Kim, S. Lee, A. Sood, C. M. Neumann*, et al.*, "Energy-Efficient Phase-Change Memory with Graphene as a Thermal Barrier," *Nano Lett,* vol. 15, pp. 6809-14, Oct 14 2015.

Accepted manuscript. Not copyedited.

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[383] C. M. Neumann, K. L. Okabe, E. Yalon, R. W. Grady, H. S. P. Wong, and E. Pop, "Engineering thermal and electrical interface properties of phase change memory with monolayer MoS2," *Applied Physics Letters,* vol. 114, p. 082103, 2019.

[384] C. Ma, J. He, J. Lu, J. Zhu, and Z. Hu, "Impact of scaling on thermoelectric heating process in the reset operation of phase-change memory cells," *Japanese Journal of Applied Physics,* vol. 58, p. 105003, 2019.

[385] B. Kersting and M. Salinga, "Exploiting nanoscale effects in phase change memories," *Faraday Discuss,* vol. 213, pp. 357-370, Feb 18 2019.

[386] S. Durai, S. Raj, and A. Manivannan, "Impact of Thermal Boundary Resistance on the Performance and Scaling of Phase Change Memory Device," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* pp. 1-1, 2019.

[387] P. Wang, Y. Chen, S. Li, S. Raju, L. Wang, L. Zhang*, et al.*, "Low Power Phase Change Memory With Vertical Carbon Nanotube Electrode," *IEEE Journal of the Electron Devices Society,* vol. 5, pp. 362-366, 2017.

[388] Y. Yin and S. Hosaka, "Controlled promotion of crystallization for application to multilevel phase-change memory," *Applied Physics Letters,* vol. 100, p. 253503, 2012.

[389] D. Ventrice, P. Fantini, A. Redaelli, A. Pirovano, A. Benvenuti, and F. Pellizzer, "A Phase Change Memory Compact Model for Multilevel Applications," *IEEE Electron Device Letters,* vol. 28, pp. 973-975, 2007.

[390] N. Papandreou, A. Pantazi, A. Sebastian, E. Eleftheriou, M. Breitwisch, C. Lam*, et al.*, "Estimation of amorphous fraction in multilevel phase-change memory cells," *Solid-State Electronics,* vol. 54, pp. 991-996, 2010.

[391] J.-S. Moon, H.-C. Seo, K.-A. Son, K. Lee, D. Zehnder, and H. Tai, "5 THz figure-of-merit reliable phase-change RF switches for millimeter-wave applications," in *2018 IEEE/MTT-S International Microwave Symposium-IMS*, 2018, pp. 836-838.

[392] N. El-Hinnawy, P. Borodulin, E. B. Jones, B. Wagner, M. R. King, J. S. Mason*, et al.*, "12.5 THz Fco GeTe Inline Phase-Change Switch Technology for Reconfigurable RF and Switching Applications " presented at the 2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2014.

[393] M. Wang, F. Lin, and M. Rais-Zadeh, "An X-band reconfigurable bandpass filter using phase change RF switches," in *2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2016, pp. 38-41.

[394] N. El-Hinnawy, P. Borodulin, A. Ezis, C. Furrow, C. Padilla, M. King*, et al.*, "Substrate agnostic monolithic integration of the inline phase-change switch technology," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, pp. 1-4.

[395] M. Wang, F. Lin, and M. Rais-Zadeh, "Performance measurements and non-linearity modeling of GeTe phase change RF switches with direct and indirect heating schemes," in *2015 IEEE MTT-S International Microwave Symposium*, 2015, pp. 1-4.

[396] L. Chau, J. G. Ho, X. Lan, G. Altvater, R. M. Young, N. El-Hinnawy*, et al.*, "Optically controlled GeTe phase change switch and its applications in reconfigurable antenna arrays," in *Open Architecture/Open Business Model Net-Centric Systems and Defense Transformation 2015*, 2015, p. 947905.

Accepted Manuscript Copyrighted

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[397] G. Slovin, M. Xu, J. Paramesh, T. E. Schlesinger, and J. A. Bain, "AlN Barriers for Capacitance Reduction in Phase-Change RF Switches," *IEEE Electron Device Letters,* vol. 37, pp. 568-571, 2016.

[398] N. El-Hinnawy, P. Borodulin, M. R. King, C. Furrow, C. R. Padilla, A. Ezis*, et al.*, "Experimental Demonstration of AlN Heat Spreaders for the Monolithic Integration of Inline Phase-Change Switches," *IEEE Electron Device Letters,* vol. 39, pp. 610-613, 2018.

[399] P. Guo, J. A. Burrow, G. A. Sevison, A. Sood, M. Asheghi, J. R. Hendrickson*, et al.*, "Improving the performance of Ge2Sb2Te5 materials via nickel doping: Towards RF-compatible phase-change devices," *Applied Physics Letters,* vol. 113, p. 171903, 2018.

[400] R. E. Simpson, P. Fons, A. V. Kolobov, T. Fukaya, M. Krbal, T. Yagi*, et al.*, "Interfacial phase-change memory," *Nat Nanotechnol,* vol. 6, pp. 501-5, Jul 3 2011.

[401] R. Liu, X. Zhou, J. Zhai, J. Song, P. Wu, T. Lai*, et al.*, "Multilayer SnSb4-SbSe Thin Films for Phase Change Materials Possessing Ultrafast Phase Change Speed and Enhanced Stability," *ACS Appl Mater Interfaces,* vol. 9, pp. 27004-27013, Aug 16 2017.

[402] E. Yalon, I. M. Datye, J.-S. Moon, K.-A. Son, K. Lee, and E. Pop, "Energy-Efficient Indirectly Heated Phase Change RF Switch," *IEEE Electron Device Letters,* vol. 40, pp. 455-458, 2019.

[403] R. M. Young, N. El-Hinnawy, P. Borodulin, B. P. Wagner, M. R. King, E. B. Jones*, et al.*, "Thermal analysis of an indirectly heat pulsed non-volatile phase change material microwave switch," *Journal of Applied Physics,* vol. 116, p. 054504, 2014.

[404] S. Ambrogio, N. Ciocchini, M. Laudato, V. Milo, A. Pirovano, P. Fantini*, et al.*, "Unsupervised Learning by Spike Timing Dependent Plasticity in Phase Change Memory (PCM) Synapses," *Front Neurosci,* vol. 10, p. 56, 2016.

[405] M. Suri, O. Bichler, D. Querlioz, B. Traoré, O. Cueto, L. Perniola*, et al.*, "Physical aspects of low power synapses based on phase change memory devices," *Journal of Applied Physics,* vol. 112, p. 054904, 2012.

[406] T. Tuma, A. Pantazi, M. Le Gallo, A. Sebastian, and E. Eleftheriou, "Stochastic phase-change neurons," *Nat Nanotechnol,* vol. 11, pp. 693-9, Aug 2016.

[407] R. A. Cobley, H. Hayat, and C. D. Wright, "A self-resetting spiking phase-change neuron," *Nanotechnology,* vol. 29, p. 195202, 2018.

[408] A. Pantazi, S. Wozniak, T. Tuma, and E. Eleftheriou, "All-memristive neuromorphic computing with level-tuned neurons," *Nanotechnology,* vol. 27, p. 355205, Sep 2 2016.

[409] D.-H. Kang, H.-G. Jun, K.-C. Ryoo, H. Jeong, and H. Sohn, "Emulation of spike-timing dependent plasticity in nano-scale phase change memory," *Neurocomputing,* vol. 155, pp. 153-158, 2015.

[410] O. Bichler, M. Suri, D. Querlioz, D. Vuillaume, B. DeSalvo, and C. Gamrat, "Visual Pattern Extraction Using Energy-Efficient "2-PCM Synapse" Neuromorphic Architecture," *IEEE Transactions on Electron Devices,* vol. 59, pp. 2206-2214, 2012.

[411] T. Tuma, M. Le Gallo, A. Sebastian, and E. Eleftheriou, "Detecting Correlations Using Phase-Change Neurons and Synapses," *IEEE Electron Device Letters,* vol. 37, pp. 1238-1241, 2016.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[412] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114 ff," *IEEE solid-state circuits society newsletter,* vol. 11, pp. 33-35, 2006.
[413] B. Bailey. (2018, November 11th, 2019). The Impact Of Moore's Law Ending. *Semiconductor Engineering*.
[414] M. M. Waldrop. (2016, The chips are down for Moore's law. *International Weekly Journal of Science 530(7589)*.
[415] S. Kim, S. Choi, and W. Lu, "Comprehensive Physical Model of Dynamic Resistive Switching in an Oxide Memristor," *ACS Nano,* vol. 8, pp. 2369-2376, 2014/03/25 2014.
[416] M.-J. Lee, G.-S. Park, D. H. Seo, S. M. Kwon, H.-J. Lee, J.-S. Kim*, et al.*, "Reliable Multivalued Conductance States in TaOx Memristors through Oxygen Plasma-Assisted Electrode Deposition with in Situ-Biased Conductance State Transmission Electron Microscopy Analysis," *ACS Applied Materials & Interfaces,* vol. 10, pp. 29757-29765, 2018/09/05 2018.
[417] J. L. Pacheco, D. L. Perry, D. R. Hughart, M. Marinella, and E. Bielejec, "Electroforming-free TaOx memristors using focused ion beam irradiations," *Applied Physics A,* vol. 124, p. 626, August 20 2018.
[418] K. M. Kim, S. R. Lee, S. Kim, M. Chang, and C. S. Hwang, "Self-Limited Switching in Ta2O5/TaOx Memristors Exhibiting Uniform Multilevel Changes in Resistance," *Advanced Functional Materials,* vol. 25, pp. 1527-1534, 2015.
[419] S. Larentis, F. Nardi, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive Switching by Voltage-Driven Ion Migration in Bipolar RRAM—Part II: Modeling," *IEEE Transactions on Electron Devices,* vol. 59, pp. 2468-2475, 2012.
[420] G. Bersuker, D. C. Gilmer, D. Veksler, P. Kirsch, L. Vandelli, A. Padovani*, et al.*, "Metal oxide resistive memory switching mechanism based on conductive filament properties," *Journal of Applied Physics,* vol. 110, p. 124518, 2011.
[421] S. Clima, Y. Y. Chen, A. Fantini, L. Goux, R. Degraeve, B. Govoreanu*, et al.*, "Intrinsic Tailing of Resistive States Distributions in Amorphous HfOx and TaOx Based Resistive Random Access Memories," *Ieee Electron Device Letters,* vol. 36, pp. 769-771, Aug 2015.
[422] A. Padovani, L. Larcher, O. Pirrotta, L. Vandelli, and G. Bersuker, "Microscopic Modeling of HfOx RRAM Operations: From Forming to Switching," *Ieee Transactions on Electron Devices,* vol. 62, pp. 1998-2006, Jun 2015.
[423] A. Wedig, M. Luebben, D. Y. Cho, M. Moors, K. Skaja, V. Rana*, et al.*, "Nanoscale cation motion in TaOx, HfOx and TiOx memristive systems," *Nature Nanotechnology,* vol. 11, pp. 67-+, Jan 2016.
[424] G. Broglia, G. Ori, L. Larcher, and M. Montorsi, "Molecular dynamics simulation of amorphous HfO 2 for resistive RAM applications," *Modelling and Simulation in Materials Science and Engineering,* vol. 22, p. 065006, 2014.
[425] W. F. He, H. J. Sun, Y. X. Zhou, K. Lu, K. H. Xue, and X. S. Miao, "Customized binary and multi-level HfO2-x-based memristors tuned by oxidation conditions," *Scientific Reports,* vol. 7, Aug 2017.
[426] S.-H. Bae, S. Lee, H. Koo, L. Lin, B. H. Jo, C. Park*, et al.*, "The Memristive Properties of a Single VO2 Nanowire with Switching Controlled by Self-Heating," *Advanced Materials,* vol. 25, pp. 5098-5103, 2013.

Accepted Manuscript Not Copyrighted

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020

Journal of Electronic Packaging. Received April 17, 2020;
Accepted manuscript posted December 8, 2020. doi:10.1115/1.4049293
Section 4: U.S. Gov Employees + Pre-Authors

[427] J. Lappalainen, J. Mizsei, and M. Huotari, "Neuromorphic thermal-electric circuits based on phase-change VO2 thin-film memristor elements," *Journal of Applied Physics,* vol. 125, p. 044501, 2019.

[428] Z. Wang, S. Kumar, H.-S. P. Wong, and Y. Nishi, "Effect of thermal insulation on the electrical characteristics of NbOx threshold switches," *Applied Physics Letters,* vol. 112, p. 073102, 2018.

[429] S. Kumar, J. P. Strachan, and R. S. Williams, "Chaotic dynamics in nanoscale NbO2 Mott memristors for analogue computing," *Nature,* vol. 548, p. 318, 08/09/online 2017.

[430] S. Slesazeck, H. Mähne, H. Wylezich, A. Wachowiak, J. Radhakrishnan, A. Ascoli*, et al.*, "Physical model of threshold switching in NbO2 based memristors," *RSC Advances,* vol. 5, pp. 102318-102322, 2015.

[431] J. Greenlee, C. Petersburg, W. Calley, C. Jaye, D. Fischer, F. Alamgir*, et al.*, "In-situ oxygen x-ray absorption spectroscopy investigation of the resistance modulation mechanism in LiNbO2 memristors," *Applied Physics Letters,* vol. 100, p. 182106, 04/30 2012.

[432] G. Bersuker, D. C. Gilmer, D. Veksler, P. Kirsch, L. Vandelli, A. Padovani*, et al.*, "Metal oxide resistive memory switching mechanism based on conductive filament properties," *Journal of Applied Physics,* vol. 110, Dec 2011.

[433] D. G. Pahinkar, P. Basnet, B. Zivasatienraj, A. Weidenbach, M. West, W. A. Doolittle*, et al.*, "Computational Investigation of Nanoscale Memristor Devices for Neuromorphic Computing," in *2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2019, pp. 219-225.

[434] W. Wu, H. Wu, B. Gao, N. Deng, S. Yu, and H. Qian, "Improving Analog Switching in HfOx-Based Resistive Memory With a Thermal Enhanced Layer," *IEEE Electron Device Letters,* vol. 38, pp. 1019-1022, 2017.

[435] S. Kim, H.-D. Kim, and S.-J. Choi, "Compact Two-State-Variable Second-Order Memristor Model," *Small (Weinheim an der Bergstrasse, Germany),* vol. 12, 05/06 2016.

[436] W. He, H. Sun, Y. Zhou, K. Lu, K. Xue, and X. Miao, "Customized binary and multi-level HfO2−x-based memristors tuned by oxidation conditions," *Scientific Reports,* vol. 7, p. 10070, 2017/08/30 2017.

Accepted Manuscript Not Copyedited

Downloaded from http://asmedigitalcollection.asme.org/electronicpackaging/article-pdf/doi/10.1115/1.4049293/6600361/ep-20-1070.pdf by The Pennsylvania State University, Sukwon Choi on 24 December 2020