A Chalcogenide Based Memristor Used as a Neuromorphic Circuit Element

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***Abstract*— Memristor has been a promising candidate for designing in-memory computation architecture. In other words, such two terminal resistive switching devices can be utilized as synthetic synapse for the hardware implementation of neuromorphic computing. This work portrays some experimentally obtained attributes from chalcogenide based memristor which would act as a suitable emulator for biological synapse. Among different chalcogenides, Germanium Antimony Telluride (GST) based memristor device has been taken under consideration. Electrical characterization and suitability of a GST based memristor device as the core element for neuromorphic architecture has been investigated in this research.**

***Keywords*—— neuromorphic computation; multi state resistive switching; memristor, synthetic synapse.**

I. Introduction

Due to limitation of classical Von-Neumann computers in speed, power efficiency and parallel processing there is urgent need for novel computing architectures. Therefore, neuromorphic computing inspired by human brain has attracted researchers in recent years. Among different characterization aspects, device stability, repeatability, analog resistive switching, ultra-low power consumption, longer retention and endurance are the most primitive ones [1]. This paper proposes a 20μm^2 memristor device where Germanium Antimony Telluride (GST) is the high 'k' dielectric and the thin film GST layer has been deposited using Sputtering technique. Platinum has been used as both the top and bottom electrodes and a very thin layer of titanium has been added to promote adhesion. Fig.1 shows schematic representation for the proposed GST based memristor device along with the electrical characterization at room temperature. Zero crossing pinched hysteresis was obtained from the proposed memristor characterization [2].

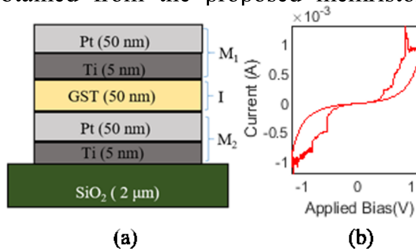

Fig.1. (a) Schematic representation of GST based memristor device (b) Variation of device current with applied bias.

II. Techniques for Determining Multi-Level Resistive Switching (MRS)

Existence of multi-level states is a very important criterion for designing neuromorphic architecture. Sweep dependent measurement techniques have been adopted to explore multiple resistive states from a GST based memristor device. This paper emphasizes on reproducible multilevel switching without the requirement of electroforming. Experimental verification for existence of several repeatable intermediate resistive states have been demonstrated.

III. Results and Discussion

This section provides results found for intermediate resistive states in between memristor off and on condition. Modulation of bias, compliance current and thermal effect have been chosen as factors governing multiple resistive states from the proposed chalcogenide based memristor device.

A. Incremental Bias dependent MRS

Variable bias dependent intermediate resistive levels were achieved at room temperature. Twenty times repeatable, stable intermediate resistive state was found at around 0.80 V sweep bias. In this case memristor device switched to the low resistive state (LRS) at around 1.20 V. Fig. 2 c shows combined plot for memristor off state (HRS), intermediate state (IRS) and on state (LRS) at room temperature.

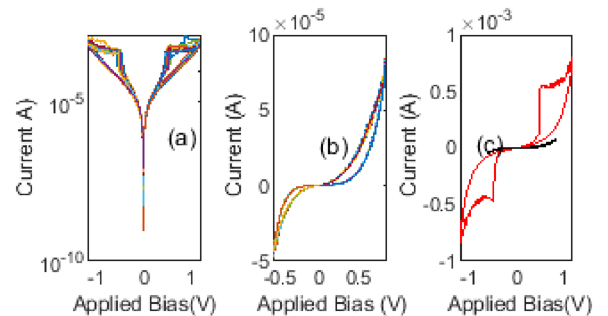

Fig.2. (a) Logarithmic plot for twenty repeatable current-voltage characterization (b) Linear plot for stable, repeatable intermediate resistive state at 0.80 V (c) Combined plot for HRS, IRS and LRS from a 20 um^2, memristor device where GST is the switching layer

B. Compliance Current dependent MRS

Next experiment is the verification of different resistive states by varying the compliance current level [3] for the memristor while keeping the applied bias always the same. Six different compliance current levels were able to produce ten distinct intermediate resistive states which have been depicted within the logarithmic plot for device characterization. Fig.3 b shows variation of both HRS and LRS states with that of compliance.

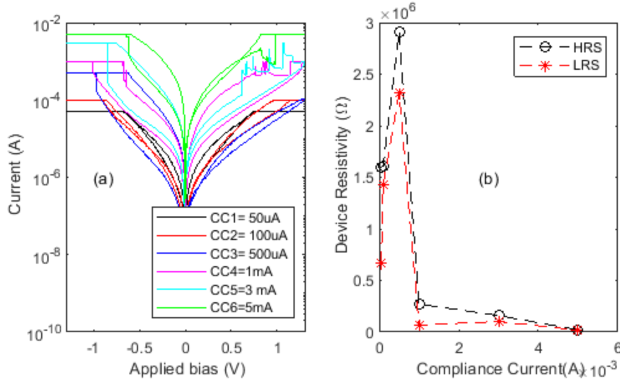

Fig.3. (a) Logarithmic plot for current voltage characterization with the variation of compliance current levels (b) Modulation of device resistive states (both HRS and LRS) with variable compliance current levels

C. Reset Voltage dependent MRS

Keeping the SET voltage the same, another experiment was done on the same device where application of repetitive negative bias produces multiple hysteresis, defining distinct intermediate resistive states with two different reset voltages [4]. In this case first we applied positive voltage to Set the device. Compliance current was set at 1 mA as the voltage was swept to 2.20 V. The resistance value of the on state was approximately 0.375 kΩ. Next, negative voltage was applied to reset the device. As the voltage was swept to -1.50 V, the current abruptly decreased around -0.75 V (1st reset). Subsequently we applied negative voltage again to sweep until -2.0 V and the resistance further decreased at around -1.250 V (2nd reset). The resistance values were approximately 0.94kΩ and after 1st reset and approximately 1.57kΩ after 2nd reset. Hence two level reset were observed from the GST based memristor device.

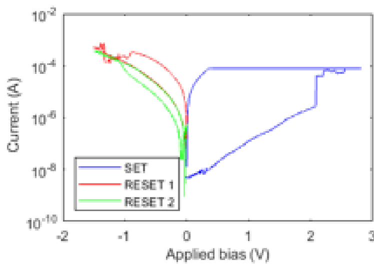

Fig.4. Logarithmic plot for reset voltage dependent multi level resistive states

D. Temperature dependent MRS

Thermal dependence of multi-level resistive states from GST memristor was characterized. Applying the same sweep voltage (0.80 V positive and 0.60 V negative) and keeping the compliance current (3 mA) the same, current voltage characterization was done at three different temperatures (room temperature: 25ºC, 55ºC and 85ºC) . Fig.5 shows logarithmic plot for multiple resistive switching states within a GST based memristor device which varies with the temperature.

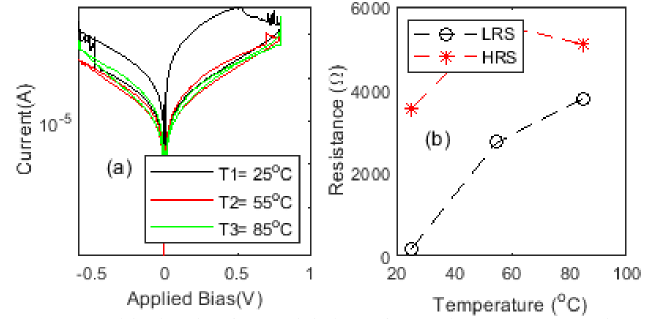

Fig.5. (a) Logarithmic plot for modulation of memristor's current voltage characterization with variation of temperature (b) Modulation of resistance levels (both HRS and LRS) with varying temperatures

IV. CONCLUSION

Biological brain shows continuous change of synaptic weight states in between maximum and minimum conductance states. These are named as intermediate resistive states. This report demonstrates experimental results for intermediate resistive states from a GST based memristor device using different techniques. Overall energy consumption from a neuromorphic system can be reduced if synaptic device is mostly cycled within these intermediate resistive states.

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