Experimental Verification of Current Conduction Mechanism for a Lithium Niobate based Memristor

Ayesha Zaman [1,z], Guru Subramanyam [1], Eunsung Shin[1], Chris Yakopcic[1], Tarek M. Taha[1], Ahmad Ehteshamul Islam[2], Sabyasachi Ganguli[2], Donald Dorsey[2] and Ajit Roy[2]
[1]University of Dayton; {zamana3, gsubramanyam1, eshin1, cyakopcic1, ttaha1}@udayton.edu
[2]Airforce Research Lab, Materials Directorate; {ahmad.islam.1.ctr, sabyasachi.ganguli.2, donald. dorsey, ajit.roy}@us.af.mil
[1,z]Ayesha Zaman: zamana3@udayton.edu

Abstract: This work presents electrical characterization and analysis of the dominant charge transport mechanism suggesting inhomogeneous, filamentary conduction for a lithium niobate switching layer based memristor for use in neuromorphic computing. Memristor conductivity has been investigated both for the high and low resistance states. It is suggested that when the device is in a high resistance state, deep trap energy level within the switching layer initiate the device conduction process. The elastic trap assisted tunneling mechanism with a simple steady state approach agrees with the experimental measurements in the high resistance state. This work considers existence of inhomogeneously distributed positively charged oxygen ions/vacancies (within the oxygen deficient switching layer) as the deep trap energy level, required for electron tunneling from memristor electrode. Alternatively, ohmic conduction was found to be the main mechanism for the memristor on state conductivity at room temperature. Existence of intermediate resistive states in the memristor's high resistive region was experimentally investigated and the elastic trap assisted tunneling mechanism for such phenomena was validated through simulation.
Keywords: Neuromorphic device; Memristor; Elastic Trap Assisted Tunneling; Charge transport, Resistive Switching

Introduction

The memristor was defined as the fourth fundamental electrical circuit element in 1971 by Prof. Leon Chua [1] and was physically realized by a research group from Hewlett Packard (HP) Labs in 2008 [2]. While resistive switching is a phenomenon that has been known for more than half a century [3], work in [2] appears to be a practical implementation, connecting the theory in [1]. Studies in this area have widely progressed within the last decade in terms of device size, power consumption, data retention, and endurance [4],[5], [6]. On chip memory-based network has been reported as a promising platform for neuro-morphic architecture design [7],[8]. One possible way of designing the memristor structure is depositing an insulating thin film layer with a high 'k' dielectric sandwiched between two conducting layers in a Metal-Insulator-Metal (MIM) structure. The value for 'k' that is preferable is between 10 and 30 [9] to provide a large enough energy bandgap. Research in memristor devices [10] suggests, the formation of a conductive filament through ion mobility is the principal reason for the pinched hysteresis observed in memristor [11],[12],[13]. Filamentary conduction through hafnium oxide-based RRAM ($Pt/HfO_x/TiN$) was reported by S. Yu et al., demonstrating the effect of the elastic trap assisted tunneling (ETAT) mechanism in the high resistance region [14]. Having inspired by the proposed mechanism mentioned in [14], our work explores a two-step steady state approach for the high resistance region through a lithium niobate based ($Pt/LiNbO_{3-x}/LiNbO_3/Pt$) memristor device. Main contributions of our current research work are as follows:

I. Investigation of conductivity mechanism for the memristor ($Pt/LiNbO_{3-x}/LiNbO_3/Pt$) using a steady state approach.

II. Demonstration of stable, analog conductivity from the proposed memristor device.

This manuscript presents characterization and simulation results for the dominant charge transport process of lithium niobate based memristor devices. Proposed charge transport mechanism was corroborated using theoretical framework and experimental validation.

Theory

In its stoichiometric state, $LiNbO_3$ is a wide band gap semiconductor [15]. In this work, it has been utilized as a memristor switching layer along with a lightly doped oxygen deficient thin film ($LiNbO_{3-x}$) using pulsed laser deposition. Knowledge of electrical conduction through the memristor is very useful in optimizing the devices for various applications, including neuromorphic computing [16],[17]. The memristor's charge transport mechanisms are analyzed segmenting the device conductivity for high resistance state (HRS) which can be thought of as the 'offstate' and low resistance state (LRS) which can be thought of as the 'onstate'. Different studies consider Poole-Frankel (P-F) emission as the principle conduction mechanism in the HRS through high k dielectrics. This was claimed to be a dominant conduction process within Si-$LiNbO_3$ heterostructure fabricated by the sol-gel method and the ion-beam sputtering method [18]. Charge transport equation for P-F mechanism is given by

$$I \sim V exp\left(\frac{\beta_{PF}\sqrt{V} - \Phi_{PF}}{kT}\right) \quad , \tag{1}$$

I and V are the device current and applied bias and k is the Boltzmann's constant. Φ_{PF} is the barrier height an electron needs to overcome and move to the oxide conduction band (E_c). The parameter β_{PF} is the P-F coefficient, which is defined as,

$$\beta_{PF} = \sqrt{\frac{q^3}{L\pi\varepsilon_o\,\varepsilon_r}} \quad , \tag{2}$$

where ε_o is the dielectric permittivity of free space and ε_r is the relative dielectric constant of the dielectric layer used in the metal-insulator-metal (MIM) structure. Also, q denotes the electronic charge and L is the thickness of the oxide layer. Next, we investigated the possibility of electrode-oxide interface modulation due to the accumulation of defects/oxygen vacancies and thus contribute to the existence of the Schottky emission. Interfacial or homogeneous switching mechanism has been explained as the modification of Schottky barrier height between the electrode and the switching layer when defects are attracted to the metal layer through the application of external bias. According to the Schottky emission, the current density (J) can be expressed as in eqn. (3)[19]

$$J = A^*\,T^2\,\exp\left(\frac{-q\Phi_B}{kT}\right)\exp\left(\frac{qV}{kT}\right) \quad , \tag{3}$$

Where A^* is the Richardson's constant, T refers to the experimental temperature and Φ_B is the Schottky barrier potential. A straight line (linear change) on a ln $(\frac{I}{T^2})$ vs $(\frac{1000}{T})$ plot for any applied bias serves as strong evidence of Schottky emission. Direct tunneling [20] applies primarily in the case of ultra-thin oxide layers (<10 nm). This mechanism can be ignored for our memristor devices, as we use a 42nm thick oxide layer. Fowler Nordheim (F-N) tunneling [21] could be dominant when very high electric field (~MV/cm) acts upon the device. Ohmic conduction [22] is applicable when the device is completely conducting and there is linear relationship between current and applied bias. In view of these, simple two step ETAT mechanism [14] using steady state approach is investigated in detail. Elastic tunneling mechanism (ballistic transport) considering mono-energetic trap has been proposed to be dominant for memristor HRS

conduction. This means electrons originating from the cathode terminal first traverse to a trap within the switching layer without any loss of energy. Then this carrier travels towards the memristor anode terminal. In this case, we have used the simplest expression for elastic tunneling probability, assuming uniform voltage drop across the switching layer without considering the image force into account. Figure 1. illustrates modulation of a memristor energy band diagram under a triangular sweep bias condition. Figure 1.a shows the energy band diagram for the possible tunneling of electrons through two step Elastic Trap Assisted Tunneling (ETAT) mechanism for memristor HRS conduction. Figure 1. b shows energy band diagram for the carrier flow for LRS conductivity due to Ohmic conduction.

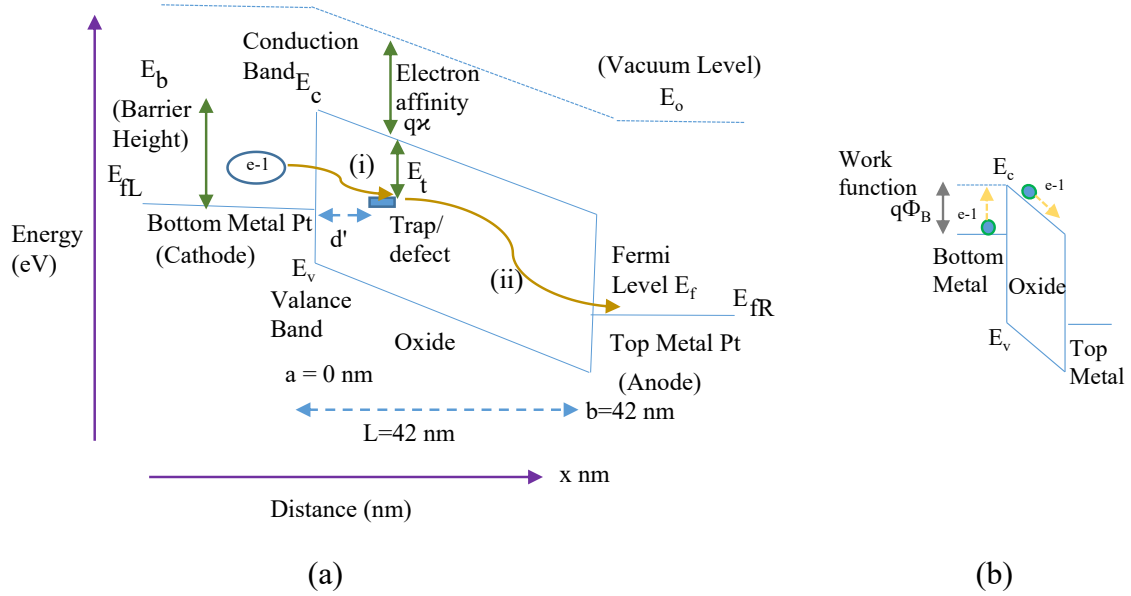


Figure 1. Modulation of energy band diagram for the lithium niobate based memristor device under external bias, (a) supporting the ETAT mechanism along HRS (b) Ohmic conduction for LRS

During the memristor HRS condition, charge carriers (electrons in this case) do not gain enough energy to overcome the large barrier height(E_b) estimated to be ~4.23 eV for the metal-dielectric interface. Probability of quantum mechanical tunneling through the interface to the oxide defect level has been taken into consideration. Tunneling would take place from the bottom electrode towards an unoccupied trap or an oxide defect. In the band diagram, E_t denotes the defect (trap) energy level and d' is the distance between the bottom electrode and the nearest trap. Arrows from left to right indicate the flow of charge carriers through the positively charged oxygen ions (traps/defects). Tunneling of charge carriers under the applied bias condition can be described in two steps. In step (i), electrons from the bottom electrode (cathode) travel towards the nearest trap position within the oxide switching layer. In this case, the trap level is at a distance from the cathode and at an energy level below the oxide conduction band minima. In step (ii) electrons transit from the defect towards the top electrode (anode). The transmission probability of an electron (T'), tunneling from the cathode is evaluated using the standard Wentzel-Kramer-Brillouin (WKB) approximation [23] as shown in eqn. (4).

$$T' = \exp\left(-\frac{4}{3\hbar q F'}\sqrt{2m_{eff}}\left(E_t^{3/2} - (E_t - F'.d')^{3/2}\right)\right), \quad (4)$$

In Eqn. (4), ħ is the reduced Planck's constant, F' is the electric field influencing the charge carriers, m_{eff} is the effective mass of an electron and d' is the trap distance from the bottom

electrode. The transition rate of the charge carriers (v_1) has been estimated using the following eqn. (5), where v_o is the characteristic vibration frequency of a trap within the oxide layer, which is equal to 10^{13} Hz [14]. Also, f_{fermi} denotes the Fermi Dirac distribution for electrons residing in the bottom electrode.

$$v_1 = v_o \cdot f_{fermi} \cdot T' \quad , \tag{5}$$

The probability that an empty energy state will be filled by an electron from the cathode is expressed in eqn. (6).

$$F_{fermi} = \frac{1}{\left(1 + \exp\left(\frac{E_b - E_t - F'.d'}{kT}\right)\right)} \quad , \tag{6}$$

The transition rate v_2 of electrons from the trap towards the anode is evaluated using eqn. (7). There the de-trapping probability of charge carriers responsible for current conduction has been expressed with the function ($1-f_{fermi}$).

$$v_2 = v_o.\left(1 - f_{fermi}\right).T' \quad , \tag{7}$$

Current 'I' in both polarity cases is determined using the following relation in eqn. (8). The term v' is the transition rate of electrons through the oxide-electrode interface (v_1 for charge trapping and v_2 for charge de-trapping). The value N' is the total trap density within the memristor switching layer.

$$I = N'.q.v' \tag{8}$$

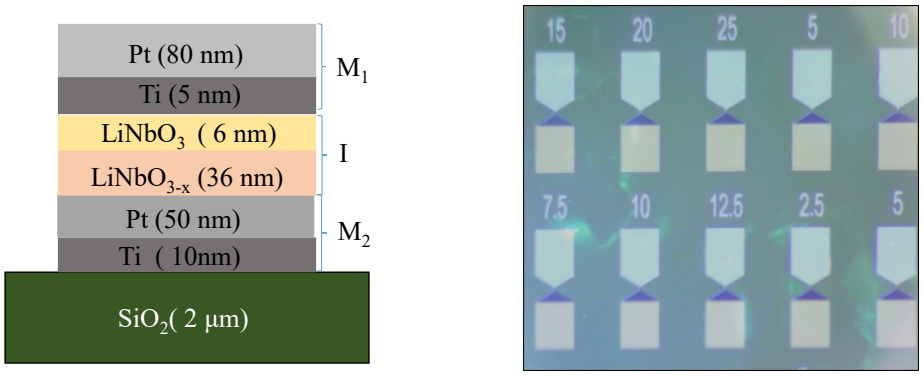
After a set voltage is applied, the memristor device is in a highly conductive state. Room temperature current voltage characterization shows almost linear relationship which would suggest ohmic conduction for the memristor LRS. The current density (J) for ohmic conduction can be expressed as in the following eqn. 9 [22], where E_A is the activation energy, μ and N' are the electron mobility and trap density respectively.

$$J = q\mu F' N' \exp\left(\frac{E_A}{2kT}\right) \tag{9}$$

Experimental

Our devices (Pt/$LiNbO_{3-x}$/$LiNbO_3$/Pt) were fabricated using the pulsed laser deposition (PLD) technique maintaining simple square geometry. A thin layer of titanium (Ti) was used to promote adhesion for both top and bottom electrodes. Reason for choosing such sequence of conducting layers is to provide a cation non-blocking and blocking metal layers at the top and bottom of the oxide thin film respectively. Our device characterization results were found to be non-volatile, stable, repetitive and showed gradual conductivity change analogous to the potentiation and depression phenomena in biological synapses. Memristors presented in this work were fabricated as MIM structures on a two-inch silicon wafer with a 2 μm thick layer of SiO_2. Platinum (Pt) was deposited for the top and bottom electrodes using an electron-beam evaporation process with a thin (~10 nm) of titanium (Ti) adhesion layer. The switching layer was deposited using PLD as explained in [24],[25]. An oxygen deficient layer was incorporated maintaining very low vacuum pressure (10^{-6} Torr). Deposition temperature of the switching layer was about 550° C. Deposited memristor switching layer comprised of oxygen deficient $LiNbO_{3-x}$ (36 nm) and $LiNbO_3$ (6 nm) sandwiched between the two electrodes. Thickness of the thin film layers were confirmed using a surface profilometer [26]. Figure 2.a shows a cross-sectional view of the memristor structure. The labels 'M_1' and 'M_2' refer to the metal layers (top and bottom electrodes respectively) and 'I' refers to the insulating layer. The memristor device dimension was varied from 2.5 μm^2 to 40 μm^2 based on the photo lithographic mask

design. Figure 2.b shows a microscopic image for memristor devices with multiple device areas.



(a) (b)

Figure 2. Thin film layers for an oxide based memristor device (a) cross-sectional view for memristor sandwiched structure (b) microscopic image for single memristor devices with variable overlap areas

While performing electrical characterization using the Keithley 2400 Semiconductor Characterization System (SCS), the top electrode was always connected to the (positive/negative) bias and the bottom electrode was grounded. A triangular sweep (peak to peak 1.20 V and 58. 82 Hz) was used for DC current-voltage characterization. A compliance current was set at 5mA to protect the devices from breakdown. A thermoelectric temperature controller (MELCOR MTTC 1410) was utilized to heat the thermal chuck for higher temperature measurements up to 100 ºC.

4. Results and Discussions

The bipolar resistive switching phenomena is observed from the DC characterization. A zero-crossing pinched hysteresis demonstrates memory capability present in this MIM structure. Figures 3.a and 3.b show the memristor I-V characteristics measured at temperatures of 25ºC and 95ºC respectively. Both the characterization results in figures 3.a and 3.b were obtained from a memristor device having an overlap area of 7.50 µm^2. At maximum elevated temperature (95ºC in figure 3.b) device current reaches the compliance current (CC=5 mA) limit due to LRS conduction. Bidirectional arrows (in blue) show the characterization regions under investigation for HRS and LRS of the memristor with the overlap area 7.50 µm^2.

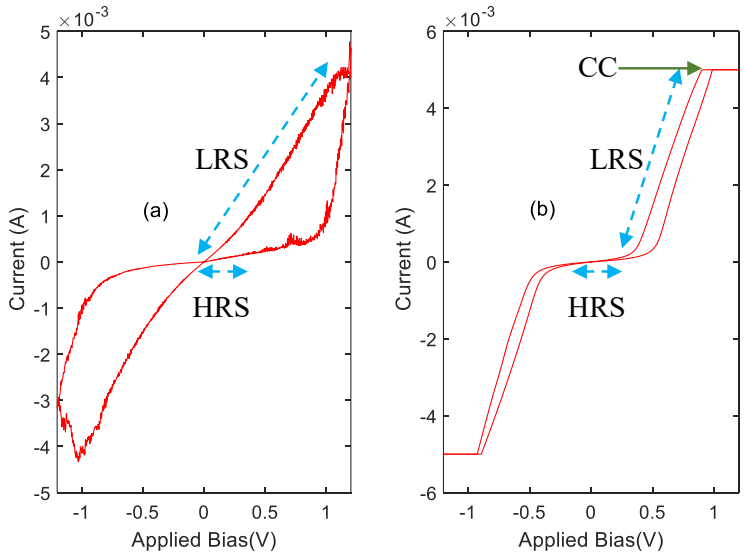


Figure 3. Electrical characterization from lithium niobate based memristor device using 5 mA compliance current (CC)(a) memristor signature characteristics at room temperature 25 ºC and (b) 95 ºC.

Set voltage is the bias required to turn the memristor device completely and causes abrupt change of device current. After the set voltage, device current increased linearly at room temperature according to the characterization results shown in figure 3.a. The temperature effect has been investigated both for memristor HRS and LRS states. During the HRS (~0.35 V bias) the device conductivity is not significantly affected at high temperature. During LRS, increase of temperature (95 ºC) would cause some decrease of carrier mobility at low bias resulting in reduction of the LRS current. This eventually reduces memristor resistance ratio (R_{off}/R_{on}) for high temperature (95 ºC) measurements. Off to on resistance ratio was obtained as (~5) using measurement results at room temperature (25 ºC). Low resistance ratio (~10) from another combination of $LiNbO_2$ based memristor device with Ni/Au metal stack was also reported in [27].After the memristor device is on, strong non-linearity with device current at high bias was observed. As per electrical characterization, the set voltage for the bilayer lithium niobate based memristor device was found to be ~1.20 V at room temperature. The set voltage for the same device at 95ºC was found to be reduced to ~ 0.95 V. Figure 4.a shows thermal variation of memristor conductivity at different bias conditions. Slope of the plot from figure 4.a provides activation energy (E_A) for the switching layer. Figure 4.b. shows activation energy for low bias 0.10V condition. From the fitted graphs for P-F conduction demonstrated using figure 4., value of relative dielectric constant (ε_r) is obtained as ~2.7242 which is much less than the known value 28.5 [28] for $LiNbO_3$. The vertical intercept of the plot in figure 4.b provides the value of estimated trap energy level for the device under consideration, which is found as 0.102 eV. This implies existence of very shallow trap level below oxide conduction band (E_c) responsible for HRS conductivity. Also, the experimentally known value of activation energy for lithium niobate varies from 1 to 1.20 eV [29]. Unrealistic values of device parameters (i.e. defect/trap energy level and relative dielectric constant) obtained from the fitting results of P-F emission model, makes it unreasonable as the primary/dominant conduction mechanism through the memristor in the HRS.

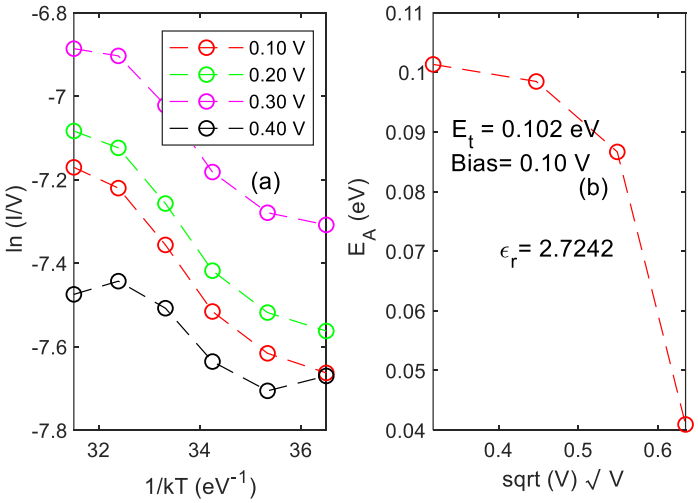


Figure 4. Investigation of Poole-Frenkel emission for memristor (HRS) (a) conductivity modulation for low bias state with thermal variation (b) plot for electron activation energy with sqrt of bias voltage. Y-intercept for the plot provides extracted trap energy level assumed to be responsible for P-F emission during HRS.

Plots in figure 5 investigated the possibility of Schottky emission for the memristor HRS. To satisfy the Schottky emission, variation of plot of device current with that of electric field should be linear irrespective of temperature changes [19]. Figure 5. b correlates the projected parameters ((ln (I/T^2))with that of $(E^{1/2})$ both for room temperature and 95°C measurements. Rather, exponential change was observed from the plot which deviates from the definition of Schottky emission. To further justify this Schottky emission for memristor HRS conductivity, we determined the Schottky barrier height from the plot in figure 5. c. As per fitting results, Schottky barrier height evaluated from the slope of figure 5.c was found as 0.005 eV. Such unrealistic value of interface layer evaluated from the fitting results demonstrated within figure 5, delineates inapplicability of the Schottky mechanism for the proposed lithium niobate based memristor device in the HRS.

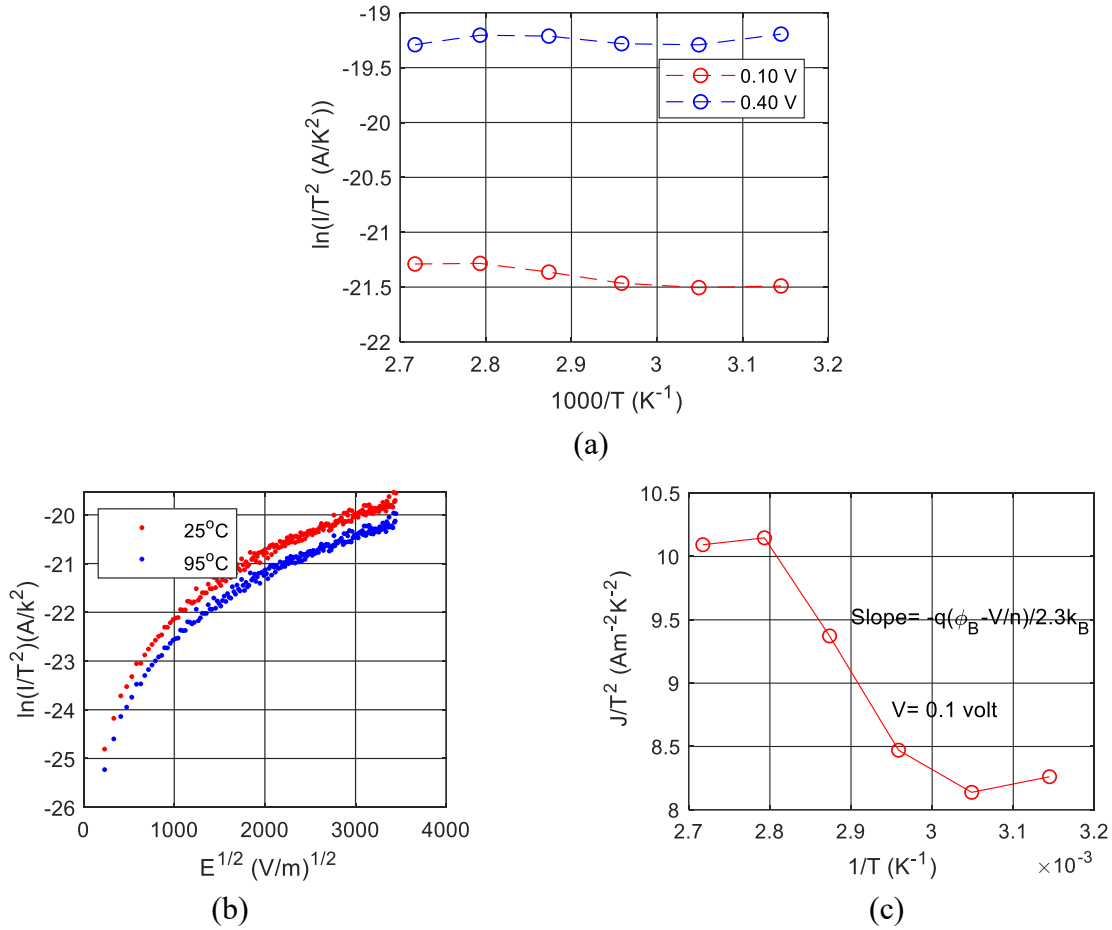


Figure 5. Fitting results for Schottky emission for bilayer lithium niobate based memristor device (a) thermal variation of memristor resistivity (b) plot for the HRS current with variation of electric field (c) extraction of Schottky barrier height as per definition mentioned in eqn. 3

In order to investigate the conduction mechanism of the ($Pt/LiNbO_{3-x}/LiNbO_3/Pt$) memristor, the current-voltage relationship is further studied. Existence of deep trap/defect level has been presumed to be responsible for memristor HRS conduction. HRS current through the device is neither affected by temperature nor by high electric field. According to the plots shown in figure 4, validation of Poole Frenkel emission was found inappropriate for HRS conduction through the memristor device. Also, Schottky emission can be ruled out from the fitting results as shown in figure 5. All these leave trap assisted tunneling mechanism to be further analyzed as the dominant mechanism for the memristor's HRS conduction. During simulation the ETAT mechanism was applied for memristor HRS, utilizing equations 4 through 8. Figure 6 summarizes simulation

results using the ETAT mechanism for the memristor device at HRS. Simulation results were obtained by estimating the effective mass of an electron as $0.05m_o$ [30]. Deep trap energy (E_C-1.145) eV level within the switching oxide is suggested to be responsible for this HRS current. Here E_c is the oxide conduction band energy level having a value 4.23 eV.

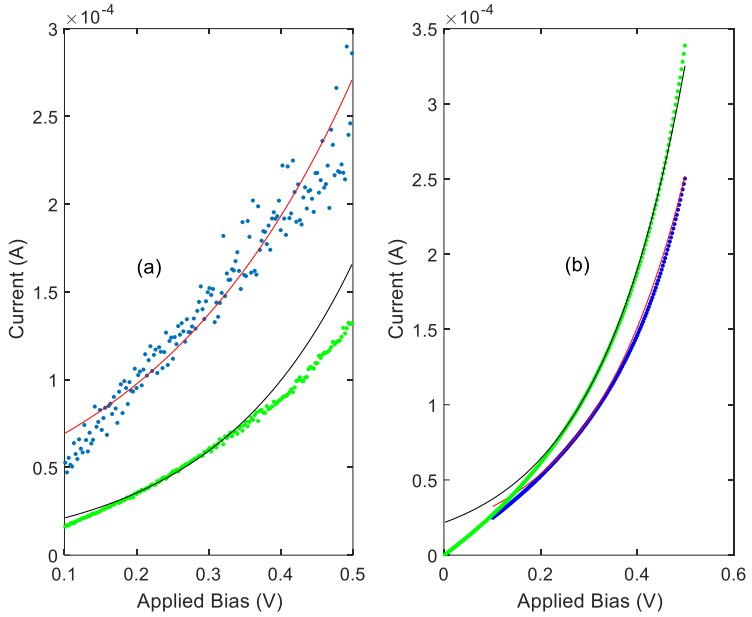


Figure 6. ETAT simulation results for lithium niobate based memristor (area 7.50 μm^2) during device HRS at (a) room temperature 25°C (b) 95°C compared with experimental results. All dotted points (blue and green dots for positive and negative polarity respectively) correspond to measured values and lines drawn (red and black lines positive and negative polarity respectively) correspond to the simulated values.

Reasonably good agreement is achieved between experimental data and the approximate response for carrier transport in the memristor's HRS. It is clear from the ETAT simulation, memristor HRS conductivity is not affected by thermal variation, rather it is the existence of unfilled deep trap energy level, which initiates electron tunneling from the cathode terminal. During simulation, deep trap energy level (distance, position, density) was found to be the same for both room temperature and 95°C measurements for the HRS (~0.35V bias). As per the expression for ohmic conduction mentioned in eqn. 9, a plot for memristor LRS current with an applied bias shows almost a linear behavior (with a slope of ~1) at room temperature as plotted in figure 7.a. LRS simulation results in figure 7.a. provide the extracted value of electron mobility μ=25 $cm^2\ V^{-1}\ s^{-1}$ from room temperature measurements which is higher than the one obtained by Ohmori et.el. in [31]. Simulation results for the memristor LRS at 95°C shown in figure 7.b confirms that the ohmic conduction prevails for the memristor LRS at low bias (~0.25 V) only. Also reduced value of electron mobility (μ=21.5 $cm^2\ V^{-1}\ s^{-1}$) was extracted from fitting results which is agreeable with high temperature effect as shown in figure 7.b.

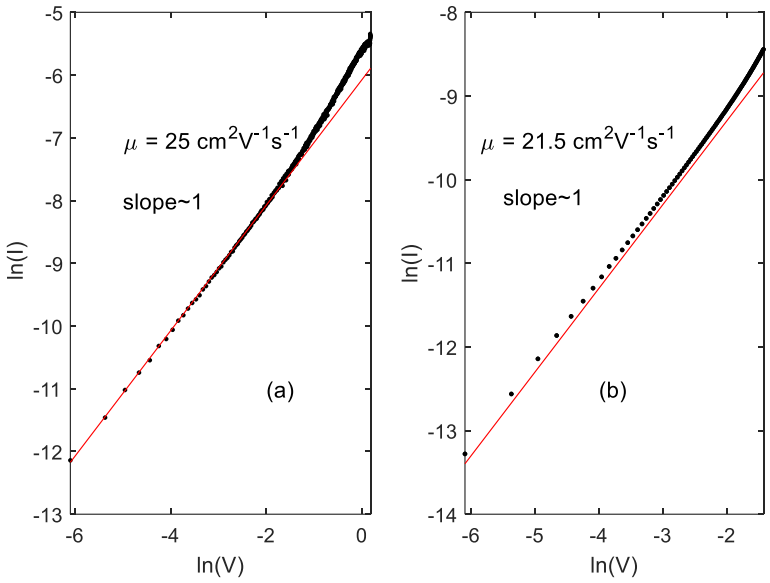


Figure 7. Simulation results plotted for LRS conductivity using ohmic conduction (a) up to high bias for 25 ºC (b) low bias (0.25 V) for 95 ºC compared to the experimental results (all dotted points and lines drawn correspond to the experimental and simulated values respectively).

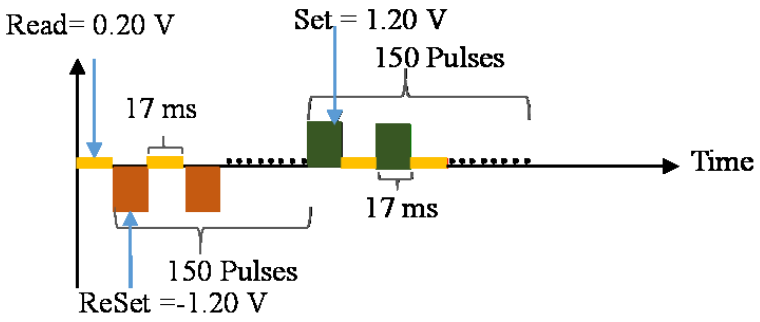
During simulation (both for HRS and LRS), fitting parameters were evaluated using a 95% confidence interval and regression analysis. Table I summarizes values of all the fitting parameters as per the proposed charge transport mechanisms explained in this report. Average error margin for the fitted parameters was in the range of (~$3.42e^{-4}$).

Table I

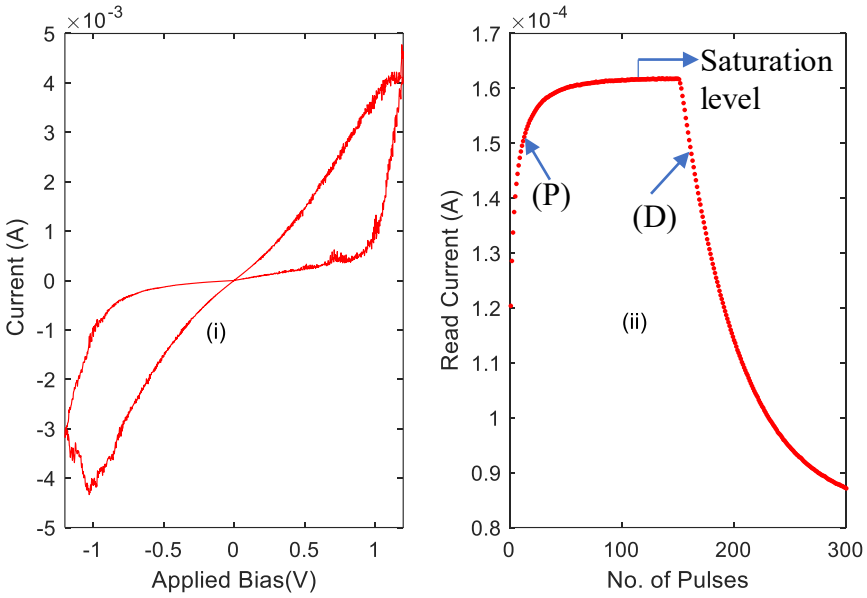
Symbol	Fitting Parameter	Fitted Value	Unit
m_{eff}	Electron Effective Mass	0.05 m_o $m_o = 9.1x10^{-31}$	kg
μ	Electron Mobility	25	$cm^2\ V^{-1}s^{-1}$
N′	Trap Density	$\sim 10^{19}$	cm^{-3}
E_t	Deep Trap	E_c -1.145	eV
d′	Trap distance	6.2581	nm

Biological brain shows continuous change of synaptic weights between maximum and minimum conductance/resistance states. This is a very important criterion for designing neuromorphic architecture. HRS current is suggested to be responsible for intermediate resistive/conductive states in the nonvolatile memory device. At high resistance state, existence of unfilled defect energy levels at a certain distance below the oxide conduction band were found responsible for quantum mechanical tunneling of electrons through the electrode-oxide interface. Application of same, repetitive pulses along high sub-threshold region produces multiple, distinct conductive states much less than the device on state current. These intermediate states promote gradual change of conductivity. As explained, the deep trap energy level is not exactly at the interface rather at a distance from the cathode terminal. Multiple repetitive read bias would bring the deep trap energy level within the switching layer, closer to the bottom electrode. In other words, consecutive read bias in between each write bias reduces the distance

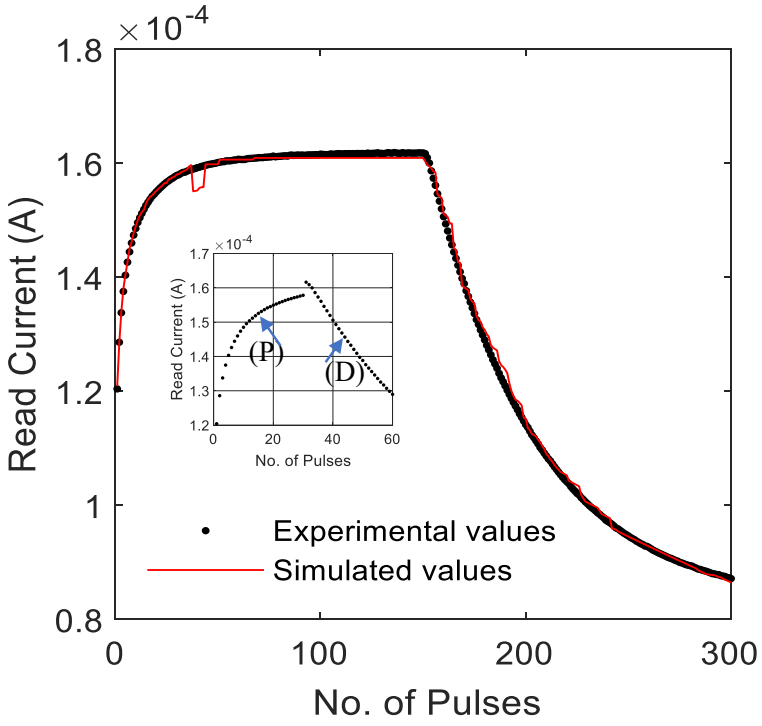
between the deep trap energy level and the cathode terminal which enhances the tunneling probability of electron eventually with gradual change of memristor conductivity for memristor high resistance state. Experimental results demonstrate feasibility of the lithium niobate based memristor as a neuromorphic device. The programming protocol mentioned in [32] has been followed in this work to investigate the proposed memristor's controllability. A series of positive voltage pulses (1.2 V, 17 ms) or negative voltage pulses (-1.2 V, 17ms) with uniform time interval were applied to the memristor. Device conductance was measured in the high resistance region, using a read voltage pulse (0.2 V, 17 ms) immediately after each programming pulse. Experimental condition applied for studying multiple intermediate resistive states along memristor HRS region has been depicted in figure 8.a. Precise analog control was achieved in the lithium niobate based memristor device as shown in figure 8.b.ii. Each dotted point (in red) shows individual conductive state with the application of repetitive read bias. Appearance of such intermediate states (in between memristor off and on states) are desired to ensure analog conductivity modulation required for neuro morphic device. This work reports continuous increase and decrease of memristor read current (same as potentiation (P) and depression (D) phenomena in human brain). After 60 consecutive negative voltage pulses (-1.2 V, 17ms) with uniform time interval, memristor off state (HRS) conductivity reaches a saturation level and application of 90 more similar bias sustains the saturation level. This implies existence of sixty independent conductive states required for the potentiation phenomena. Lithium niobate based memristor device shows faster depression compared to the potentiation phenomena as depicted in the inset of figure 8.c. This would signify the probability of tunneling of electrons from the oxide filled traps is slower than that of the unfilled ones. Each black dotted point in the inset of fig.8.c. indicates individual intermediate states obtained in between memristor HRS and LRS region. Hence results presented in fig.8 are analogous to the potentiation(P) and depression (D) phenomena observed in the synapses in brain tissue [33].



(a)



(b)



(c)

Figure 8. Experimental condition applied for studying analog programmability from lithium niobate based memristor device (area 7.50 μm^2)(b) evidence of analog switching along high resistive state evaluated at read voltage: 0.20 V (c) Gradual increase (Potentiation) and decrease (depression) of device current simulated with the variation of trap distance d$^{'}$ from 7.78 to 4.45 nm using ETAT mechanism at room temperature. Inset individually shows experimental read current values (using dotted points) indicating different intermediate conductive states from the memristor device.

Existence of multilevel resistive switching was investigated for the lithium niobate based memristor. Pulse stimulations resulted in gradually modulated HRS currents. Conductivity

modulation from the lithium niobate based memristor device for the HRS has been simulated using the ETAT mechanism. This has been achieved by changing the distance d' for the nearest (defect) trap energy level from the cathode terminal while all other device parameters (trap density, electron effective mass and deep trap energy level) remain the same. In this regard, value of d' was varied from 7.78 to 4.45 nm. Multiple distinct resistance levels for memristor HRS conductivity have been simulated by varying the trap distance (d') only. Existence of multiple states in the memristor HRS ensures low power required for information storage and processing. Energy consumption per synaptic activity was evaluated as ~$1.69e^{-6}$ J, as the external stimuli required for HRS analog modulation was ~ 0.20 V and HRS current was in the micro-ampere range.

Synaptic conductivity modulation within human brain is basically a stochastic process. Analysis of dynamic resistive switching phenomena requires consideration of the impact of different noise upon the states of memristor and its electrical properties. Authors in [34] reported an experimental analysis of improved resistive switching in presence of white Gaussian noise signal[35],[36]. A stochastic model using both analytical and numerical validation were demonstrated in [37] to study the influence of fluctuations for memristor switching dynamics. Work presented in [38] explains a method for determining activation energy of oxygen ion utilizing the flicker noise spectra. Our future work would focus on developing a robust, stochastic model with the consideration of different noise signals which would investigate time dependent changes of the filament profile including area and filament shape within the proposed memristor device.

5. Conclusions

This work characterizes a lithium niobate based memristor as a suitable candidate for a neuromorphic device. The prevalent charge transport mechanism for such devices has been investigated using a simple steady state approach. In this report, the dc characterization for memristor device is segmented into high and low resistance regions. The elastic trap assisted tunneling (ETAT) mechanism was found to be dominant for memristor HRS conductivity. Existence of intermediate resistance levels for HRS conduction is also verified using the ETAT mechanism. The memristor LRS follows ohmic conduction even for high bias for room temperature measurements. Simulated I-V curves show reasonable agreement with the experimental data.

References

[1] Chua, L. (1971). Memristor-the missing circuit element. *IEEE Transactions on circuit theory*, *18*(5), 507-519; DOI: 10.1109/TCT.1971.1083337.

[2] Strukov, D. B., Snider, G. S., Stewart, D. R., & Williams, R. S. (2008). The missing memristor found. *nature*, *453*(7191), 80-83; https://doi.org/10.1038/nature06932.

[3] Hickmott, T. W. (1962). Low-frequency negative resistance in thin anodic oxide films. *Journal of Applied Physics*, *33*(9), 2669-2682; DOI: 10.1063/1.1702530.

[4] Burr, G. W., Kurdi, B. N., Scott, J. C., Lam, C. H., Gopalakrishnan, K., & Shenoy, R. S. (2008). Overview of candidate device technologies for storage-class memory. *IBM Journal of Research and Development*, *52*(4.5), 449-464; DOI: 10.1147/rd.524.0449.

[5] Zhirnov, V. V., Cavin, R. K., Menzel, S., Linn, E., Schmelzer, S., Bräuhaus, D., Schindler, C. & Waser, R. (2010). Memory devices: Energy–space–time tradeoffs. *Proceedings of the IEEE*, *98*(12), 2185-2200; DOI: 10.1109/JPROC.2010.2064271.

[6] Mikhaylov, A. N., Gryaznov, E. G., Belov, A. I., Korolev, D. S., Sharapov, A. N., Guseinov, Telelbaum, D. V., Tikhov, S.V., Malekhonova, N.V., Bobrov, A.I., Pavlov, D. A., Gerasimova, S.A., Kazantsev, V.B., Agudov, N.V., Dubkov, A.A., Rosario, C.M.M., Sobolev, N.A. & Spagnolo, B. (2016). Field-and irradiation-induced phenomena in memristive nanomaterials. *physica status solidi (c)*, *13*(10-12), 870-881; https://doi.org/10.1002/pssc.201600083.

[7] Li, C., Hu, M., Li, Y., Jiang, H., Ge, N., Montgomery, E., Lin, P., Wang, Z., Song, W., Strachan, J. P. , Barnell, M., Wu, Q., Williams, R.S., Yang, J.J. & Xia, Q. (2018). Analogue signal and image processing with large memristor crossbars. *Nature Electronics*, *1*(1), 52; https://doi.org/10.1038/s41928-017-0002-z.

[8] Cai, F., Correll, J. M., Lee, S. H., Lim, Y., Bothra, V., Zhang, Z., Flynn, M.P., & Lu, W. D. (2019). A fully integrated reprogrammable memristor–CMOS system for efficient multiply–accumulate operations. *Nature Electronics*, *2*(7), 290-299; https://doi.org/10.1038/s41928-019-0270-x.

[9] Robertson, J. (2005). High dielectric constant gate oxides for metal oxide Si transistors. *Reports on progress in Physics*, *69*(2), 327; https://doi.org/10.1051/epjap:2004206.

[10] Mohammad, B., Abi Jaoude, M., Kumar, V., Al Homouz, D. M., Nahla, H. A., Al-Qutayri, M., & Christoforou, N. (2016). State of the art of metal oxide memristor devices. *Nanotechnology Reviews*, *5*(3), 311-329; https://doi.org/10.1515/ntrev-2015-0029.

[11] Kim, S., Choi, S., & Lu, W. (2014). Comprehensive physical model of dynamic resistive switching in an oxide memristor. *ACS nano*, *8*(3), 2369-2376; https://doi.org/10.1021/nn405827t.

[12] Ielmini, D. (2016). Resistive switching memories based on metal oxides: mechanisms, reliability and scaling. *Semiconductor Science and Technology*, *31*(6), 063002; https://doi.org/10.1021/nn405827t.

[13] Wang, Z., Wu, H., Burr, G. W., Hwang, C. S., Wang, K. L., Xia, Q., & Yang, J. J. (2020). Resistive switching materials for information processing. *Nature Reviews Materials*, 1-23; https://doi.org/10.1038/s41578-019-0159-3.

[14] Yu, S., Guan, X., & Wong, H. S. P. (2011). Conduction mechanism of TiN/HfO_x/Pt resistive switching memory: A trap-assisted-tunneling model. *Applied Physics Letters*, *99*(6), 063507; https://doi.org/10.1063/1.3624472.

[15] Schmidt, W. G., Albrecht, M., Wippermann, S., Blankenburg, S., Rauls, E., Fuchs, F., Rodi, C., & Hermann, A. (2008). $LiNbO_3$ ground-and excited-state properties from first-principles calculations. *Physical Review B*, *77*(3), 035106; https://doi.org/10.1103/PhysRevB.77.035106.

[16] Li, Y., Wang, Z., Midya, R., Xia, Q., & Yang, J. J. (2018). Review of memristor devices in neuromorphic computing: materials sciences and device challenges. *Journal of Physics D: Applied Physics*, *51*(50), 503002; https://doi.org/10.1088/1361-6463/aade3f.

[17] Zaman, A., Yakopcic, C., Wang, S., Shin, E., Wang, W., Taha, T. M., & Subramanyam, G. (2019, July). Analysis of Lithium Niobate Memristor Devices for Neuromorphic Programmability. In *2019 IEEE National Aerospace and Electronics Conference (NAECON)* (pp. 41-45). IEEE; DOI: 10.1109/NAECON46414.2019.9058020.

[18] Ievlev, V., Sumets, M., & Kostyuchenko, A. (2013). Conduction mechanisms in Si-$LiNbO_3$ heterostructures grown by ion-beam sputtering method. *Journal of Materials Science*, *48*(4), 1562-1570; https://doi.org/10.1007/s10853-012-6912-2.

[19] Hansen, M., Ziegler, M., Kolberg, L., Soni, R., Dirkmann, S., Mussenbrock, T., & Kohlstedt, H. (2015). A double barrier memristive device. *Scientific reports*, *5*, 13753;

https://doi.org/10.1038/srep13753.
[20] Clerc, R., Spinelli, A., Ghibaudo, G., & Pananakakis, G. (2002). Theory of direct tunneling current in metal–oxide–semiconductor structures. *Journal of applied physics*, *91*(3), 1400-1409; https://doi.org/10.1063/1.1427398.
[21] Ravindra, N. M., & Zhao, J. (1992). Fowler-Nordheim tunneling in thin SiO2 films. *Smart Materials and Structures*, *1*(3), 197; https://doi.org/10.1088/0964-1726/1/3/002.
[22] Wang, M. T., Deng, S. Y., Wang, T. H., Cheng, B. Y. Y., & Lee, J. Y. M. (2005). The ohmic conduction mechanism in high-dielectric-constant ZrO_2 thin films. *Journal of The Electrochemical Society*, *152*(7), G542; https://doi.org/10.1149/1.1931308.
[23] Cheng, X. R., Cheng, Y. C., & Liu, B. Y. (1988). Nitridation-enhanced conductivity behavior and current transport mechanism in thin thermally nitrided SiO_2. *journal of applied physics*, *63*(3), 797-802; https://doi.org/10.1063/1.340072.
[24] Iyevlev, V., Kostyuchenko, A., & Sumets, M. (2011, January). Fabrication, substructure and properties of $LiNbO_3$ films. In *16th International School on Quantum Electronics: Laser Physics and Applications* (Vol. 7747, p. 77471J). International Society for Optics and Photonics; https://doi.org/10.1117/12.879075.
[25] Zaman, A., Shin, E., Yakopcic, C., Taha, T. M., & Subramanyam, G. (2018, July). Experimental Study of Memristors for use in Neuromorphic Computing. In *NAECON 2018-IEEE National Aerospace and Electronics Conference* (pp. 370-374). IEEE; DOI: 10.1109/NAECON.2018.8556749.
[26] Wood, J. W., & Redin, R. D. (1993). A simple profilometer for film thickness measurement. *Review of scientific instruments*, *64*(8), 2405-2406; https://doi.org/10.1063/1.1143897.
[27] Greenlee, J. D., Shank, J. C., Tellekamp, M. B., Gunning, B. P., Fabien, C. A., & Doolittle, W. A. (2014). Liquid phase electro-epitaxy of memristive $LiNbO_2$ crystals. *Crystal growth & design*, *14*(5), 2218-2222; https://doi.org/10.1021/cg401775p.
[28] Li, H., Xia, Y., Xu, B., Guo, H., Yin, J., & Liu, Z. (2010). Memristive behaviors of $LiNbO_3$ ferroelectric diodes. *Applied Physics Letters*, *97*(1), 012902; https://doi.org/10.1063/1.3462067.
[29] Sumets, M. (2018). *Lithium Niobate-Based Heterostructures*. IOP Publishing; https://doi.org/10.1088/978-0-7503-1729-0
[30] Eliseev, E. A., Morozovska, A. N., Svechnikov, G. S., Gopalan, V., & Shur, V. Y. (2011). Static conductivity of charged domain walls in uniaxial ferroelectric semiconductors. *Physical Review B*, *83*(23), 235313; https://doi.org/10.1103/PhysRevB.83.235313.
[31] Ohmori, Y., Yamaguchi, M., Yoshino, K., & Inuishi, Y. (1976). Electron Hall mobility in reduced $LiNbO_3$. *Japanese Journal of Applied Physics*, *15*(11), 2263; https://doi.org/10.1143/JJAP.15.2263.
[32] Kim, S., Kim, H., Hwang, S., Kim, M. H., Chang, Y. F., & Park, B. G. (2017). Analog synaptic behavior of a silicon nitride memristor. *ACS applied materials & interfaces*, *9*(46), 40420-40427; https://doi.org/10.1021/acsami.7b11191.
[33] Kuzum, D., Jeyasingh, R. G. D., Yu, S., & Wong, H. S. P. (2012). Low-energy robust neuromorphic computation using synaptic devices. *IEEE Transactions on Electron Devices*, *59*(12), 3489-3494; DOI: 10.1109/TED.2012.2217146.
[34] Filatov, D. O., Vrzheshch, D. V., Tabakov, O. V., Novikov, A. S., Belov, A. I., Antonov, I. N., Sharkov, V.V., Koryazhkina, M.N., Mikhaylov, A.N., Gorshkov, O.N., Dubkov, A. A., Carollo, A. & Spagnolo, B. (2019). Noise-induced resistive switching in a memristor based on ZrO_2 (Y)/Ta_2O_5 stack. *Journal of Statistical Mechanics: Theory and Experiment*, *2019*(12), 124026; https://doi.org/10.1088/1742-5468/ab5704.

[35] Spagnolo, B., Guarcello, C., Magazzù, L., Carollo, A., Persano Adorno, D., & Valenti, D. (2017). Nonlinear relaxation phenomena in metastable condensed matter systems. *Entropy*, *19*(1), 20; https://doi.org/10.3390/e19010020.

[36] Spagnolo, B., Valenti, D., Guarcello, C., Carollo, A., Adorno, D. P., Spezia, S., Pizzolato, N., & Paola, Di B. (2015). Noise-induced effects in nonlinear relaxation of condensed matter systems. *Chaos, Solitons & Fractals*, *81*, 412-424; https://doi.org/10.1016/j.chaos.2015.07.023

[37] Agudov, N. V., Safonov, A. V., Krichigin, A. V., Kharcheva, A. A., Dubkov, A. A., Valenti, D., Mikhailov, A.N., Carollo, A., & Spagnolo, B. (2020). Nonstationary distributions and relaxation times in a stochastic model of memristor. *Journal of Statistical Mechanics: Theory and Experiment*, *2020*(2), 024003; https://doi.org/10.1088/1742-5468/ab684a.

[38] Yakimov, A. V., Filatov, D. O., Gorshkov, O. N., Antonov, D. A., Liskin, D. A., Antonov, I. N., Belyakov, A.V., Klyuev, A.V., Carollo, A. & Spagnolo, B. (2019). Measurement of the activation energies of oxygen ion diffusion in yttria stabilized zirconia by flicker noise spectroscopy. *Applied Physics Letters*, *114*(25), 253506; https://doi.org/10.1063/1.5098066.