RFIC Inductorless, Widely-Tunable N-Path Shekel Circulators Based on Harmonic Engineering

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***Abstract*— Recently demonstrated non-magnetic circulators rely on the interference between an LPTV non-reciprocal gyrator and reciprocal transmission-line circuits, which limits their form factor and compromises the tunability of N-path circuits. In this paper, a new class of non-magnetic inductorless widely-tunable non-reciprocal circulators based on harmonic engineering is introduced. LPTV circuits rely on modulating the input signals with a square-wave clock waveform that can contain multiple harmonics. The harmonic engineering concept controls the response to various harmonics of the clock signal, the superposition of which results in the desired functionality. Two prototype N-path Shekel circulators have been implemented in 65nm CMOS. The first prototype, operating in the large-RC-regime can be reconfigured for operation across 0.1-1.1 GHz, with losses ranging from 2.4-3.4 dB. It has a form factor of $\frac{\lambda^2}{2{,}000{,}000}$ at 500 MHz, with a power consumption of 9.6 mW. The second prototype operates in the low-RC-regime with a tuning range of 0.28-1.15 GHz and a loss of 2.3-3.3 dB, and achieves more than 20 dB isolation across a 233 MHz BW (38%) within a $\frac{\lambda^2}{1{,}500{,}000}$ form factor at 600 MHz.**

I. Introduction

In 1948, Tellegen hypothesized a non-reciprocal component called a "gyrator" as the fifth elemental circuit building block, as shown in Fig. 1(a) [1]. The gyrator enables the synthesis of arbitrary non-reciprocal networks, including circulators. The simplest circulator topology was proposed by Shekel in [2], and only consists of one gyrator, in which the reference nodes of the two ports of the gyrator are connected together to form a separate third port (Fig. 1(b)).

While circulators have been traditionally implemented using ferrite materials, recently non-magnetic CMOS-integrated circulators based on linear periodically-time-varying (LPTV) circuits have been demonstrated [3]–[6]. Relying on gyrators based on switched-capacitor N-path filters [3], [4] or switched transmission lines [5], a fundamental limitation of all these implementations is the usage of quarter-wave transmission lines or hybrids around the N-path filter or the switched t-line gyrator, which limit the tuning range. Furthermore, these quarter-wave components require the integration of large inductors which limit the chip area. Similarly, prior angular momentum biasing schemes [6] have relied on off-chip inductors to allow CMOS integration, since large values of high-quality-factor inductance are needed. Additionally, such approaches are not tunable in frequency due to the interaction of multiple LC tanks at their resonance.

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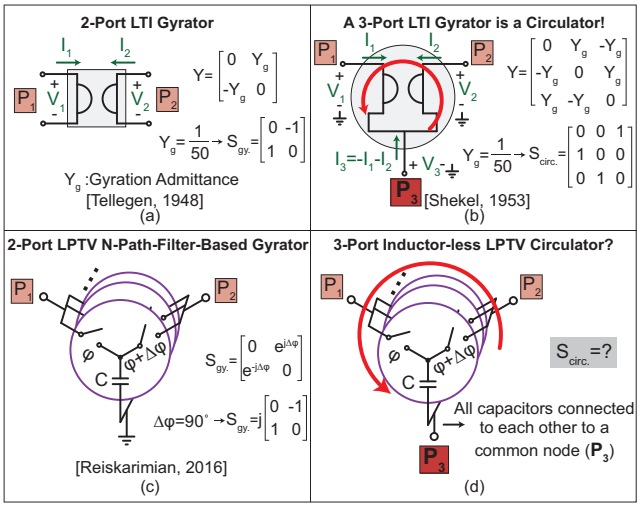

Fig. 1. The evolution of the 3-port inductorless LPTV circulator. (a) The original Tellegen's LTI gyrator and (b) Shekel's circulator employing a 3-port gyrator. (c) A 2-port LPTV N-path-filter-based gyrator and (d) its potential transformation to a 3-port inductorless circulator.

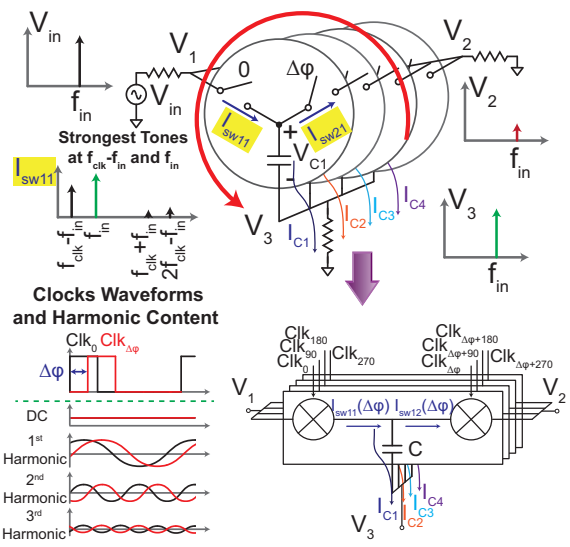

Fig. 2. Harmonic engineering in the two-port LPTV N-path gyrator to realize an LPTV Shekel circulator.

Recently, we have demonstrated an inductorless N-path nonreciprocal isolator in [7]. Here, we realize Shekel's vision in silicon for the first time to demonstrate two N-path circulator prototypes that (i) can be reconfigured across a wide bandwidth by changing the clock frequency, thus preserving the tunability of N-path structures, (ii) completely eliminate the need for

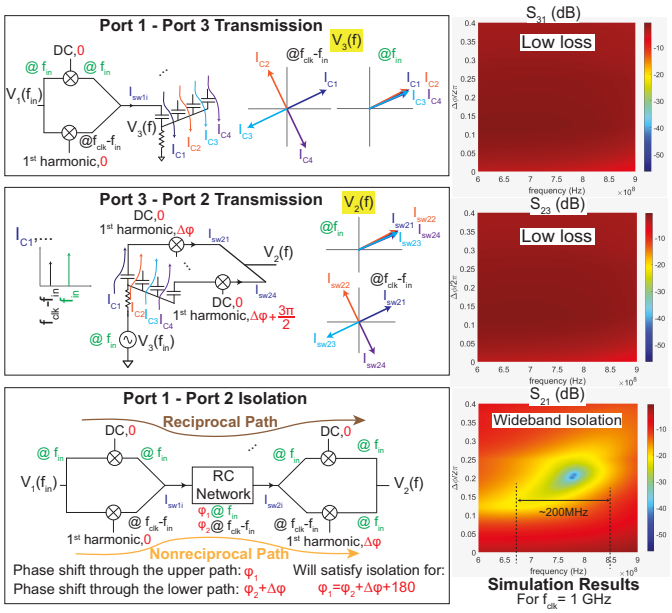

Fig. 3. Simulation results of the LPTV Shekel circulator as a function of f_{in} and $\Delta\phi$ for C=1.8 pF and f_{clk}=1 GHz using an 8-path N-path gyrator.

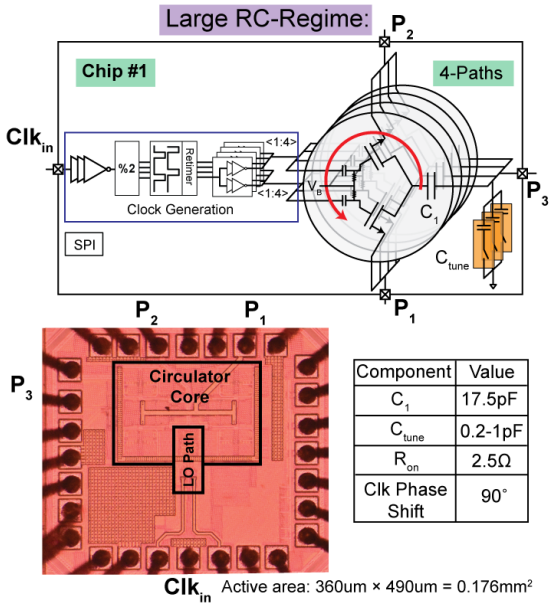

Fig. 4. Block and circuit diagram, chip photo and component values of the proposed large-RC-regime widely-tunable inductorless N-path Shekel circulator.

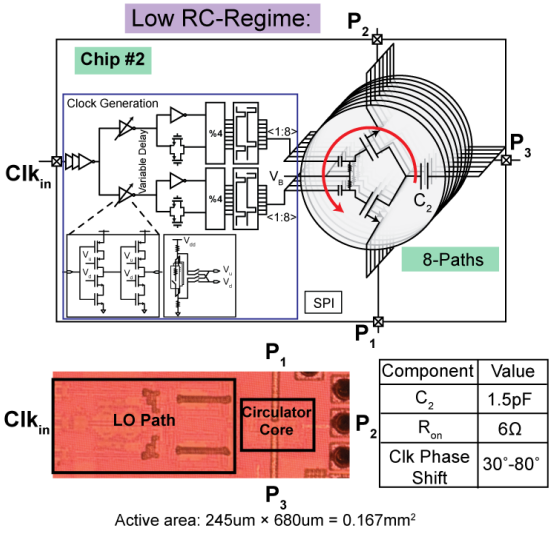

Fig. 5. Block and circuit diagram, chip photo and component values of the proposed low-RC-regime widely-tunable inductorless N-path Shekel circulator.

inductors and hence miniaturize the circulator to very small dimensions, and (iii) reduce the clock complexity compared to prior architectures, lowering the power consumption. Since Shekel's architecture considered LTI gyrators, we have developed harmonic engineering techniques that enable Shekel's architecture to be applied to the LPTV N-path gyrator (Fig. 1(d)).

II. Inductorless Nonreciprocity Through Harmonic Engineering

Due to its LPTV nature, the introduction of a third port at the reference terminals of the N-path-based gyrator does not seamlessly translate the circuit response to that of a circulator. This can be intuitively understood as follows: in the original N-path-based gyrator, no two capacitors interact with each other in any manner. When the third port resistor is introduced, at any instant, two capacitors are simultaneously connected to the resistor at any time (assuming that there is a non-zero phase-shift between the clocks to enable non-reciprocity), allowing a charge-sharing between the paths.

The circuit can be further understood by considering the currents flowing through various branches in the frequency domain (Fig. 2). Modeling the switches by a time-varying conductance ($G_{sw} = \infty$ in the ON-period and $G_{sw} = 0$ in the OFF-period), the input voltage at port 1 creates a current in each switch (I_{sw1i}) with frequency content created by various harmonics of the clock: f_{in}, $f_{clk} \pm f_{in}$, $2f_{clk} \pm f_{in}$, etc. Part of this frequency-converted current passes through the second switch, re-mixing back with the phase-shifted clock, while the rest passes through the capacitors. Finally, currents through the capacitors of the various paths sum up at the third port and create a voltage. Note that, similar to conventional N-path structures, this voltage can only have harmonics at around $kNf_{clk} \pm f_{in}$ due to summation and cancellation across a polyphase structure. The transfer functions from port 1 to ports 2 and 3 are dependent on the phase shift between the switches ($\Delta\phi$), the difference between f_{in} and f_{clk}, and the RC time constant.

Based on this picture, we introduce a harmonic engineering technique that enables the design of Shekel LPTV circulators. The original LPTV N-path gyrator relies only on the mixing of the input frequency with the fundamental harmonic of the clock signal to create the near-DC frequency content that is stored on the large baseband capacitors, which in turn mixes with the phase-shifted clocks on the output side to impart a non-reciprocal phase response to the output. Here, in our proposed circulator, we take advantage of mixing not only with the fundamental harmonic, but also with other content:

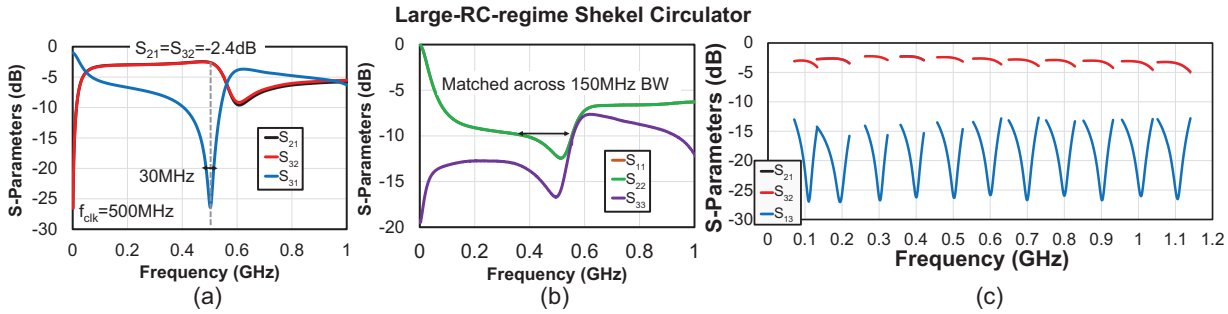

Fig. 6. Measured large-RC-regime circulator S-parameters demonstrating low-loss, wide-bandwidth and high tuning range.

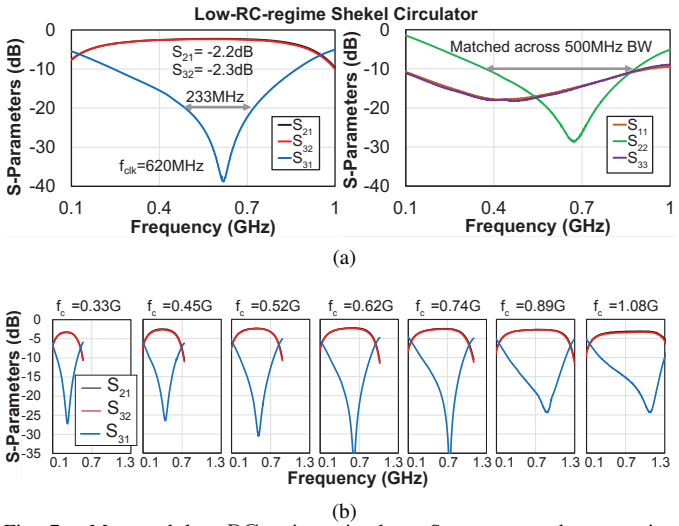

Fig. 7. Measured low-RC-regime circulator S-parameters demonstrating low-loss, wide-bandwidth and high tuning range.

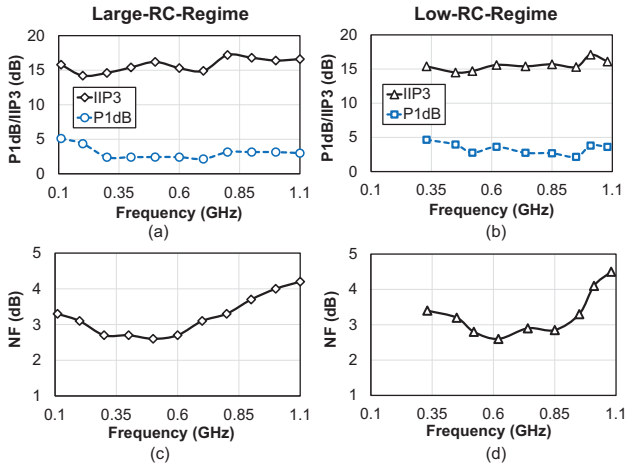

Fig. 8. Measured noise and linearity performance across the tuning range.

specifically, the DC component of the clocks.

Fig. 3 shows an intuitive explanation of the operation of our LPTV Shekel circulator. As mentioned earlier, part of the switch currents (I_{sw1i}) pass through the capacitors to sum up at port 3, at which time the components at f_{in} coming from the DC component of the clocks add constructively, while the components at $f_{clk} - f_{in}$ cancel. The voltage created at port 3 can be maximized by proper choice of $\Delta\phi$, $\frac{f_{in}}{f_{clk}}$, and the RC time constant. On the other hand, from port 1 to port 2, two parallel signal flows exist - a reciprocal flow through mixing with the DC components of the clocks (since DC components contain no phase shift), and another non-reciprocal flow through the act of down-conversion and up-conversion. Based on the value of $\Delta\phi$, $\frac{f_{in}}{f_{clk}}$ and the RC time constant, these two contributions can add destructively to create isolation from port 1 to port 2. The same argument can be extended to an excitation at any of the other two ports. Therefore, this structure can indeed act as a circulator if properly designed.

Fig. 3 shows the insertion loss and isolation as a function of f_{in} and $\Delta\phi$ for C=1.8 pF, f_{clk}=1 GHz and 8 paths. It can be seen that low loss (1.3 dB) and wide isolation BW (26%) can be achieved at f_{in}=0.775 GHz for $\Delta\phi = \frac{2\pi}{5}$. Note that simultaneous optimization of loss and isolation happens at an offset frequency from the clock frequency. This offset frequency becomes smaller for larger capacitor values. This offset frequency offers the advantage of mitigating LO leakage, and can be incorporated within the existing transceiver signal generation through careful frequency planning.

III. Implementation and Measurement Results

Two inductorless widely-tunable LPTV Shekel circulators are designed in a 65 nm CMOS technology (Fig. 4 and Fig. 5). One operates in the large-RC-regime with C=17.5 pF, 4 paths and $\Delta\phi = 90°$ (non-overlapping clocks), simplifying clock generation. Fixing the capacitance value and clock phase-shift removes them as degrees of freedom to simultaneously optimize loss and isolation. However, since any circulator is limited in its isolation by the matching at the 3^{rd} port, a 3-bit (0.2-1 pF) capacitor (C_{tune}) bank at the third port has been implemented which improves the port matching while maintaining the isolation across the tuning range. The second circulator operates in the low-RC-regime with C=1.5 pF, 8 paths and a variable $\Delta\phi$ (∼30-80°) across the tuning range, achieved through an LO path phase shifter. While the switch resistance can be used as a degree of freedom for harmonic engineering purposes, we solely choose the switch resistance values in both implementations to optimize the losses.

Measurement results (Figs. 6, 7 and 8) reveal that the large-RC circulator operates across a decade of frequency from 110 MHz to 1.1 GHz, with a loss range of 2.4 to 3.4 dB at the center frequency. The ratio between the operation frequency and clock frequency is around 0.75-0.95 across the

Table 1. Comparison with state-of-the-art integrated non-magnetic circulators.

		JSSC 2017 [3]	JSSC 2019 [5]	ISSCC 2018 [4]	TMTT 2019 [6]	JSSC 2019 [7]	This work [Chip #1]	This work [Chip #2]
Technology and Frequency	Architecture	N-path-based-gyrator in a ¾λ t-line ring	t-line-based gyrator in a ¾λ t-line ring	Hybrid-coupler-based N-path circulator	Angular momentum biasing using LC resonators	N-path-based-gyrator using wirebond inductance	Low-RC-regime Shekel circulator	Large-RC-regime Shekel circulator
	Technology	65nm CMOS	180nm SOI CMOS	65nm CMOS	180nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
	Frequency Range	0.61-0.975GHz	0.86-1.08GHz	0.55-0.9GHz	0.91G	2.2GHz	0.28-1.15GHz	0.11-1.1GHz
	Tuning BW ($\frac{f_{max}}{f_{min}}$)	1.6	1.26	1.64	1	1	4.1	10
Form Factor and Integration	Total Capacitance	152pF	~19pF	N/R	12.3pF	74.6pF	12pF	70pF
	Number of Inductors	3 (off-chip)	13 + 3 off-chip baluns	1 (off-chip balun)	6 (off-chip)	6 (wirebond) + 2 off-chip baluns	0	0
	Total Inductance	26.7nH	99nH	N/R	180nH	30nH	0nH	0nH
	Fully Integrated?	No	No	No	No	No	Yes	Yes
	Form factor	λ²/5,100 36mm²	λ²/6,000 16.5mm²	~λ²/2000 or 82mm²	λ²/3,000 36mm²	~λ²/130 or 144mm² (including the RX)	λ²/1,500,000 @600MHz 0.167mm²	λ²/2,000,000 @500MHz 0.176mm²
Performance Metrics	Transmission (P1-P3, P3-P2)	-1.8dB/ N/A	-2.1/-2.9dB	-2.6 to -4.7dB/ N/R	-4.8/-4.8dB [4]	-3.7dB/ N/A	-2.2/-2.3 to -3.2/-3.3dB Across the tuning range	-2.4/-2.4 to -3.4/-3.4dB Across the tuning range
	Isolation BW (>20dB)	7.1%	23%	22% (30dB BW) 4.4% (40dB BW) [3]	2.4% (20dB BW)	~1% (30dB BW)	38% (20dB BW) 11.6% (30dB BW) @600MHz	6% @500MHz
	P3-P2 NF	6.3dB [1]	3.1dB	2.7dB [1]	5.2dB	9.5dB [1]	2.6-4.5dB	2.6-4.2dB
	P1-P3 IIP3	+32.3dBm [2]	+50dBm [2]	+25dBm [2]	+6.1dBm	+45.5dBm [2]	+13.2 to +16.8dBm	+12.5 to +15.9dBm
	P1-P3 P1dB	N/R	>+30.7dBm [2]	+5.5dBm [2]	N/R	+14dBm	+1 to +3.2dBm	+0.8 to +3.4dBm
	P3-P2 IIP3	N/R	+36.9dBm	N/R	+6dBm	+21dBm	+14.5 to +17.1dBm	+14.2 to +17.2dBm
	P3-P2 P1dB	N/R	+21dBm	N/R	N/R	-6dBm [6]	+2.1 to +4.6dBm	+2.2 to +5.1dBm
	Power Consumption	36mW	170mW	24mW	64mW [5]	26.25mW	36mW @ 600MHz operation freq.	9.6mW @ 500MHz operation freq.

1. NF of the receiver. 2. Enhanced due to the relative positioning of the gyrator inside the t-line ring. 3. Achieves a large BW by using an off-chip hybrid. 4.With external impedance tuners.
5. Not including power consumed in generating the clocks. 6. ANT-BB P1dB, limited by the receiver chain.

tuning bandwidth. The isolation is better than 25 dB across the band with a 20 dB isolation BW of 30 MHz (6%) at 500 MHz operation frequency. The circulator dissipates only 9.6 mW power, and exhibits an active area of 0.176 mm^2. The measured noise figure varies from 2.6 to 4.2 dB. In-band P1dB and IIP3 are measured to be +0.8 to +3.4 dBm/+2.2 to +5.1 dBm and +12.5 to +15.9 dBm/+14.2 to +17.2 dBm in the two transmission directions, respectively.

The low-RC-regime circulator operates across 280 MHz to 1.15 GHz with 2.2 to 3.2 dB loss. The operation to clock frequency ratio ranges from 0.6-0.8. The isolation is as high as 40 dB, with a 20 dB isolation BW of more than 230 MHz at 620 MHz operation frequency (38%). The chip consumes 36 mW of power. The active area of the chip is 0.163 mm^2. Measurements reveal 2.6 to 4.5 dB of NF across the band. The P1dB ranges from +1 to +3.2 dB and +2.1 to +4.6 dBm in the two transmission directions, while IIP3 ranges from +13.2 to +16.8 dBm, and +14.5 to +17.1 dBm.

IV. Conclusion

When compared with prior CMOS-integrated non-magnetic RF circulators (Table 1), this work achieves significantly smaller footprint (150× smaller than prior works [3], [6], [8]), higher tuning range, and higher instantaneous BW, while maintaining loss and NF. Compared to a broader range of non-reciprocal devices implemented in various platforms (Fig. 9), our work significantly improves the tuning bandwidth at a much smaller form factor. The power handling is consistent with N-path filters that feature switches in the signal path, and can be enhanced using clock bootstrapping [8] (preliminary simulation results demonstrate around 8-10 dB improvement in P1dB for our proposed architectures in 65 nm technology with 2.7-3.5× power consumption), stacked SOI CMOS switches [5] and/or GaAs/GaN technologies.

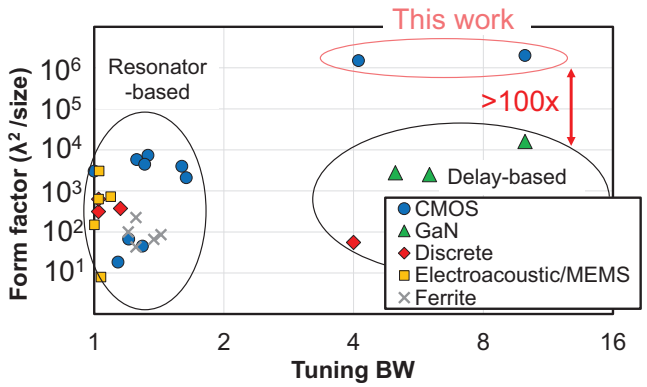

Fig. 9. A comparison of state-of-the-art circulators based on their form factor and tuning BW (defined as $\frac{f_{max}}{f_{min}}$).

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