Ultra Compact, Ultra Wideband, DC-1GHz CMOS Circulator Based on Quasi-Electrostatic Wave Propagation in Commutated Switched Capacitor Networks

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***Abstract*— Recent research has revealed the possibility to achieve non-magnetic non-reciprocity using time-variance. However, prior CMOS-based circulators rely on the interference between non-reciprocal switched-capacitor/transmission-line gyrators and reciprocal transmission-line rings, which increases form factor and restricts frequency tunability and bandwidth. On the other hand, recent works on quasi-electrostatic wave propagation in switched-capacitor media have demonstrated a new regime in multipath switched-capacitor network operation that enables an ultra-broadband, ultra-compact reciprocal/non-reciprocal true-time-delay element. In this work, we apply synthetic rotation across this quasi-electrostatic medium to realize an ultra-broadband N-port circulator with ultra-compact form-factor. This new architecture is showcased in a wideband 3-port circulator implemented in a standard 65nm CMOS process. This circulator exhibits symmetric performance across all 3 ports and DC-1GHz operation for a modulation frequency of 500MHz. The measured transmission losses range between 3.1-4.3dB, matching is <-15dB, isolation is >18dB and NF is consistent with the insertion loss. This device occupies an area of 0.19mm^2 (λ^2_{center}/1.9×10^6), representing about 100-1000× higher miniaturization compared to the prior art.**

***Keywords*— circulators, delay lines, full-duplex, switched-capacitor, LPTV, ultra-wideband (UWB).**

I. Introduction

Devices with non-reciprocal transmission (gyrators, isolators and circulators) are often required in wireless communications and radar/imaging sensors. There has been a recent surge in research to realize integrated CMOS non-reciprocal components that do not rely on magnetic (ferrite) materials [1]-[6]. Techniques that have been explored include varactor modulation in resonant rings [1], switched-capacitor N-path filter approaches [2], [3] and switched-transmission-line approaches [4], [5]. While these efforts have been successful in enhancing linearity and power handling [5], their bandwidths and frequency tunability have been limited to a fraction of the center frequency and their footprints have been large due to the use of LC resonators or wavelength-scale transmission lines.

In [7], a new regime of operation for switched-capacitor networks was proposed that enables the realization of integrated quasi-electrostatic passive true-time-delay lines with (i) low loss, nanosecond-scale delay over GHz-range bandwidths, (ii) ultra-compact footprint, and (iii)

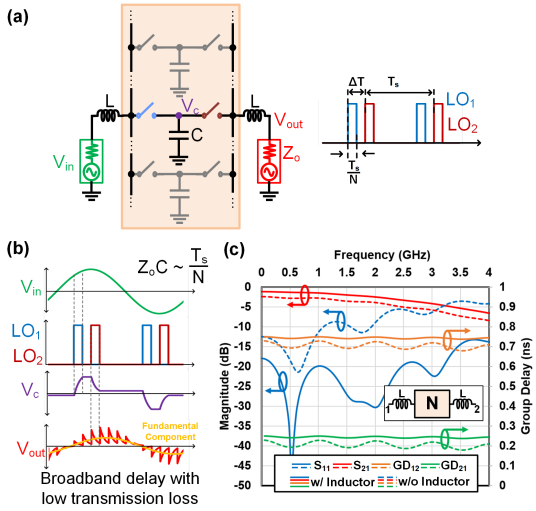

Fig. 1. (a) Circuit diagram of a commutated multipath network realized using N identical branches of a switch-capacitance-switch structure. (b) Evolution of the charge on the capacitor during the charging and discharging phases when $T_s/N \approx Z_0C$. (c) S-parameters of the network with and without the matching inductors when N = 8, f_s=1GHz, ΔT=250ps and L=1.4nH.

reciprocal/non-reciprocal responses based on the clocking scheme. In this work, we leverage the large bandwidth and miniaturization factors offered by these quasi-electrostatic delay lines proposed in [7] to realize an ultra-broadband N-port circulator with ultra-compact form-factor. These claims are validated through the implementation of the first CMOS instantaneously-ultra-wideband (UWB) circulator operating over DC-1GHz, with insertion losses of 3.1dB-4.3dB, matching<-15dB, isolation >18dB, and a miniaturization factor (defined as λ^2_{center}/Chip Area) of 1.9×10^6, representing about 100-1000× higher miniaturization over prior work.

II. Quasi-Electrostatic Delay Element

Fig. 1(a) shows a 2-port commutated N-path switched-capacitor network where the output switches are delayed with respect to the input set by time $\Delta T > T_s/N$. Such N-path networks have thus far been explored in two asymptotic regimes - filtering, where $RC >> T_s/N$ and sampling, where $RC << T_s/N$. In [7], a rather unexplored regime of $RC \approx T_s/N$ was investigated. In this case, the capacitors faintly track the input voltage, and subsequently

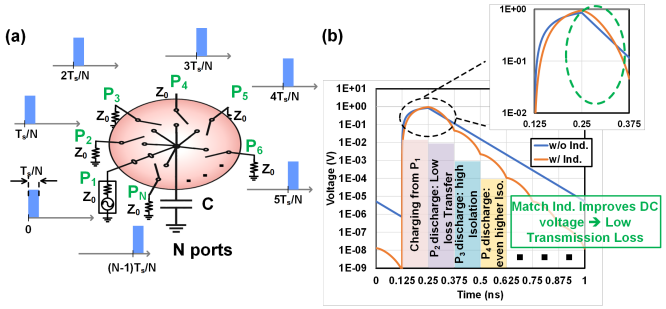

Fig. 2. (a) Schematic and timing diagram of an N-port switched capacitor layer based on the concept of electrostatic delay. (b) Evolution of the voltage on the shunt capacitor across time for an excitation at port 1 when f_s=1GHz, N=8, C= 1.25pF and L=1.4nH.

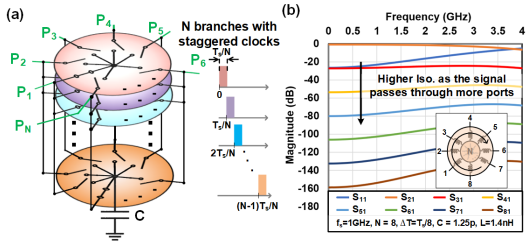

Fig. 3. (a) Schematic and timing diagram of the N-Way circulator realized using N-port switched capacitor layers. (b) Simulated S-parameters of the N-port circulator when f_s=1GHz, N=8, C= 1.25pF and L=1.4nH.

faintly discharge that voltage into the output port as shown in Fig. 1(b). The result is that the structure exhibits a low-loss broadband response with a true-time delay determined by the clock delay. Further, the network imparts non-reciprocal temporal delays in the forward and reverse directions of ΔT and $T_s - \Delta T$, respectively. To improve matching to the port impedance Z_0, small inductors can be added on either side of the network shown as in Fig. 1(a). It was shown that, for an 8-path network with C=1.25pF and f_s=1GHz, the small inductances of 1.4nH improve the matching and reduce insertion loss by about 8 dB and 1.2 dB, respectively (see Fig. 1(c)). The wave propagation in this network is termed quasi-electrostatic as the energy storage is primarily in the switched capacitors, and very little magnetic energy is stored in the small matching inductors.

III. Quasi-Electrostatic N-Port Circulator

This new delay element can be used to synthesize wideband microwave components with ultra-compact size. We extended the concept to an N-port commutated N-path network which exhibits extremely wideband N-way non-reciprocity.

A. N-port Switched Capacitor layer

Fig. 2(a) shows the circuit diagram of a shunt capacitor switched across N ports using N non-overlapping pulses. When operated in the quasi-electrostatic delay regime ($Z_0 C \approx T_s/N$), this circuit operates as a charge relay between the ports. The shunt capacitor is charged from one port, and most of this charge is subsequently released to the next port. For instance, when the switch at port 1 is closed, the voltage is recorded in the shunt capacitor at the center node. When the

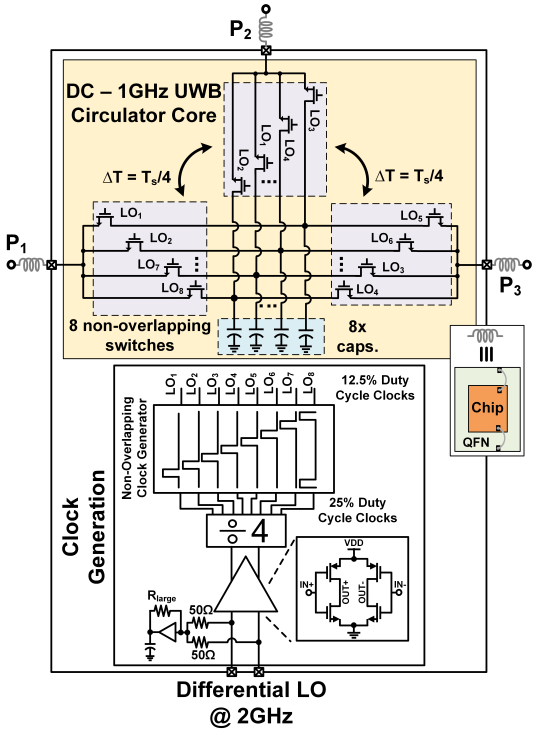

Fig. 4. Block diagram of the 3-port, 8-path UWB circulator implemented in standard 65nm bulk CMOS process.

switch at the port 2 is closed, this voltage is almost fully released to this port, resulting in low-loss transmission. The small residual voltage in the capacitor will be consecutively released to other ports when the corresponding switches are closed, resulting in progressively weaker transmission or stronger isolation (see Fig. 2(b) for a circuit with f_s = 1 GHz, N=8, C = 1.25 pF). Similar to the electrostatic delay case, adding small matching inductors (L=1.4nH in this case) at the ports improves the performance of this circuit by providing current boosting during both charging and discharging phases, thus improving the transmission to the subsequent port and increasing the isolation to other ports as shown in Fig. 2(b). However, since each port is connected only for $1/N^{th}$ of the total time, this network alone exhibits a transmission loss $\propto log(N)$ (in dB scale) and large harmonic conversion.

B. Ultra Wideband N-Port Circulator

To avoid this issue, this N-port switched capacitor layer is stacked with $(N-1)$ other identical layers in parallel operating in a time-intervleaved manner, as depicted in Fig. 3(a). In other words, this structure can be viewed as $N/2$ delay elements connected to each other at the central capacitor nodes. As mentioned earlier, the switches in each layer are modulated in a revolving fashion so that only one switch in each layer is connected to the capacitor at any time instant as shown in the switch timing diagram in Fig. 3(a). The time interleaving across layers ensures that each port is connected to only one capacitor at any instant. Similar to N-path filters, the usage of N non-overlapping layers ensures low loss transmission due to constructive

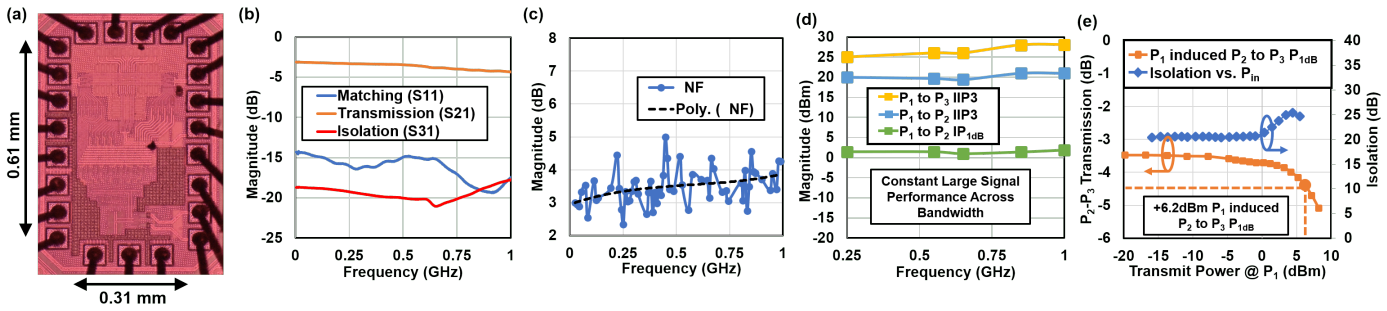

Fig. 5. (a) Chip microphotograph. Measured results of the DC-1GHz circulator: (b) S-parameters, (c) noise figure, (d) large signal performance, IIP3s and $P_{1dB}s$, and (e) TX-induced ANT-RX compression and isolation across TX power.

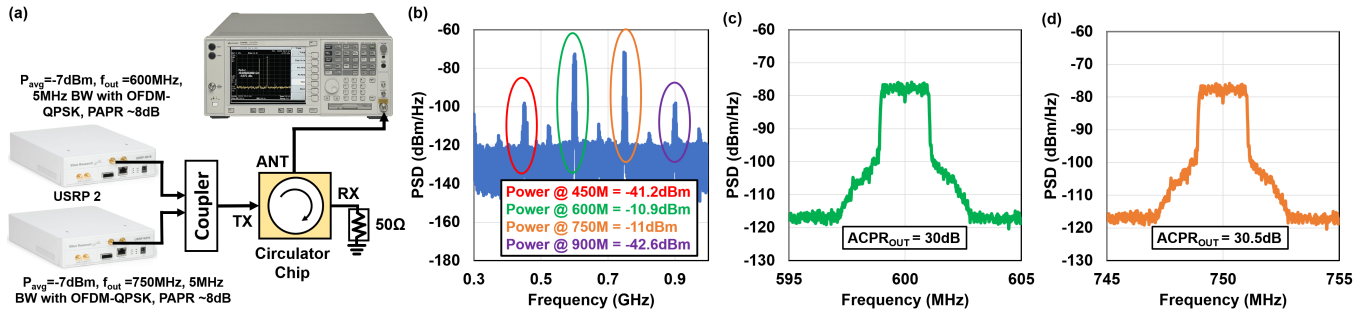

Fig. 6. (a) Measurement setup to evaluate the instantaneously-wideband performance of the circulator. (b) Received signal at second port P_2 when two signals with -7dBm average power, 5MHz bandwidth with OFDM-QPSK modulation (PAPR of ≈8dB) are provided at the first port P_1. (c) and (d) Zoomed version of the signal at 600MHz and 750MHz respectively.

summation at the fundamental frequency (f_{in}), and low harmonic conversion due to the destructive interference at inter-modulation frequencies ($f_{in} \pm Mf_m$) where M=1,2,3... and $M \neq$ multiples of N.

The revolving switching produces non-reciprocity and N-port circulation, i.e., transmission from port 1 to port 2, from port 2 to port 3, and so on, and isolation in the opposite direction. Fig. 3(b) shows the simulated S-parameters of an ideal 8-port circulator with f_s = 1 GHz, C = 1.25 pF and small series inductors of 1.4 nH at all ports for matching. Aliasing-free bandwidth of this circulator is $Nf_s/2$, while the circulator ideally has <3dB transmission loss from DC to $Nf_s/4$. Hence, by increasing the number of paths N, one can increase the bandwidth of this circulator. This architecture overcomes the limitations of prior non-magnetic CMOS circulators [2]-[5] that rely on quarter-wave structures, and are consequently limited in their instantaneous bandwidth. The matching inductors are small, and the circulator performance is not very sensitive to their specific value, enabling their realization using wirebond inductance, and consequently extreme miniaturization of the resultant circulator compared to prior art.

C. Implementation and Measurements

As a proof of concept, we implemented a 3-port UWB circulator in 65nm bulk CMOS. Fig. 4 depicts the block diagram, and Fig. 5(a) depicts the chip microphotograph. The circulator consists of 8 parallel non-overlapping layers, with each consisting of a 2.5pF capacitor connected to 3-ports through three $51\mu m/60nm$ transistors. For increased layout symmetry and improved parasitic performance, the shunt capacitors are divided into 3 equal parts and are connected symmetrically to all the three 8-phase modulating switches sets. As mentioned earlier, we leveraged the inductance from bond wires as the 3nH inductor required for matching, resulting in an extremely compact area of $0.19mm^2$. The clock path consists of pseudo-differential buffers to generate square-waves from the input 2GHz differential sinusoidal signals. These 2GHz square wave signals were divided by a factor of 4 and then fed to a non-overlapping clock-generator to generate the 8 phases of 500MHz, 12.5% duty cycle non-overlapping clocks required by the commutated switches. Fig. 5 shows the measurements. We measured symmetric performance across the 3 ports for 500MHz modulation and DC-1GHz operation, with transmission losses ranging from 3.1dB - 4.3dB, isolation > 18dB, matching < -15dB, and noise figure ranging from 3dB - 4dB. For 500MHz modulation, the circulator consumes 20mW in the clock generation. Measured transmission ($P_1 \rightarrow P_2$) IIP3 is +20dBm and remains constant across the bandwidth, while isolation ($P_1 \rightarrow P_3$) IIP3 ranges between +25dBm - +28dBm. Measured IP_{1dB} of the transmission path is +1.5dBm, while P_1-induced $P_2 - P_3$ transmission P_{1dB} (TX-induced ANT-RX compression) is +6.2dBm. The isolation is >18dB for this range of P_{TX}. Fig. 6(a) shows the measurement setup used for evaluating the instantaneously-wideband nature of the circulator. Spectral performance of the UWB circulator when two -7dBm, 5MHz, OFDM-BPSK signals (PAPR≈8dB) at 600MHz and 750MHz are incident at P_1 is shown in Fig. 6(b). Fig. 6(c) and (d) shows

Table 1. Performance Comparison with prior work.

		TMTT 2019 [1]	JSSC 2017 [2]	ISSCC 2017 [4]	ISSCC 2018 [3]	RFIC 2018 [5]	IMS 2019 [7]	This work
Architecture	Technique	STM-AM	N-path-filter circulator	Spatio-Temporal Conductivity Mod. across Delay Line	Hybrid-Coupler based N-path Circulator RX	Switched T-Line based Circulator	Sequentially Switched Delay Lines	UWB Circulator based on Commutated Switched Capacitor Networks
	Technology	180nm CMOS	65nm CMOS	45nm CMOS SOI	65nm CMOS	65nm CMOS	0.2µm GaN	65nm CMOS
	Center Frequency	0.91 GHz	0.61-0.975 GHz	25 GHz	0.725 GHz	0.95 GHz	0.55 GHz	0.5GHz
	Transmission BW	0.02 GHz	0.03 GHz	4.6 GHz	0.35 GHz	0.22 GHz	0.9 GHz	DC – 1GHz
	Modulation Freq.	0.1 GHz	1GHz	8.3GHz	1GHz	0.33 GHz	1.25 GHz	500MHz
	Off-Chip Components	Yes	Yes	No	Yes	No	No	No
	Supply Voltage	3.3 V	1.2 V	1.2 V	1.2V	2.5V	12V	1.3V
Small Signal	TX-ANT/ANT-RX Transmission	-4.8 dB/-4.8 dB [1]	-1.7 dB / -1.7 dB [1]	-3.3 dB / -3.2 dB [1]	-3.1 / 15 [1]	-2.1 dB / -2.9dB [1]	-3dB to -4.1dB/ -3dB to -4.1dB [2]	-3.1 dB to -4.3dB/ -3.1 dB to -4.3dB [2]
	TX-RX Isolation BW (BW/f_{center})	2.4% (>20dB)	1.9%(>25dB) 0.33%(>40dB)	>18.5 dB (18%) [3]	4.6% (>40 dB) 27% (>30 dB) [4]	17% (>25dB) 3.1% (>40 dB)	163% (>18dB) [5]	200% (>18dB)
	ANT-RX NF	5.2 dB	4.3 dB	3.3 dB - 4.4 dB	2.7 dB	3.1 dB	N/R	3.1dB – 4.1dB
Large Signal	TX-ANT/ANT-RX IP_{1dB}s	+6.1dBm / +6dBm	+27.5dBm/ N/R	>+21.5 dBm/ >+21dBm	N/R	>+30.66 dBm / 21dBm	17dBm / 17dBm	+1.4dBm/+1.4dBm
	TX-ANT/ANT-RX IIP3s	N/R / N/R	+8.7dBm/ N/R	20.1 dBm / 19.9 dBm	+25 dBm/ +4 dBm	+50.25dBm/+36.9dBm	N/R / N/R	+20 dBm / +20 dBm
	TX-RX Compression (20dB / 15dB Levels)	N/R	N/R	N/A / +21 dBm	N/R	+26dBm / >+29dBm	N/R	>+5dBm / >+5dBm
	TX-induced ANT-RX P_{1dB} Compression	N/R	N/R	N/R	+5.5 dBm	+21.3 dBm	N/R	+6.2dBm
Others	PDC	64mW	59 mW	78.4 mW	24 mW	170 mW	4100 W	20mW
	Chip Area [6]	36 mm^2 (λ^2/3018)	25mm^2 [1] (λ^2/6400)	2.16mm^2 (λ^2/66)	38.61mm^2 (λ^2/4435)	16.5mm^2 (λ^2/6043)	18.5mm^2 (λ^2/1.6×10⁴)	0.19mm^2 (λ^2/1.9×10⁶)

[1] Transmission losses at the center frequency. [2] Transmission losses across the wide bandwidth. [3] Limited by measurement setup. [4] Using an external tuner.
[5] Calculated from measurement plot. [6] λ is the free space wavelength at the center frequency. N/R – Not reported.

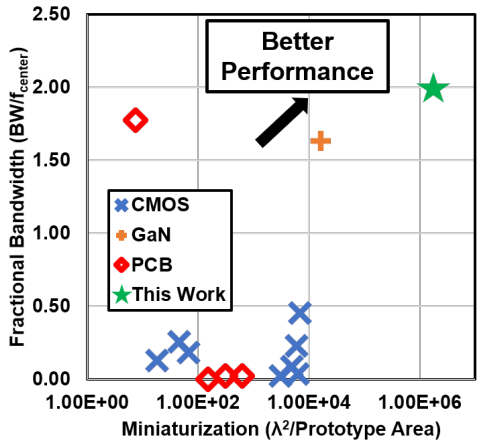

Fig. 7. Fractional bandwidth versus miniaturization factor of various circulator prototypes demonstrated in CMOS, GaN and PCBs.

the zoomed version of the received signal at 600MHz and 750MHz respectively. This measurement clearly demonstrates the ability of the circulator to simultaneously handle multiple signals spread across its instantaneously-wide bandwidth.

Table. 1 compares this paper to prior art. This represents the first instantaneously-ultra-wideband circulator implemented in CMOS while featuring a footprint that is 100-1000× smaller than prior art. Finally, Fig. 7 shows the comparison of various circulator prototypes in terms of the fractional bandwidth achieved versus the area miniaturization that was offered. As it can be seen, this concept of a UWB electrostatic circulator offers the best fractional bandwidth along with a huge miniaturization factor.

IV. Conclusion

In this work, we presented the novel concept of quasi-electrostatic wave propagation in N-port rotating switched capacitor networks to achieve ultra-broadband, low-loss N-way non-reciprocity. The non-resonant nature of such networks enables ultra-broadband operation bandwidth ranging from DC to $Nf_s/2$. Finally, the fact that these networks are largely composed of only switches and capacitors enables extremely-small form-factors. We envision that the concepts of ultra-broadband delays and N-way reconfigurable circulators will find many applications in wideband compact true-time-delay-based beamforming, wideband full-duplex wireless radios, and N-way reflection amplifiers targeting quantum computing applications.

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