Process Variation in Spoof Plasmon Interconnect: Consequences and Compensations

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***Abstract*— The concept of chip-to-chip information propagation by spoof surface plasmon polariton (SSPP) metasurface at terahertz frequency has been introduced of late, that promises data transfer with high bandwidth, low cross-talk, and low energy consumption. As the exotic electromagnetic properties of the metasurface derive from its designed geometric pattern and periodicity, any possible variation of fabrication process parameters may affect the design pattern and consequently the information capacity of SSPP interconnects. In this work, we have investigated the extent of performance degradation of SSPP interconnect with the statistical variation of geometric pattern of the metasurface. We also described the technique of the design of appropriate analog circuit so that the loss of signal integrity incurred by the process variation can be recuperated in real time.**

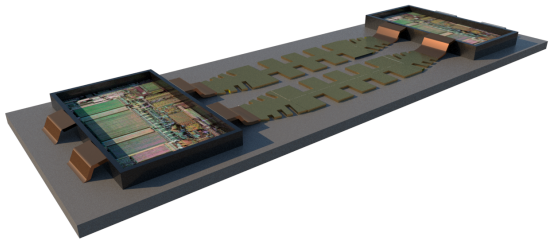
***Index Terms*— spoof plasmon, interconnect, variability, compensation technique**

I. Introduction

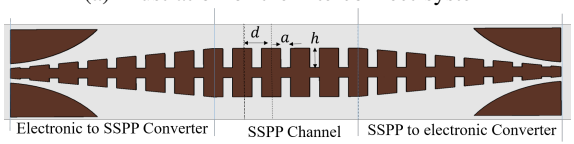
With aggressive scaling of the devices to keep up with Moore's law, we are inevitably entering a regime where the interconnects, rather than the logic devices become the most critical components for designing [1]. Very recently, Joy et al. [2] proposes a technique of information transfer over short distance, spanning 0.1-10 cm by spoof surface plasmon polariton (SSPP) at terahertz frequency, an entirely different class of quasiparticle accommodated by metallic surface with deliberate design pattern [3], illustrated in Fig. 1a.

Spoof plasmon interconnect is a novel communication system which leverages the unique electromagnetic properties of metasurface for high speed data transfer with low energy budget. Unlike conventional interconnects which incur aggravated signal fidelity at elevated frequencies owing to cross-talk, spoof plasmon channel demonstrates quite reverse trend: the cross-talk is suppressed further at high frequency end of its band— allowing the possibility of faster data transfer with signal integrity.

However, every new technology also poses its own challenges and raises new issues to address in order to test its feasibility. For instance, the unique ability of the metasurface to carry information with high fidelity is attributed to its carefully crafted geometric pattern [4]; and hence it might be critical to maintain signal integrity if the actual fabricated patterns on the metal incur random



(a) Illustration of the interconnect system



(b) Geometric features of SSPP channel, including the converter

Fig. 1: Spoof Plasmon Interconnect for chip-to-chip communication

variation due to fabrication process imperfection such as mask misalignment, diffraction in lithography, non-uniform metal deposition and polishing etc.

It might be argued that, the state-of-the-art fabrication technologies have become matured enough to provide sub-nanometer scale resolution [5], and therefore the study of the impact of process variation in SSPP structures with micron scale feature sizes is now mere an academic interest. While the argument is valid for a planar or horizontal interconnect structure, an act of metal patterning on a vertical direction in a multi-layered board of three dimensional large scale integration (3D-LSI) system [6] would definitely confront far more challenges, and could easily be resulted into significant pattern variation. Pattern variation may also result from post-fabrication process such as aging or electromigration.

In the present work, we delve into some practical fabrication non-idealities that can impact the performance of spoof plasmon channel. We investigate the frequency responses of an SSPP channel with geometric irregular

patterning; and elaborate the consequences of the pattern irregularity on the integrity of the transmitted digital signal; and explain how we can build compensating analog circuit in order to recuperate the loss in signal quality in real-time.

II. Frequency response of SSPP channel

A. SSPP channel with ideal pattern

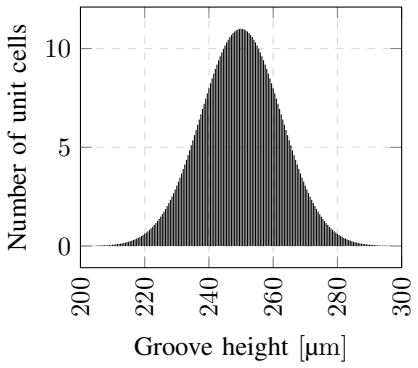


Fig. 2: Probability distribution of groove length in a 5 cm SSPP channel, where the length varies around the designed mean value by 3%

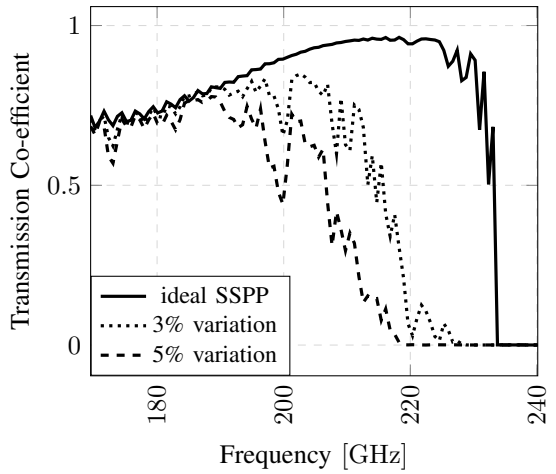


Fig. 3: Magnitude response of ideal SSPP, SSPP with 3% and 5% co-efficient of variance of the irregular metasurface pattern.

SSPP metasurface, as shown in Fig. 1b, is characterized by few features including length (h) and width (a) of groove, period (d) of an unit cell, thickness (t) of metal film, refractive index (n_s) of substrate. Among them, the most critical parameter happens to be h, since it determines the resonant frequency (ω_r). The detuning of the SSPP band-edge frequency (ω_B) from ω_r is proportional to the coupling between the modes in resonating groove and that in free space. The fundamental band of SSPP spans from zero frequency up to ω_B. The field confinement gradually increases as one proceeds along the band to the highest frequency ω_B.

B. SSPP with pattern irregularity

We assumed that the process variation would result in a Gaussian distribution of the feature size of SSPP metasurface, as such sorts of distributions are also reported in the features of standard VLSI interconnects [7]. In our model, the number of unit cells having groove length h is defined as follows:

$$N(h) = \frac{N_T}{\sigma_h\sqrt{2\pi}} exp\Big(- \frac{(h-h_m)^2}{2\sigma_h^2}\Big) \qquad (1)$$

Where N_T is the total number of unit cells in an SSPP channel, h_m is the mean value of groove length in the structure, and $\sigma_h^2 = 1/N_T \sum_i (h_i - h_m)^2$ is the variance of the distribution for h, which depends on the particular fabrication process. We have taken $h_m = 250$ μm, $d = 375$ μm, and $a = 125$ μm. The value of period d is chosen in a way so that we meet the condition $(2h > d)$ of yielding high field confinement zone of SSPP [3], but at the same time evade being into too deep SSPP region where the advantage of strong field confinement is smeared by the drawback of dispersion induced pulse distortion and heightened ohmic loss. The interconnect length is chosen as $L = 5$ cm with over 120 unit cells in the channel, a reasonably large number to test the impact of inhomogeneity in their geometric shape.

In order to study the impact of geometric shape variation of SSPP structure on the information capacity of the channel, we took different values of σ_h. For instance, for a 3% variation, the length of the groove h of all the unit cells in the 5 cm long channel will vary within the range of (250 ± 7.5) μm around the designed length of 250 μm, which corresponds to $3\sigma_h = 7.5$ μm. Figure 2 shows the Gaussian distribution of the groove lengths, centered around the mean value of 250 μm, that we have taken to simulate the behavior of SSPP channel with pattern irregularity.

III. Performance Loss for Structural Imperfections

A. Bandwidth degradations

Because of random variation of the length of groove in SSPP structure, the transmission characteristics over the frequency range is affected. Figure 3 shows the magnitude of transmission coefficient for different degree of co-efficient of variance of SSPP pattern irregularity. We defined the bandwidth of a perfect SSPP channel by the difference between the upper (f_U) and lower frequency (f_L). Beyond upper frequency f_U, the transmission magnitude drops below -3 dB, whereas below lower frequency f_L, the transmission coefficient drops below 0.7 due to the extension of mode beyond the optical cross-section area of the receiver. We observed that the upper cut-off frequency

is quite sensitive to the variation of groove length, and shows red-shift with the increase of σ_h. On the contrary, the lower cut-off frequency is relatively less sensitive to the variation of groove length.

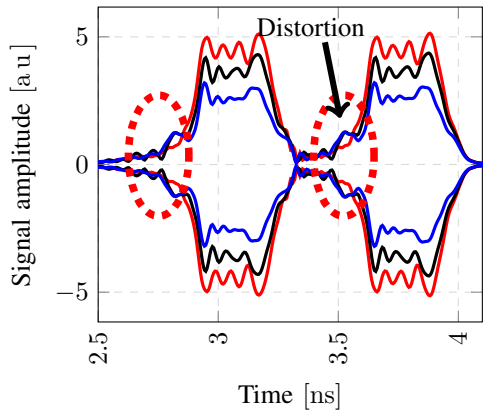


Fig. 4: Received signal after transmitting through ideal SSPP (red line), SSPP with 3% variation (black line) and SSPP with 5% variation (blue line), Besides signal attenuation, the signal also suffers from shape distortion, shown by the elliptical zone in the figure.

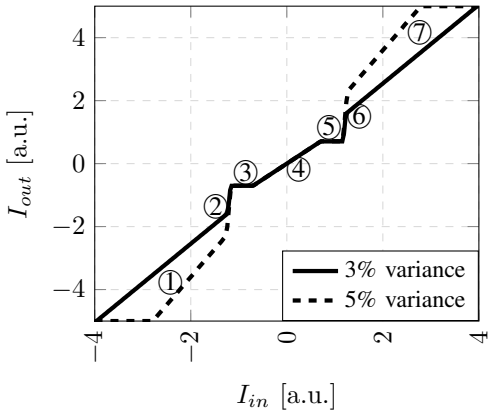


Fig. 5: Transfer function of nonlinear compensation circuit for different co-efficient of variance of structural irregularities in SSPP channel. The different linear pieces on a particular compensation function are designated with numbers from ① to ⑦

B. Loss of signal integrity

While transmitting data through SSPP channel, we restrict the bandwidth of the data pulse to be within $(225-180)$ GHz$=45$ GHz, the spectrum over which the transmission co-efficient of ideal SSPP remains roughly constant. We transmitted the double side-band data, hence the carrier frequency is selected to be the mid-frequency $f_{carrier} = (225+180)/2$ GHz ≈ 203 GHz of the available transmission window of SSPP channel. The input signal is taken as '1010' bit pattern, sampled at a frequency of $F_s = 2.75$ GHz, and is fed to the SSPP channel after appropriate filtering and modulation. Depending on the degree of of patterning irregularity in SSPP metasurface, the fidelity of the signal emerging from the other end of the channel aggravates. Figure 4 shows the time domain '1010' signals that emerge at the receiving side of SSPP channel. The comparison vividly shows that, with the pattern irregularity getting worse, the amplitude of the signal deteriorates. More importantly, due to the apparent non-uniform gain in the frequency response of the imperfect SSPP channel over the chosen 45 GHz bandwidth, the signal undergoes pulse-shape distortion, shown by red mark in Fig. 4, which complicates the design process of the compensation circuit for regaining signal quality.

IV. Mitigation of Performance Degradation

In order to determine the amplitude transfer function of the required compensating circuit, we have taken the envelop of the modulated signal of a '...000101000..' data stream that emerges through the receiving end of SSPP interconnect. Then we performed appropriate vector mapping in order to express the output signal amplitude of imperfectly shaped SSPP channel (with variance in groove length) as a function of that of perfect SSPP channel, and approximated the transfer function with a piece-wise linear function. Figure 5 shows the approximated transfer function of the compensating circuit.

In order to generate the particular non-linear response in the compensating circuit, we have chosen the technique of 'summation of current' in a circuit node, since addition of current can be as simple as joining wires to a common output node. The basic building blocks of our designed circuit are current mirrors (CM). The CM blocks are supplied with two bias currents, I_1 and I_2. One pair of the FET have a width ratio of $\frac{1}{\alpha}$. The I/O characteristics of each of the current mirror blocks is a straight line with a slope α, clipped at two different co-ordinates. Figure 6 shows the basic CM block and its amplitude transfer function. It has been shown in [8] that the above described CM blocks can be combined to generate arbitrary non-linear transfer function.

For concise representation of the final design of the full compensation circuit, we shall represent the CM block as a black box, characterized by the ratios of transistors' widths. In order to acquire the desired transfer characteristics (shown in Fig. 5) of the compensating circuit, we added the output node of five such CM blocks, where the ratios of transistors' widths of each of the CM blocks have been chosen carefully so as to generate the full transfer curve, as shown in Fig. 7. As the individual CM blocks cannot provide bidirectional current, we have to also add an offset current source at the input terminal of

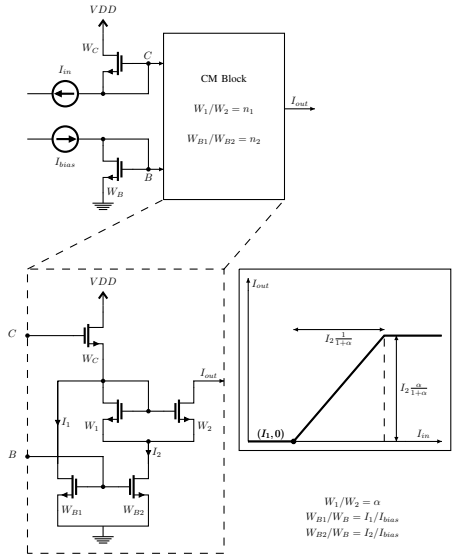


Fig. 6: Basic current mirror block of the compensation circuit with its piece-wise linear amplitude response shown in the inset. Such sort of blocks will be combined to construct the full compensation circuit.

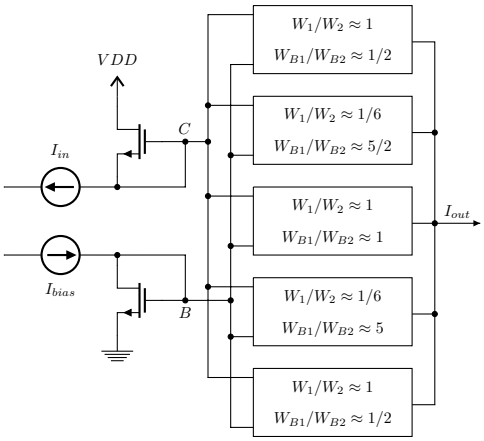


Fig. 7: Full circuit design for compensation of performance loss of SSPP channel for structural irregularity. The current mirrors are drawn in the form of black boxes, characterized by the ratios of transistor widths for concise representation.

the compensation circuit so as to shift the entire transfer curve either to the right or to the left of x-axis (i.e., to a quadrant of the Cartesian co-ordinate system where input current is unidirectional). The output of the compensation circuit will be fed to the next SSPP channel through a transformer so as to truncate the DC component from the output signal.

A. Dynamic Tunability of Compensation Circuit

Despite a standard fabrication process is characterized by minimum resolution features and expectation value of errors, it is unlikely that we would have a prior exact knowledge of the degree of variations in a specific sample of SSPP channel. Hence the compensation circuit ought to have the in-situ tunability, as the fine details of the input-output characteristics of the required compensating circuit depends upon the exact co-efficient of variance of geometric pattern of the particular sample interconnect chip. As suggested by our analysis, regardless of the degree of pattern irregularity, the required input-output amplitude transfer behavior of the compensation circuit remains mostly identical for region ③, ④, ⑤, designated on Fig. 5. The parts of the compensation function designated as region ①, ②, ⑥, ⑦ vary with the degree of geometric irregularity in terms of their slopes, where the slopes have to become steeper with increased degree pattern irregularity. The tunability of the compensation circuit can be readily obtained by inclusion of additional FETs parallel to that designated with transistor width W_2 in Fig. 6, each of the additional FETs will be controlled by a series connected transistor.

V. Conclusion

With the beginning of the era of 'tyranny of interconnect', the quest for a novel interconnect technology can potentially be satiated by spoof surface plasmon based channel, which gets rid of conventional parasitic effect such as channel capacitance and inductance. In this work, we look into practical aspect of employing SSPP interconnect and the collateral fabrication issues that may emerge with the introduction of the new technology, the ramification of the same in the channel performance, and the methodology for compensation for the degraded performance. We believe, this will be marked as an important step towards realization of the novel technology and integrating it with the standard CMOS fabrication process.

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