Digital Electronics as RFID Tags: Impedance Estimation and Propagation Characterization at 26.5 GHz and 300 GHz

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***Abstract*— This paper presents a circuit impedance model and results of propagation characterization at 26.5 GHz and 300 GHz for a new type of RFID tag that is based on digital electronics. This RFID tag leverages the backscatter radio generated from switching of transistors inside digital circuits, which does not need antennas or RF front-end circuits thereby further reducing the device's form factor. Moreover, the proposed RFID tag is compatible with a wide range of interrogating frequencies and can be implemented on existing electronics without additional cost. The proposed circuit impedance model explains the modulation mechanism of this new backscatter radio and provides an estimation of digital circuits' impedance using SPICE model parameters. Based on the proposed circuit impedance model, we develop a modified modulation loss factor to estimate the modulation loss resulting from the switching activity of the digital electronics. Furthermore, propagation characterization is conducted at 26.5 GHz and 300 GHz, where the shadowing gain for the carrier power and the backscattered power is characterized as 3.93 dB and 0.96 dB at 26.5 GHz, and 1.01 dB and 0.52 dB at 300 GHz, respectively, showing that the backscatter channel can provide a more reliable link that is resistant to the constructive and destructive interference from the multipaths as compared to the carrier channel.**

***Index Terms*— Radio frequency identification, RFID, backscatter radio, propagation characterization, link budget.**

I. Introduction

Radio-frequency identification (RFID) system has been widely used for supply chain management, asset tracking, data exchange, telemetry, access control, etc. [1]–[9]. The RFID market is worth several billion dollars today, and is expected to grow $>$ 10 % per year [10]. Traditional RFID is based on backscatter radio, where a reader sends a continuous carrier wave (CW) to a tag and retrieves information from a modulated wave backscattered from the tag. During backscatter operation, the input impedance of a tag antenna is intentionally mismatched by two-state RF loads (Z_0 and Z_1) to vary the tag's reflection coefficient and radar cross section (RCS) and to modulate the incoming CW [11], [12]. Using such approach, existing RFID tags have inflexible form factor and limited room for further miniaturization since they all need to use the antenna, which is the largest part of the tag [13]. Moreover, current RFID tags can only be interrogated at specific frequencies due to antenna's frequency-selective characteristics. To further miniaturize the backscatter communication systems and enhance the coding capacity, a new backscatter architecture that can operate without antennas and is compatible with a wide range of interrogating frequencies needs to be developed.

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A. Related Work

Our previous work [14] proposed a semi-passive RFID tag based on a new class of backscatter radio generated from switching of transistors in digital electronics, where the impedance difference between transistor gates in the high-state and in the low-state changes the radar cross section (RCS) and modulates the backscattered signal. The proposed RFID tag does not need antennas or any RF front-end circuits thereby further reducing the device's form factor. Moreover, the proposed RFID tag is compatible with a wide range of interrogating frequencies from sub-6 GHz up to millimeter-wave frequencies, and can be implemented on existing digital electronics, e.g., field-programmable gate array (FPGA), with zero additional cost. Simulation results have shown the potential of implementing the proposed RFID tag on application-specific integrated circuit (ASIC) to enhance the backscatter signal and to further miniaturize the size of the tag. The applications of the static and dynamic IDs, where the static ID can transmit up to 36 bits simultaneously and provide up to 68.7 billion (2^{36}) combinations of unique IDs and the dynamic ID can achieve a data rate of 100 kbits/sec with a bit error rate (BER) of 0.00000183 (10^{-6}), have been demonstrated. The number and pattern of bits are fully re-configurable, and the flexible bit design does not occupy additional space on the printed circuit board of the FPGA as the number of bits increases.

Since the proposed RFID tag is based on a new backscatter radio, its backscatter mechanism needs to be understood and modeled. In [14], we proposed a simplified circuit impedance model that consists of the resistance of the NMOS and PMOS transistors, where the difference of resistance between transistor gates in the high-state and in the low-state can change the RCS and modulate the incoming CW. However, the simplified circuit impedance model does not include transistors' parasitics, which would influence the transient behavior of the transistors [15]. Furthermore, propagation of this new

backscatter channel needs to be characterized to assess link budget, which is important for evaluating the feasibility and reliability of a wireless link. Although backscatter radio's link budget has been demonstrated in the ultra high frequency band (UHF, in the range of 300 MHz–3 GHz) [12], [16], [17], it does not provide the estimation of the modulation loss resulting from the switching activity of the digital electronics, and thus cannot be directly applied to the proposed backscatter radio link.

B. Contribution

As seen from the above literature survey, there is a lack of development of complete circuit impedance model and propagation characterization for this new backscatter radio. This paper attempts to fill this gap. A circuit impedance model that includes transistors' equivalent resistance and reactance is developed to explain the modulation mechanism of the proposed backscatter radio and to describe the relation between the total input impedance and the logic resources of the digital circuits. The procedure of estimating digital circuits' impedance (resistance and reactance) from SPICE model parameters is also presented. Based on the proposed circuit impedance model, a modified modulation loss factor is derived to estimate the modulation loss resulting from the switching activity of the digital electronics. Furthermore, propagation characterization of the carrier power and backscattered power is conducted at 26.5 GHz and 300 GHz with the shadowing gain analyzed at various transmitter (Tx)-receiver (Rx) distances. The 26.5 GHz frequency is selected since it belongs to the FR2 band of the 5G spectrum [18] and is promising to deliver multi-gigabit-per-second data rates [19], [20]. The 300 GHz frequency is chosen since it provides a higher data rate with its larger bandwidth and lower interference (because of the directional antennas) [21]–[24]. An IEEE 802.15.3d [25] standard for THz communication proposed a data rate of up to 100 Gbit/s at 252–325 GHz using eight different bandwidths between 2.16 GHz and 69.12 GHz. In addition, smaller antenna form factor at millimeter-wave/THz frequencies results in a shorter Fraunhofer distance and guarantees far-field propagation for the measurement distances we studied.

The remainder of the paper is organized as follows. Section II presents a circuit impedance model that explains the modulation mechanism of the proposed backscatter radio. Section III describes the procedure of estimating digital circuits' impedance from SPICE model parameters. Section IV introduces the design methodology of the proposed RFID tag. Section V presents the measurement setup and examples of the measured spectra of the modulated sidebands. Section VI presents the characterization of the carrier power and the backscattered power at 26.5 GHz and 300 GHz in a non-line-of-sight (NLoS) link with an FPGA board serving as a reflector/RFID tag. Finally, Section VII provides some concluding remarks.

II. Equivalent Circuit Model

This section presents a circuit impedance model that includes transistors' equivalent resistance and parasitic capacitance to explain the modulation mechanism of the proposed backscatter radio.

Traditional backscatter communication in Fig. 1 (a) refers to a radio channel where a reader sends a CW to a tag and retrieves information from a modulated wave backscattered from the tag. During backscatter operation, the input impedance of a tag antenna is intentionally mismatched by two-state RF loads (Z_0 and Z_1) to vary the tag's reflection coefficient and modulate the incoming CW [11]. Compared to the traditional RFID backscatter modulation scheme, the proposed RFID tag in Fig. 1 (b) modulates the incoming CW by switching activity in digital logic, e.g., programmable flip-flops inside an FPGA chip. The equivalent impedance of the digital logic (transistors) changes as the toggling pattern and the number of toggled flip-flops change. Such impedance variation in the digital logic modulates the incoming CW in a form of amplitude modulation. As a result, the proposed RFID tag does not require pre-designed antennas, two-state RF loads (Z_0 and Z_1), or RF front-end circuits (e.g., matching networks, resonant circuits, etc.). By controlling the activity of the chip's logic and flip-flops, we can transmit information through backscatter modulation.

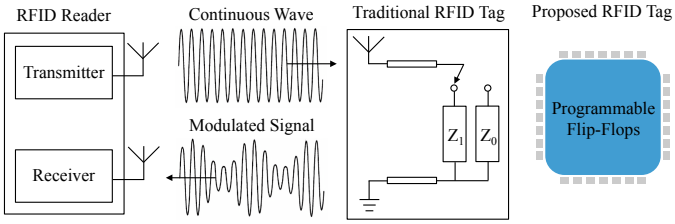


Fig. 1. Illustrations of the (a) traditional RFID tag and the (b) proposed RFID tag.

Transistors' equivalent impedance ($Z_{1/0}$) consists of resistance ($R_{1/0}$) and reactance ($X_{1/0}$), where $R_{1/0}$ is the real part of the high/low state impedance and $X_{1/0}$ is the imaginary part of the high/low state impedance, i.e., $Z_{1/0} = R_{1/0} + jX_{1/0}$. Resistance and reactance together determine the magnitude and phase of the impedance. According to [15], the equivalent reactance ($X_{1/0}$) of transistors is dominated by the parasitic capacitance of the transistors, i.e., $X_{1/0} \approx -1/(\omega C_{1/0})$, whereas transistors' parasitic inductance can be overlooked due to the relatively short channel length as technology node further miniaturizes. As a result, the proposed circuit model focuses on the equivalent R and C of the transistors.

The equivalent circuit impedance model is developed based on an FPGA due to its re-configurability. The "programmable/re-configurable" term in FPGAs indicates their ability to implement a new function on the chip after its fabrication is complete. A simplified internal structure of an FPGA is shown in Fig. 2 (a), where logic blocks are connected by programmable-routing interconnects and arranged in a two-dimensional grid. This symmetrical grid is connected to I/O blocks which make off-chip connections. Logic blocks can be simplified as programmable flip-flops. The output circuit of flip-flops consists of multiple inverters [26]. An equivalent output circuit of a CMOS inverter is shown in Fig. 2 (b). During the steady state, when input voltage of the inverter is

low, NMOS transistors are off and PMOS transistors are on. A direct path exists between V_{out} and V_{DD}, resulting in a high output state. On the other hand, high input results in a low output state. As shown in Fig. 2 (c), there exists a finite resistance between the output and V_{DD}, R_1 (or R_p, PMOS on-resistance), and between the output and the ground, R_0 (or R_n, NMOS on-resistance), respectively. During the transient

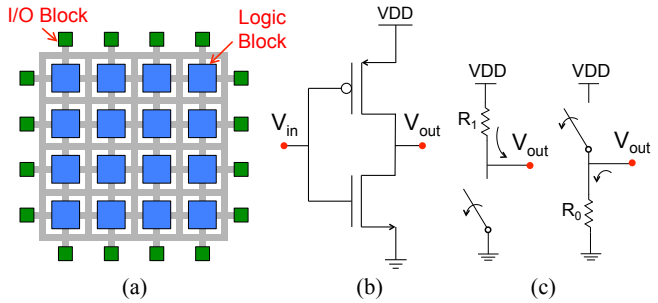


Fig. 2. (a) Simplified internal structure of an FPGA; (b) equivalent output circuit of a CMOS inverter; (c) high-state resistance, R_1 (PMOS on-resistance), and low-state resistance, R_0 (NMOS on-resistance).

state, that is, when the input voltage of the inverter is switching from low to high and from high to low, parasitic capacitance would influence the transient behavior of the cascaded inverter pair [15]. An equivalent output circuit of the cascaded inverter pair during transient state is shown in Fig. 3, where C_{gd} is the gate-drain capacitance, C_{db} is the diffusion capacitance, C_g is the gate capacitance of fanout, C_w is the wiring (interconnect) capacitance, and N is the fanout number of the cascaded inverters (assumed as 1 in this work). For simplification, all the capacitances are lumped together into one single capacitor C_L located between V_{out} and ground.

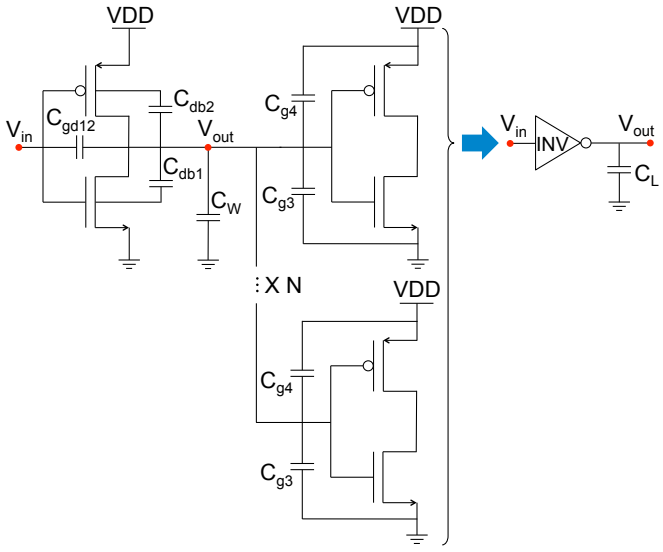


Fig. 3. Parasitic capacitance observed at the output of the cascaded inverter during transient state.

III. Impedance Estimation

This section describes the procedure of estimating the impedance of the proposed equivalent circuit model (introduced in Section II) from SPICE model parameters.

Link budget is a commonly used metric to evaluate the coverage of a radio system. Backscatter radio's link budget is expressed as follows [12]

$$P_{\text{rx\_backscattered}} = \frac{P_{\text{tx}} G_{\text{tx}} G_{\text{rx}} L_{\text{refl}}^2 M \lambda^4}{(4\pi d)^4}, \quad (1)$$

where $P_{\text{rx\_backscattered}}$ is the received backscattered power, P_{tx} is the transmit power, G_{tx}/G_{rx} is the Tx/Rx antenna gain, L_{refl} is the reflection loss of the tag, M is the modulation loss factor, λ is the wavelength, and d is the distance between the Tx/Rx and the tag. The existing modulation loss factor, M, does not accommodate the modulation loss caused by the switching of digital circuits since the estimation of digital circuits' impedance is not available, therefore, cannot be directly applied to the proposed backscatter radio that is based on digital electronics. To fill this gap, we propose a modified M that interprets the tag impedance as a function of logic utilization of digital circuits.

From a power delivery network point of view, the output impedance of digital circuits is the parallel combination of output impedances of individual logic (simplified as flip-flops in this work) [27]. The more logics (flip-flops) are connected, the more NMOS/PMOS transistors are connected in parallel, which reduces impedance. That is, the total input impedance of the proposed RFID tag is inversely related to the logic utilization. Given this relationship between logic utilization and input impedance, a modified M can be expressed as [12]

$$M(x\%) = \frac{1}{4}\left|\frac{Z_1(x\%) - 377^*}{Z_1(x\%) + 377} - \frac{Z_0(x\%) - 377^*}{Z_0(x\%) + 377}\right|^2, \quad (2)$$

where $Z_1(x\%)$ and $Z_0(x\%)$ are the estimated high state (1s) impedance and low state (0s) impedance of the tag, and parameter x represents the percentage of total logic resources being configured. $Z_1(x\%)$ and $Z_0(x\%)$ are defined as

$$Z_1(x\%) = \frac{Z_1(10\%)}{\frac{x\%}{10\%}}, \quad (3)$$

and

$$Z_0(x\%) = \frac{Z_0(10\%)}{\frac{x\%}{10\%}}. \quad (4)$$

$Z_1(10\%)$ and $Z_0(10\%)$ are the estimated high state (1s) and low state (0s) impedance of an FPGA chip with 10 % of total resources utilized. Note that we select 10 % since it is less than the smallest logic utilization being configured in this work, which is 15 %. The parameter x is in the denominator since the input impedance of the digital circuits is inversely related to the logic utilization, x. The input impedance of the tag is equal to free space impedance, 377 Ω, since there is no antenna but only air at the interface between the carrier signal and FPGA chip.

In order to estimate $Z_0(10\%)$ and $Z_1(10\%)$, we first calculate the values of $R_{1/0}$ and $X_{1/0}$ using transistor's SPICE model parameters (22nm PTM LP model in [28], which shares the same technology node as the Altera Cyclone V FPGA we use) to determine a range for $R_{1/0}$, $X_{1/0}$, and then perform curve fitting between the measured backscattered power and

the modeled backscattered power to estimate the optimal value of $Z_{1/0}$. According to [29], R_n (R_0) and R_p (R_1) can be estimated by $R_{n/p} = (R_{lin,n/p} + R_{sat,n/p})/2$, where $R_{lin,n/p}$ and $R_{sat,n/p}$ are the on-resistance of the NMOS/PMOS in the linear and saturation regions, respectively, and can be calculated as

$$R_{lin,n/p} = \frac{V_{lin}}{I_{lin}} = \frac{(V_{DD} - V_{SS} - V_{th,n/p})/2}{\frac{3}{8}k'_{n/p}(\frac{W}{L})_{n/p}(V_{DD} - V_{SS} - V_{th,n/p})^2}, \quad (5)$$

and

$$R_{sat,n/p} = \frac{V_{sat}}{I_{sat}} = \frac{V_{DD} - V_{SS}}{\frac{1}{2}k'_{n/p}(\frac{W}{L})_{n/p}(V_{DD} - V_{SS} - V_{th,n/p})^2}. \quad (6)$$

$k'_{n/p}$ represents $u_{n/p}C_{ox}$, where $u_{n/p}$ is the mobility of the NMOS/PMOS and C_{ox} is the gate capacitance. W and L are the width and length of the transistor, respectively. V_{SS} and V_{DD} are the source and drain voltage, respectively. $V_{th,n/p}$ is the threshold voltage of the NMOS/PMOS. Detailed values of the above parameters can be found in [15], [28], [30]. The expressions and estimated values of the parasitic capacitances C_{gd}, C_{db}, C_g, C_w, and C_L are presented in Table I. The total reactance ($X_{1/0}$) is then estimated by $X_{1/0} \approx -1/(\omega C_{L1/L0})$, whereas transistors' parasitic inductance can be overlooked due to the relatively short channel length as technology node further miniaturizes [15]. The definitions of the corresponding parameters are presented in Table II and detailed parameter values are provided in [15], [28], [30]. Figs. 4 and 5 present

TABLE I

ESTIMATED VALUES AND EXPRESSIONS OF THE PARASITIC CAPACITANCE

Capacitor	Expression	Value (fF)	
		High-to-Low	Low-to-High
C_{gd1}	$2C_{on}W_n$	0.0143	0.0143
C_{gd2}	$2C_{op}W_p$	0.0143	0.0143
C_{db1}	$K_{eqbpn}AD_nCJ_n + K_{eqswn}PD_nCJSW_n$	0.0524	0.0662
C_{db2}	$K_{eqbpp}AD_pCJ_p + K_{eqswp}PD_pCJSW_p$	0.0692	0.0584
C_{g3}	$C_{ox}W_nL_n + (2C_{on})W_n$	0.074	0.074
C_{g4}	$C_{ox}W_pL_p + (2C_{op})W_p$	0.074	0.074
C_w	From extraction	0.085	0.085
C_L	$C_{gd1}+C_{gd2}+C_{db1}+C_{db2}+(C_{g3}+C_{g4})*N+C_w$	0.383	0.386

the resistance ($R_{1/0}$), reactance ($|X_{1/0}|$), and the corresponding modulation loss factor (M) estimated from the 26.5 GHz and 300 GHz measurements, respectively. Please note that as logic utilization reduces below 15% and 20% in Figs. 4 and 5, respectively, data are not available because the measured backscattered power decreases below noise floor.

IV. RFID DESIGN METHODOLOGY

This section introduces the design metrics for the proposed RFID tag [14], such as transistors' switching pattern, modulating frequency (f_m), and logic utilization (%).

TABLE II

DEFINITIONS OF THE PARAMETERS FOR THE PARASITIC CAPACITANCE

Parameter	Definition
$C_{ox\_n/p}$ (fF/um^2)	Gate CAP (CAP per unit area by gate oxide)
$C_{on/p}$ (fF/um)	Overlap CAP
$CJ_{n/p}$ (fF/um^2)	Bottom junction CAP
$CJSW_{n/p}$ (fF/um)	Sidewall junction CAP
$AD_{n/p}$ (um^2)	Drain area
$PD_{n/p}$ (um)	Drain perimeter
$K_{eqbpn/p}$	Bottom plate capacitor linearization factor
$K_{eqswn/p}$	Sidewall capacitor linearization factor

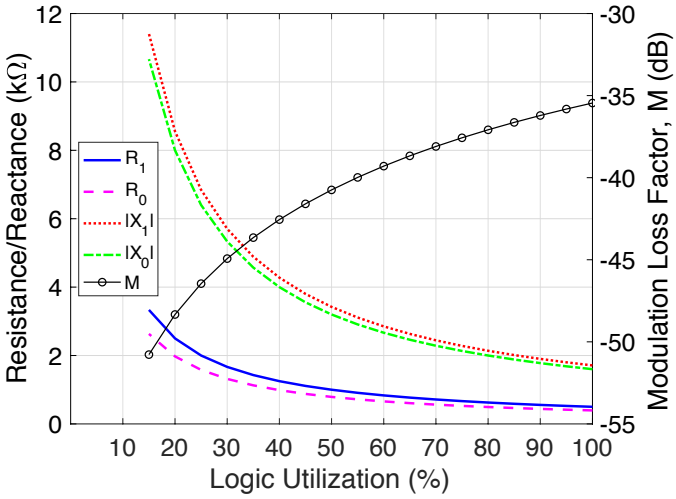


Fig. 4. Estimated values of R_1, R_0, $|X_1|$, $|X_0|$, and modulation loss factor (M) with respect to logic utilization (%) for the 26.5 GHz measurement.

The switching between inverter's high output state (Z_1) and low output state (Z_0) creates impedance variation, which is analogous to the variation in antenna terminating impedance in typical RFID tags. The impedance variation creates a difference in the circuit's RCS and thus modulates the incoming CW. We program the flip-flops switching in a pattern shown in Fig. 6 (a) to create impedance variation, where flip-flops continuously switch between high state and low state at a clock frequency (f_{clock}) of 50 MHz for half of the cycle and stay quiet for the other half of the cycle. The modulating frequency (f_m in Fig. 6 (a)) directly affects the bandwidth of the modulated signal, i.e., the first harmonic of the modulated backscattered signal will be located at $f_{carrier} \pm f_m$. The modulated signals can be easily upshifted or downshifted by changing the f_m, which makes the design very flexible. Please note that f_m should be selected to comply with radio regulations and avoid interference from other radio systems. To avoid undesired harmonics in higher frequencies caused by the ideal square pulses from the switching transistors, the highest sideband (f_m) needs to be less than three times of the lowest sideband (f_m) since an ideal square pulse has harmonics at odd multiples of the fundamental modulating frequency. In practice, the switching transistors produce pulses that have rising and falling edges rather than ideal square pulses, which

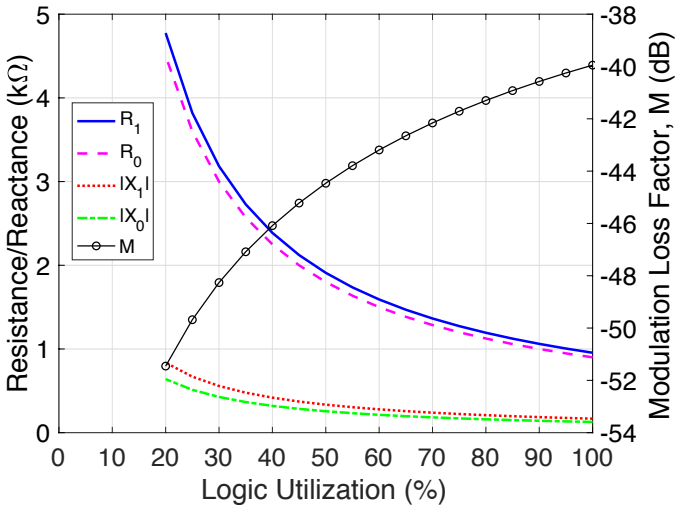


Fig. 5. Estimated values of R_1, R_0, $|X_1|$, $|X_0|$, and modulation loss factor (M) with respect to logic utilization (%) for the 300 GHz measurement.

sometimes leads to appearance of harmonics at even multiples of the modulating frequency. In such case, to avoid undesired harmonics, the highest sideband (f_m) should be less than two times of the lowest sideband (f_m).

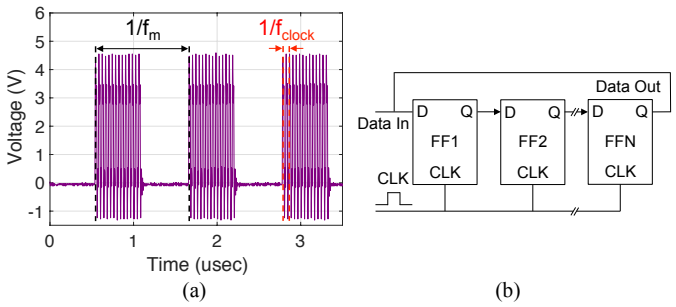


Fig. 6. (a) Measured voltage at the output of the flip-flops switching at f_m=900 kHz; (b) simplified building block of an N-bit shift register.

Board components that have periodic behavior, such as voltage regulators, typically produce signals in a frequency range that is much lower than a processor clock. One of the reasons for that is to minimize the interference from periodic activities that tend to produce multiple harmonics. When designing the proposed RFID tag, knowledge of frequencies of on-board periodic activities will help determine where to allocate the modulated sidebands [14]. The potential interfering frequencies caused by other board components can be identified by the method proposed in [31].

Apart from the switching pattern, the number of simultaneously switched logic elements is another factor that affects backscatter modulation. The more flip-flops switch synchronously, the stronger the backscattered signal becomes. To control the number of logic elements switching simultaneously, we configure N-bit shift registers out of flip-flops that consist of a large number of inverters connected in parallel, where N is used to adjust the number of simultaneously toggled flip-flops. Fig. 6 (b) shows a simplified building block for an N-bit shift register created by connecting multiple flip-flops. A shift register is a group of flip-flops set up in a linear fashion with their inputs and outputs connected together such that the data are shifted from one device to another when the circuit is active. Here we use linear feedback shift registers (LFSRs), i.e., we connect the most significant bit, MSB (FFN in Fig. 6 (b)) back to the least significant bit, LSB (FF1 in Fig. 6 (b)) to cause the function to endlessly cycle through a sequence of patterns. Fig. 7 presents the mapping of the logic resources of an Altera Cyclone V FPGA chip with various values of N, where dark blue blocks denote utilized logic resources while light blue blocks represent unused logic resources. The Cyclone V FPGA has logic utilization of 30%, 50%, and 100% with corresponding values of N=10980, N=18300, and N=36600, respectively. Note that other FPGAs may contain different numbers of programmable logic elements (total available N) such that same logic utilization (%) may require different values of N.

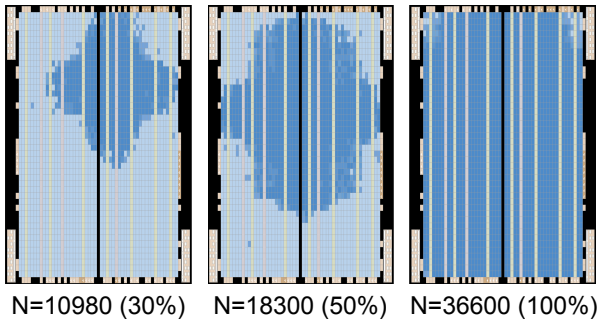


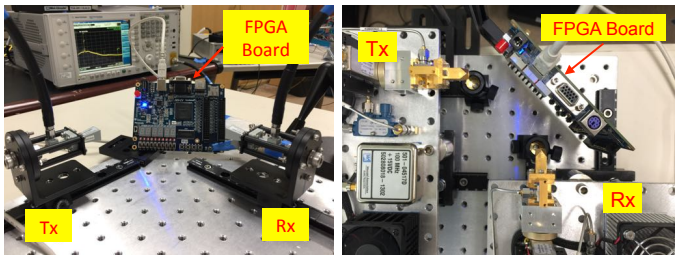
Fig. 7. Mapping of the logic resources of an ALTERA Cyclone V FPGA [14].

V. Demonstration of Backscatter Modulation From Switching of Transistors in Digital Electronics

This section presents the 26.5 GHz and 300 GHz measurement setups and examples of the measured spectra of the modulated sidebands generated by the switching transistors in an FPGA board.

A. Measurement Setup

In the 26.5 GHz measurement setup shown in Fig. 8 (a), an Agilent MXG N5183A Signal Generator with input power (P_t) of 15 dBm (31.6 mW) and $f_{carrier}$=26.5 GHz is used as a signal source and an Agilent MXA N9020A Vector Signal Analyzer is used to record the signals. For interrogation, we use standard gain horn antennas that operate from 26.5 GHz to 40 GHz with 55° half-power beam width (HPBW) and an average isotropic gain of 10 dBi ($G_{\rm tx}$/$G_{\rm rx}$). The 300 GHz measurement setup shown in Fig. 8 (b) consists of Virginia Diodes, Inc. (VDI) transceivers (Tx210/Rx148) [32] with P_t=0 dBm (1 mW). Detailed instrument descriptions can be found in [24]. Standard gain horn antennas with HPBW of 10° and an average isotropic gain of 22 dBi ($G_{\rm tx}$/$G_{\rm rx}$) are used for interrogation. An Altera DE0-Cyclone V FPGA board is used



(a) (b)

Fig. 8. Measurement setups for the (a) 26.5 GHz and (b) 300 GHz measurements.

as the RFID tag with a switching frequency (f_m, shown in Fig. 6 (a)) of 900 kHz and logic utilization of 100%.

Please note that in this work, we implemented the proposed RFID tag on an FPGA board as a proof of concept. The proposed tags can also be implemented on existing digital electronics with zero additional cost with a form factor as small as the chips or ASICs inside digital electronics [14].

B. Measurement Results

Figures 9 and 10 present the measurement results of the 26.5 GHz and 300 GHz measurements, respectively. The

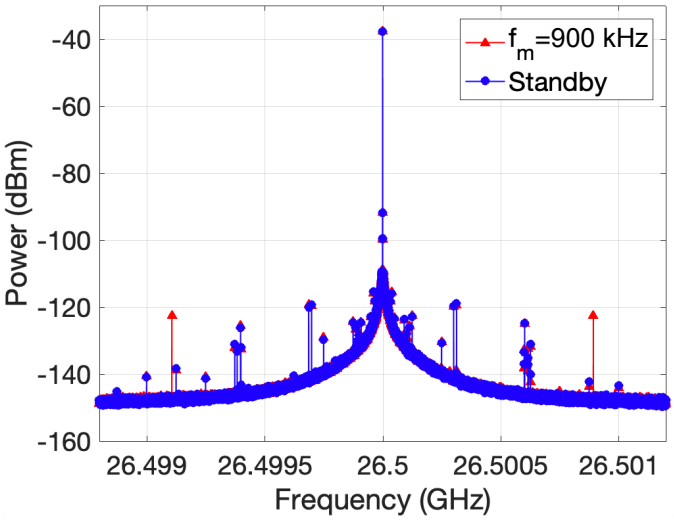


Fig. 9. Measured backscattered power with $f_{carrier}$=26.5 GHz and f_m=900 kHz (red triangle). The standby curve (blue circle) is the measured backscattered signal when the FPGA board is turned on but not switching.

standby curves (blue circles) represent the measured power spectra when the FPGA board is turned on but not switching. Distinct modulated sidebands with power level of -122 dBm (SNR=26 dB) and -136 dBm (SNR=15 dB) can be observed at 26.5 GHz $\pm$ 900 kHz and 300 GHz + 900 kHz (only the upper half of the spectrum was recorded at 300 GHz), respectively. In the standby mode, other modulated sidebands around carrier frequencies are also observed. Since the measurements are conducted in an indoor office environment, these modulated sidebands are results from surrounding interference, e.g., measurement instruments, LCD monitors, mobile phones, WiFi routers, etc. Note that conductive traces on an FPGA

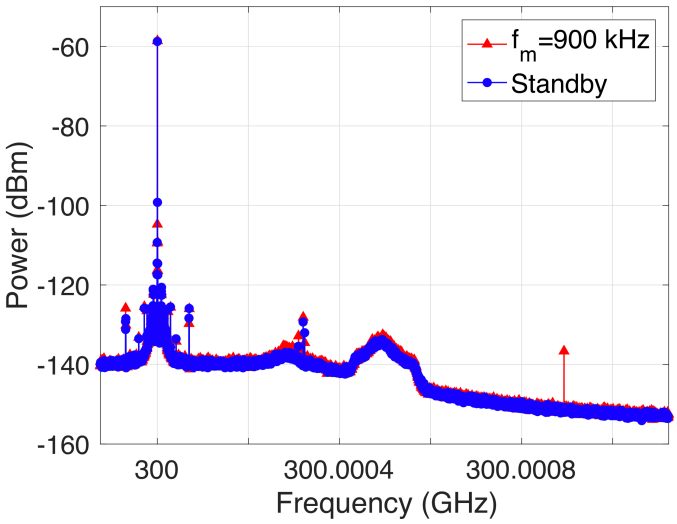


Fig. 10. Measured backscattered power with $f_{carrier}$=300 GHz and f_m=900 kHz (red triangle). The standby curve (blue circle) is the measured backscattered signal when the FPGA board is turned on but not switching.

board that connect the FPGA chip to GPIO pins may act as antennas and radiate the backscattered signal. To verify that the backscatter modulation solely results from the switching activity within the FPGA chip rather than with the assistance of the conductive traces on the board acting as antennas, we disconnect these traces (the I/O ports of the FPGA chip are switched off such that transistors' switching signal is "trapped" inside the FPGA chip) for all the RFID designs used in this paper. When the I/O ports of the FPGA chip are switched on, stronger backscattered signal has been observed. Our experiment results in Figs. 9 and 10 verify that switching electronics can establish backscatter links without antennas or RF front-end circuits, and can be interrogated across a wide range of frequencies. Please also note that the hump in the noise floor in Fig. 10 is generated from the 300 GHz transceivers.

VI. Propagation Characterization at 26.5 GHz and 300 GHz

This section presents the characterization of the carrier power and the backscattered power at 26.5 GHz and 300 GHz in a NLoS link with an FPGA board serving as a reflector/RFID tag.

A. Carrier Power Analysis

To characterize the carrier power, an empirical model that is similar to the floating-intercept (FI, the 3rd Generation Partnership Project 3GPP, or alpha-beta) pathloss model in [33, pp. 16–21], [20] is used except that the value being modeled is the received power in dBm rather than the pathloss in dB, which is expressed as

$$P_{\text{rx\_carrier}}(d)[\text{dBm}] = \alpha + 10 \cdot \beta \cdot \log_{10}\left(\frac{d}{d_0}\right) + X_{\sigma}^{P_{\text{rx\_carrier}}}, d \geq d_0, \quad (7)$$

where $P_{\text{rx\_carrier}}$ is the received carrier power in dBm as a function of d. Parameter α is a floating intercept in dBm that represents the modeled received power at a reference distance (d_0), which is the shortest distance we measured. The absolute value of parameter β in (7) is equivalent to the pathloss exponent (PLE), which characterizes the received carrier power's dependency on d. $X_\sigma^{P_{\text{rx\_carrier}}}$ is the large-scale shadowing that can be modeled as a zero-mean Gaussian distributed random variable with a standard deviation σ in dB. The carrier power model parameters (α, β, and σ) are estimated by performing the least-squares linear fitting through the measured carrier power such that the root-mean-squared (RMS) deviation from the mean carrier power is minimized.

In the 26.5 GHz measurement, the same setup presented in Fig. 8 (a) is used. Note that when characterizing a propagation channel, it is important to ensure the measurements are conducted in the far-field range. The largest physical dimension of the 26.5 GHz horn aperture is 1.9 cm, which defines the far-field boundary to be 6.2 cm at 26.5 GHz according to the Fraunhofer distance. As a result, we vary the Tx-Rx distance from 10 cm to 60 cm with a step size of 1 cm such that the far-field condition is satisfied. Fig. 11 presents the measured and modeled carrier power at 26.5 GHz with Tx-Rx distance varying from 10 cm to 60 cm in a NLoS link with an FPGA PCB board serving as a reflector. The absolute value of parameter β is estimated as 1.66, representing a waveguide type of channel. Moreover, it can be observed that

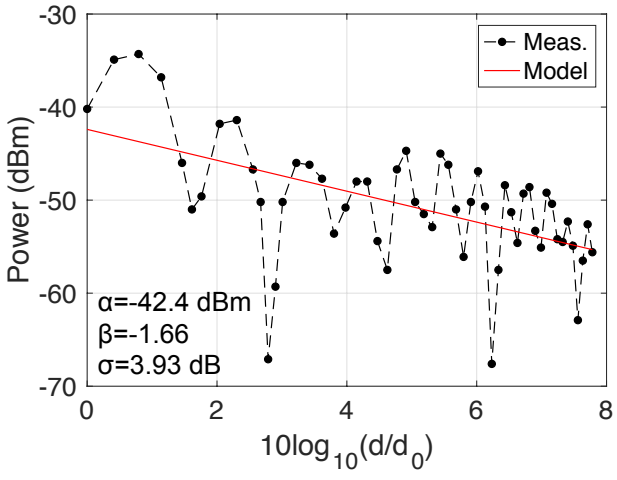


Fig. 11. Measured carrier power and modeled carrier power at 26.5 GHz with Tx-Rx distance varying from 10 cm to 60 cm.

the received carrier power experienced significant fluctuation (periodic peaks and dips) over distance. The lowest received power is observed as -67.1 dBm at a Tx-Rx distance of 19 cm, which is more than 20 dB below the modeled average value (red solid curve). We conclude that the fluctuation in the received carrier power is caused by the constructive and destructive interference from two reflected paths: 1) ground reflections and 2) reflections between components on the PCB, e.g., surface mount capacitors, resistors, switches, LEDs, I/O ports, buttons, etc. Given that the center of the 26.5 GHz horn antenna aperture is positioned at 6.5 cm above the ground plane with a beam width of 55°, a minimum path length around 30 cm is needed for the ground reflection to arrive at the Rx. Therefore, for Tx-Rx distance of 10 cm–30 cm, the constructive and destructive interference is mainly contributed from the multiple reflections between PCB board components, while at Tx-Rx distance beyond 30 cm, the sources of constructive and destructive interference are combinations of the ground reflections and the multiple reflections between PCB components. To quantify the fluctuation of the received carrier power at 26.5 GHz, we have analyzed the shadowing gain (X_σ) of the carrier power over distance and found that the X_σ follows log-normal distribution with its logarithmic equivalent having a zero-mean (in dB) and standard deviation (σ) of 3.93 dB. The cumulative distribution function (CDF) of the X_σ is presented in Fig. 12 to confirm the log-normality of the shadowing gain. Our empirical results show that for

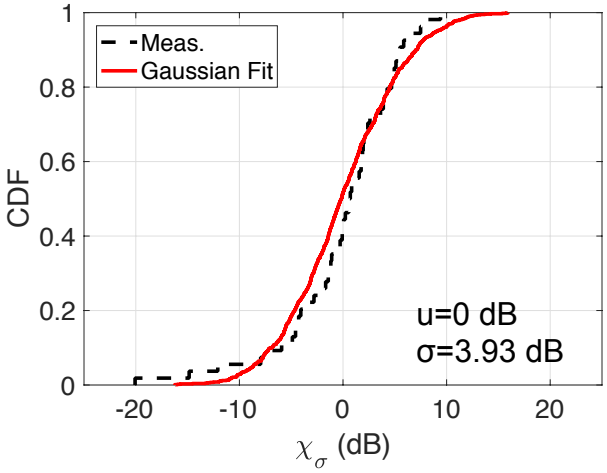


Fig. 12. CDF of the received carrier power's shadowing gain (X_σ) measured at 26.5 GHz at Tx-Rx distance of 10 cm–60 cm.

the millimeter-wave (26.5 GHz) chip-to-chip/board-to-board communication scenarios that rely on the NLoS type of link with PCB boards serving as reflectors, with Tx-Rx distance varying within a few wavelengths, the wireless link may experience communication dead zones where the received power drops by more than 20 dB from the average power level due to destructive interference from the reflections from the components on the PCB.

In the 300 GHz measurement, the same setup presented in Fig. 8 (b) is used. The largest physical dimension of the 300 GHz horn aperture is 4.6 mm, which defines the far-field boundary to be 4.23 cm at 300 GHz according to the Fraunhofer distance. To ensure the measurements are conducted in the far-field range, we vary the Tx-Rx distance from 8 cm to 24 cm with a step size of 1 cm such that the far-field condition is satisfied. Fig. 13 presents the measured and modeled carrier power at 300 GHz with Tx-Rx distance varying from 8 cm to 24 cm in a NLoS link with an FPGA PCB board serving as a reflector. The absolute value of parameter β is estimated as 2.07, indicating a free-space type of propagation. In contrast to the 26.5 GHz carrier power presented in Fig. 11, the 300 GHz carrier power experiences

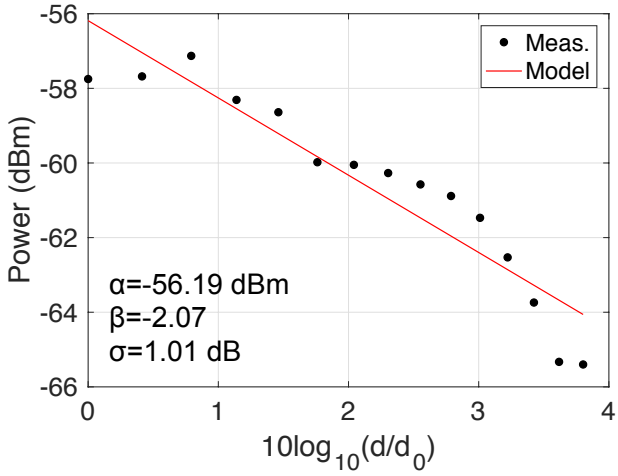


Fig. 13. Measured carrier power and modeled carrier power at 300 GHz with Tx-Rx distance varying from 8 cm to 24 cm.

much less fluctuation over distance, which shows that the constructive/destructive interference resulting from the ground reflection and the reflection between PCB components is less significant due to the narrower beam width (HPBW=10°) at 300 GHz. To quantify the fluctuation of the received carrier power at 300 GHz, we have analyzed the shadowing gain (X_σ) of the carrier power over distance and found that the X_σ follows log-normal distribution with its logarithmic equivalent having a zero-mean (in dB) and σ=1.01 dB. The CDF of the X_σ is presented in Fig. 14 to confirm the log-normality of the shadowing gain.

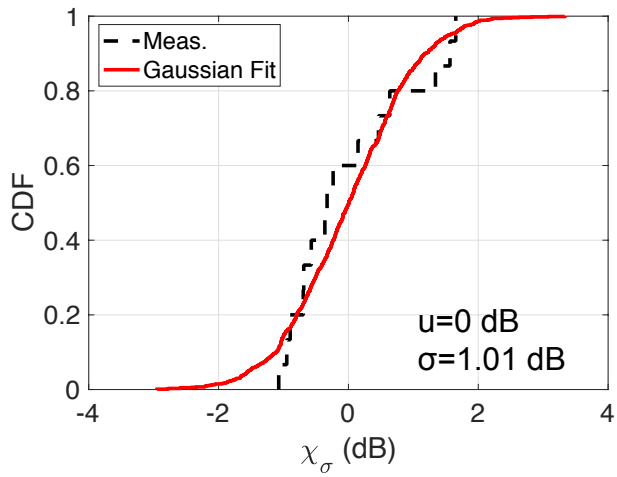


Fig. 14. CDF of the received carrier power's shadowing gain (X_σ) measured at 300 GHz at Tx-Rx distance of 8 cm–24 cm.

B. Backscattered Power Analysis

Next, we characterize the backscattered power by comparing the modeled backscattered power (using (1)) with measurements at 26.5 GHz and 300 GHz.

In the 26.5 GHz measurement, the same setup presented in Fig. 8 (a) is used. Measurements were recorded as Tx-Rx distance varies from 10 cm to 24 cm with a step size of 1 cm. The reason that the Tx-Rx distance stops at 24 cm is because the backscattered power decreased below noise floor at distance beyond 24 cm. Note that when using a lower interrogating frequency, the maximum distance can reach up to 2 m (demonstrated in [14]) due to lower pathloss. The tag's modulating frequency, f_m, is 900 kHz. It is assumed that there is no antenna polarization mismatch. Fig. 15 presents the measured and modeled backscattered power at 26.5 GHz with respect to logic utilization at Tx-Rx distances of 11 cm (black circle/solid line), 14 cm (red diamond/dash line), and 18 cm (blue triangle/dash-dot line). Results show a good agreement between the measured and modeled backscattered power. Fig. 16 presents the measured and modeled backscattered power at 26.5 GHz with Tx-Rx distance varying from 10 cm to 24 cm with logic utilization (%) of 100 % (black circle/solid line), 55 % (red diamond/dash line), and 15 % (blue triangle/dash-dot line). It can also be observed that the models have a good match with the measurements. Interestingly, in contrast to the measured carrier power in Fig. 11, the measured backscattered power does not have significant fluctuation as distance increases. We further characterize the shadowing gain (X_σ) of the backscattered power over distance and found that the X_σ follows log-normal distribution with its logarithmic equivalent having a zero-mean (in dB) and σ of 0.96 dB. CDF of the X_σ is presented in Fig. 17 to confirm the log-normality of the shadowing gain. Note that the 26.5 GHz backscatter link has a lower σ (0.96 dB) as compared to the 26.5 GHz carrier link (σ=3.93 dB). This is because the backscatter modulation is a result of the *relative amplitude change* in the carrier signal. While the absolute power level of the carrier signal experiences significant fluctuation as distance changes, the backscattered power is not affected by the fluctuation of the carrier power. Therefore, we conclude that the backscatter channel can provide a more reliable link that is resistant to the constructive and destructive interference from the multipaths as compared to the carrier channel.

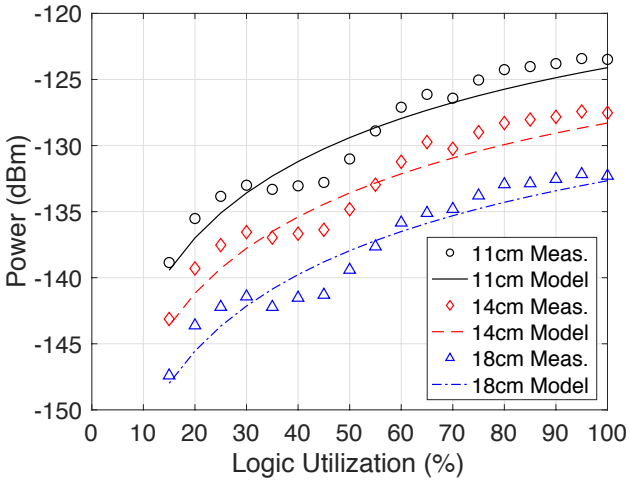


Fig. 15. Measured and modeled backscattered power at 26.5 GHz with respect to logic utilization (%) at Tx-Rx distances of 11 cm (black circle/solid line), 14 cm (red diamond/dash line), and 18 cm (blue triangle/dash-dot line).

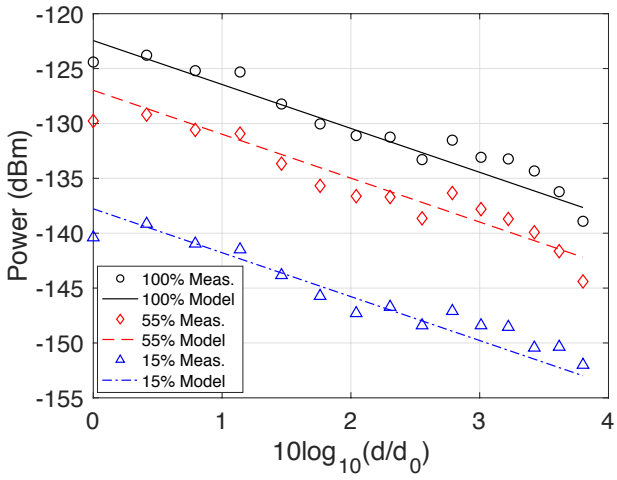


Fig. 16. Measured and modeled backscattered power at 26.5 GHz with Tx-Rx distance varying from 10 cm to 24 cm with logic utilization (%) of 100 % (black circle/solid line), 55 % (red diamond/dash line), and 15 % (blue triangle/dash-dot line).

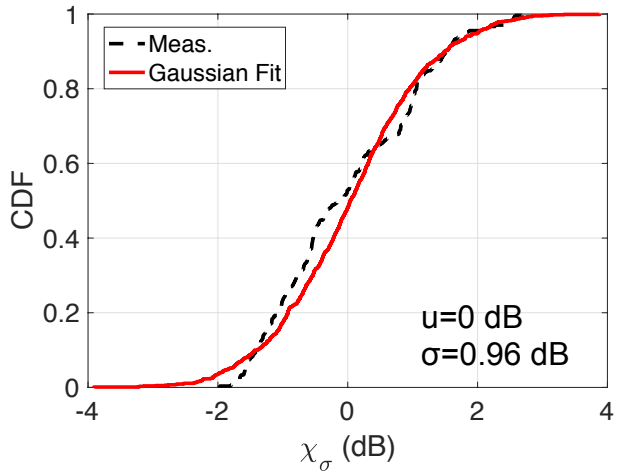


Fig. 17. CDF of the received backscattered power's shadowing gain (X_σ) measured at 26.5 GHz at Tx-Rx distance of 10 cm–24 cm.

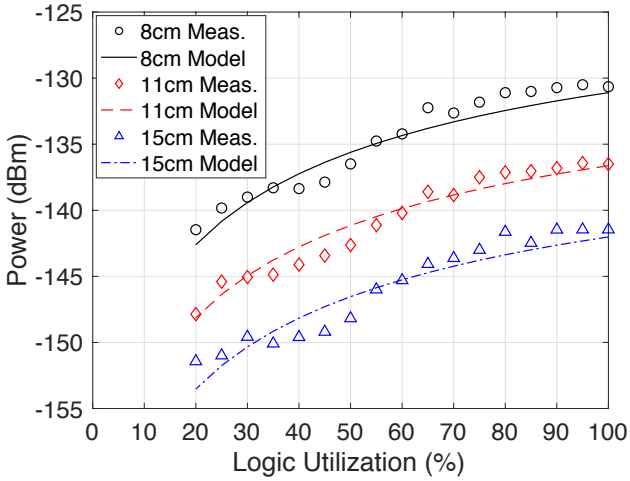


Fig. 18. Measured and modeled backscattered power at 300 GHz with respect to logic utilization (%) at Tx-Rx distances of 8 cm (black circle/solid line), 11 cm (red diamond/dash line), and 15 cm (blue triangle/dash-dot line).

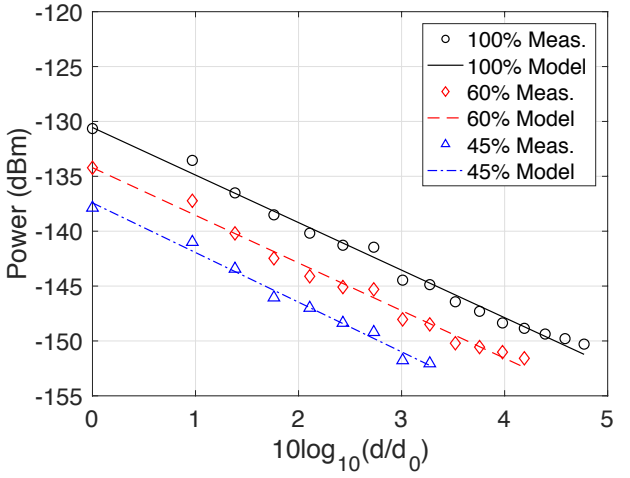


Fig. 19. Measured and modeled backscattered power at 300 GHz with Tx-Rx distance varying from 8 cm to 24 cm with logic utilization (%) of 100 % (black circle/solid line), 60 % (red diamond/dash line), and 45 % (blue triangle/dash-dot line).

In the 300 GHz measurement, the same setup presented in Fig. 8 (b) is used. Measurements were recorded as Tx-Rx distance varies from 8 cm to 24 cm with a step size of 1 cm. Fig. 18 presents the measured and modeled backscattered power at 300 GHz with respect to logic utilization at Tx-Rx distances of 8 cm (black circle/solid line), 11 cm (red diamond/dash line), and 15 cm (blue triangle/dash-dot line). Results show a good agreement between the measured and modeled backscattered power. Fig. 19 presents the measured and modeled backscattered power at 300 GHz with Tx-Rx distance varying from 8 cm to 24 cm with logic utilization (%) of 100 % (black circle/solid line), 60 % (red diamond/dash line), and 45 % (blue triangle/dash-dot line). It can also be observed that the models have a good match with the measurements. We further characterize the shadowing gain (X_σ) of the backscattered power over distance and found that the X_σ follows log-normal distribution with its logarithmic equivalent having a zero-mean (in dB) and σ of 0.52 dB. CDF of the X_σ is presented in Fig. 20 to confirm the log-normality of the shadowing gain. Following similar trend observed in the 26.5 GHz measurement, the 300 GHz backscatter link has a lower σ (0.52 dB) as compared to the 300 GHz carrier link (σ=1.01 dB).

VII. Conclusions

A circuit impedance model for the digital electronic-based RFID tag has been presented to explain the modulation mechanism of the backscatter radio generated by the switching transistors inside digital circuits and to describe the relation between the total input impedance and the logic resources of the digital circuits. The procedure of estimating digital circuits' impedance from SPICE model parameters has also been presented. Based on the proposed circuit impedance model, a

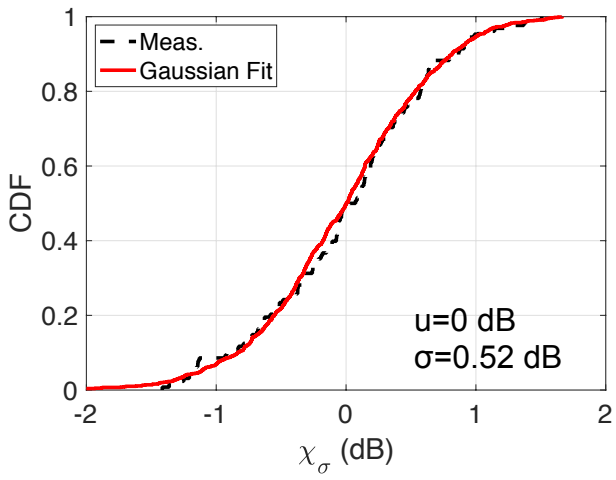


Fig. 20. CDF of the received backscattered power's shadowing gain (X_σ) measured at 300 GHz at Tx-Rx distance of 8 cm–24 cm.

modified modulation loss factor has been derived to estimate the modulation loss resulting from the switching activity of the digital electronics. Furthermore, propagation characterization of the carrier power and backscattered power is conducted at 26.5 GHz and 300 GHz. The shadowing gain for the carrier power and the backscattered power has been characterized as 3.93 dB and 0.96 dB at 26.5 GHz, and 1.01 dB and 0.52 dB at 300 GHz, respectively, showing that the backscatter channel can provide a more reliable link that is resistant to the constructive and destructive interference from the multipaths as compared to the carrier channel. A lower shadowing gain has been observed in the 300 GHz carrier/backscatter links as compared to the 26.5 GHz carrier/backscatter links due to the narrower beam width.

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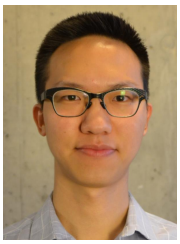

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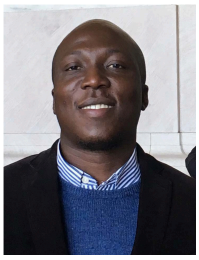

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