# Noise Optimization Techniques for Switched-Capacitor Based Neural Interfaces

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***Abstract*—This paper presents the noise optimization of a novel switched-capacitor (SC) based neural interface architecture, and its circuit demonstration in a 0.13 $\mu$m CMOS process. To reduce thermal noise folding ratio, and suppress $kT/C$ noise, several noise optimization techniques are developed in the proposed architecture. First, one parasitic capacitance suppression scheme is developed to block noise charge transfer from parasitic capacitors to amplifier output. Second, one recording path-splitting scheme is proposed in the input sampling stage to selectively record local field potentials (LFPs), extracellular spikes, or both for reducing input noise floor, and total power consumption. Third, an auto-zero noise cancellation scheme is developed to suppress $kT/C$ noise in the neural amplifier stage. A prototype neural interface chip was fabricated, and also verified in both bench-top, and *In-Vivo* experiments. Bench-top testings show the input-referred noise of the designed chip is 4.8 $\mu$V from 1 Hz to 300 Hz, and 2.3 $\mu$V from 300 Hz to 8 $kHz$ respectively, and *In-Vivo* experiments show the peak-to-peak amplitude of the total noise floor including neural activity, electrode interface noise, and the designed chip is only around 20 $\mu$V. In comparison with conventional architectures through both circuit measurement and animal experiments, it is well demonstrated that the proposed noise optimization techniques can effectively reduce circuit noise floor, thus extending the application range of switched-capacitor circuits.**

***Index Terms*—$kT/C$ noise cancellation, noise optimization techniques, neural interface, parasitic capacitance suppression, path-splitting scheme, switched-capacitor circuits.**

## I. Introduction

SWITCHED-CAPACITOR (SC) technique is widely used in mixed-signal circuits, such as low-noise amplifiers [1]–[5], low-distortion filters [6]–[10], and high-precision data converters [11]–[18]. However, when implementing such high-performance SC circuits, there is one serious problem that the thermal noise of the switched-on resistor will cause $kT/C$ noise after the switch is turned off, where $k$ is a Boltzmann constant, $T$ is the absolute temperature, and $C$ is the capacitance value. For example, when the capacitance value of $C$ is set to be 1 $pF$, 10 $pF$, and 100 $pF$, the $kT/C$ noise is 64.3 $\mu$V, 20.3 $\mu$V, and 6.4 $\mu$V, respectively. In general, SC circuits have higher noise floor compared to continuous-time (CT) counterparts. If some applications demand even lower input noise floor (around 2 $\mu$V), larger capacitance (about 1 $nF$) is needed in order to further reduce $kT/C$ noise, which will occupy additional circuit area and power consumption. As a result, trade-off considerations among low noise, circuit area, and power consumption cause SC circuits to be avoided in high-performance, miniaturized biomedical applications, especially implantable neural recording interfaces. To overcome the limitations at the cost of small circuit area and low power consumption, new noise optimization techniques are urgently demanded to improve circuit noise performance for SC circuit designs.

In [19], the noise generation of one conventional SC integrator was analyzed clearly by describing the noise model, undersampling, and noise folding of a broad-band noise source. Also, comparison results between theoretical calculation and circuit measurement were introduced to demonstrate the accuracy of the presented noise model. Therefore, useful design guidelines can be achieved from [19] when optimizing noise performance for SC circuits. As mentioned in [1], the conventional SC amplifier structure usually faces design trade-offs among settling accuracy, input noise, and total power consumption. High settling accuracy demands wide bandwidth and high power consumption, so this will be at the sacrifice of noise performance because settling accuracy is determined by averaged bandwidth during the whole amplification phase while the output noise of interest is only determined by sampling frequency and amplifier bandwidth near the end of the phase. To achieve good design trade-offs, [1] presented one noise reduction technique by adjusting the bandwidth of the SC amplifier, where the amplification phase is split into two sub-phases: the first sub-phase starts with wide bandwidth and high slew rate to achieve high setting accuracy while the amplifier bandwidth is significantly reduced during the second sub-phase to achieve much lower noise by reducing noise folding ratio. In [1], measurement results demonstrated that the designed amplifier with this bandwidth switching technique achieved 45% noise reduction. However, this technique is not an efficient method

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for $kT/C$ noise removal, especially when the capacitance is only tens of $fF$. Another thermal noise cancellation technique was presented in [20], where an unity-gain sample-and-hold amplifier was adopted to improve noise performance by 3.7−5.0 dB when the amplifier operates at a sampling frequency of 100−500 MHz. This method used one auxiliary path to sample the thermal noise of the main path and subtract the noise at the amplifier output. Nevertheless, the disadvantage is that this method will consume much additional circuit area and power consumption.

To make SC amplifier structures also suitable for neural recording applications, several thermal noise optimization techniques are presented in this study in order to achieve high input impedance, low input noise, and low power consumption for the proposed SC neural amplifier, named frequency-shaping amplifier (FSA). First, one parasitic capacitance suppression scheme is developed to block charge transfer from parasitic capacitors $C_p$ at the amplifier input terminal to a feedback capacitor $C_f$, which otherwise would increase the input noise floor of the designed amplifier. Second, one recording path-splitting scheme is proposed at the input sampling stage to selectively record local field potentials (LFPs), extracellular spikes, or both for reducing input noise floor and power consumption. Third, an auto-zero noise cancellation scheme is developed to effectively remove $kT/C$ noise that appears on $C_f$ after the reset switch is turned off. Fourth, both oversampling technique and chopper stabilization (CHS) technique are used to further reduce in-band noise floor.

As carefully discussed in our previous works [21]–[23], the proposed FSA can feature several advantages over the continuous-time neural amplifiers [24], [25]. First, the proposed FSA is not sensitive to both component mismatch and process variation, thus on-chip digital circuits can restore the original waveforms with low total phase and amplitude distortion. Second, because the loop gain of the proposed FSA is proportional to signal frequency $f$, so an embedded high-pass filter with a sub-Hz corner frequency ($1/(2\pi R_f C_f)$) is not demanded to reject electrode DC offset. As a result, the input capacitance in the FSA stage can be reduced according to those secondary constraints including capacitor mismatch, transistor leakage current, etc., which would increase the input impedance by several folds. Third, due to the use of the frequency-shaping technique, the FSA can compress the recorded neural data dynamic range by around 4.5-bit, thus relaxing the design requirement on system dynamic range. Fourth, with the help of wide system dynamic range and oversampling technique, the FSA can provide fast recovery from system saturation caused by stimulation or motion artifacts. In this work, we will focus on the noise analysis and optimization of the proposed FSA structure.

The rest of this paper is organized as follows. Section II gives a brief introduction on the conventional SC amplifier and proposed FSA. Section III presents the proposed thermal noise optimization techniques for low-noise SC neural recording interface designs. Section IV introduces the circuit measurement and *In-Vivo* experiments of the proposed frequency-shaping based neural interface. Section V gives the conclusion on this paper.

## II. Conventional Switched-Capacitor Amplifier and Proposed Frequency-Shaping Amplifier

In this section, the circuit implementation of both the conventional switched-capacitor amplifiier and the proposed FSA is fully differential, and the amplifiers are designed with one common mode feedback (CMFB) block to set their output common mode voltage $V_{ocm}= (V_{out+} + V_{out-})/2$ to the common mode voltage $V_{cm} = 0.5V_{DD}$ during the entire sampling period.

### A. Typical Switched-Capacitor Amplifier

Fig. 1 shows the circuit schematic and timing diagram of one typical SC amplifier, where $C_{in}$ is one input capacitor, $C_f$ is one feedback capacitor, $C_L$ is one load capacitor, $V_{in}$ is the input signal, $V_{out}$ is the output signal, $A(f)$ is the amplifier voltage gain, $T_s$ is the sampling period time, and $\phi_1$ and $\phi_2$ are two non-overlapped clock signals. Its basic operation is introduced as follows. During sampling phase $\phi_1$, the input signal $V_{in}$ is sampled on $C_{in}$ while the charge on $C_f$ is reset. During amplifying phase $\phi_2$, the charge on $C_{in}$ is transferred to $C_f$ and the amplifier output signal $V_{out}$ is sampled on $C_L$. The loop transfer function of this SC amplifier in $z$-domain is $|(C_{in}/C_f)z^{-0.5}|$.

To better understand the noise generation of SC circuits over the signal baseband, we will discuss the noise aliasing of several basic components derived from the typical SC amplifier. Fig. 2(a) shows one simple signal sampling circuit block that consists of one input capacitor $C_{in}$ and one switch. When the switch is turned on, the $-3$ dB corner frequency $f_{3\,dB}$ of this component is $1/(2\pi R_{on}C_{in})$, where $R_{on}$ is the switched-on resistance of the switch. To make sure that this component can achieve high-accuracy signal settling before the switch is turned off, $f_{3\,dB}$ is usually set to be several times higher than the sampling frequency $f_s$. As a result, the switched-on resistor thermal noise ($V_R^2(f) = 4kTR_{on}$) will be folded back to the signal baseband when the switch is turned off, and the folding ratio is bounded at $0.5\pi f_{3\,dB}/f_s$, where $0.5\pi$ is obtained from $\int 1/(1 + f^2/f_{3\,dB}^2)df$ [21]. According to the power spectrum density (PSD) illustration of this component in Fig. 2(a) (before and after noise folding), its final noise power density $S_a$ on $C_{in}$ is given as

$$S_a(f) = \frac{0.5\pi f_{3\,dB}}{f_s} 4kTR_{on} = \frac{kT}{C_{in} f_s}. \tag{1}$$

Fig. 2(b) presents one charge resetting circuit component during phase $\phi_1$, which includes one feedback capacitor $C_f$, one load capacitor $C_L$, one switch, and one amplifier. In this component, three primary noise sources (switched-on resistor thermal noise $V_R$, amplifier equivalent thermal noise $V_{eq}$, and amplifier flicker noise $V_{1/f}$) need to be considered when calculating the total output noise, where $V_{eq}^2(f) \approx 8\gamma kT/g_m$, $V_{1/f}^2(f) = K/(C_{ox}WLf)$, coefficient $\gamma$ is $2/3$ for long-channel transistors and greater than 1 for short-channel transistors, $g_m$ is the amplifier input-pair transconductance, $K$ is a process-dependent constant, $C_{ox}$ is the oxide capacitance in MOSFET transistors, and $W$ and $L$ are the transistor channel width and length, respectively. From the PSD distribution in Fig. 2(b), it

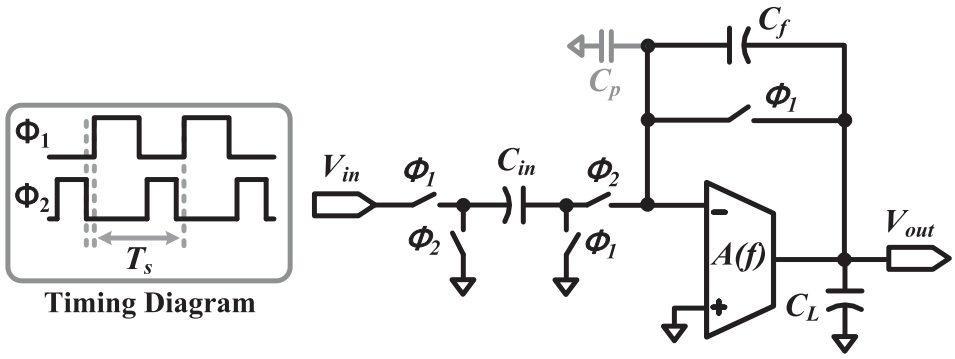


Fig. 1. Circuit schematic and timing diagram of one typical switched-capacitor amplifier, where $C_{in}$ is one input capacitor, $C_f$ is one feedback capacitor, $C_L$ is one load capacitor, $C_p$ is one parasitic capacitor at the amplifier input terminal, $V_{in}$ is the input signal, $V_{out}$ is the output signal, $A(f)$ is the amplifier voltage gain, $T_s$ is the sampling period time, and $\phi_1$ and $\phi_2$ are two non-overlapped clock signals.

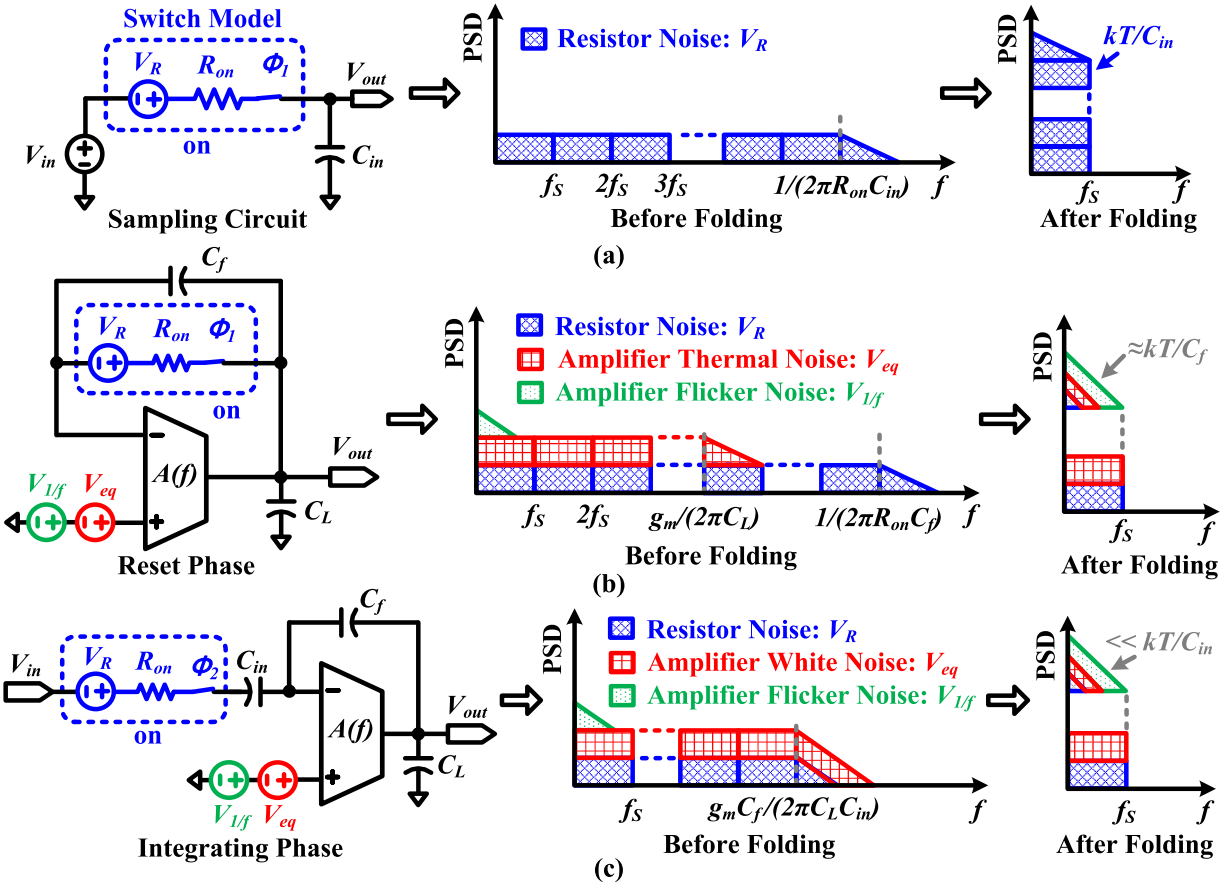


Fig. 2. Noise analysis and aliasing illustration of several basic components in switched-capacitor circuits, where $V_{1/f}$ is the amplifier flicker noise, $V_{eq}$ is the amplifier equivalent thermal noise, $V_R$ is the switched-on resistor thermal noise, $R_{on}$ is the switched-on resistor, $g_m$ is the amplifier input-pair transconductance, $f$ is the signal frequency, $f_s$ is the sampling frequency, and PSD is the power spectrum density. (a) Simple signal sampling circuit consisting of one switch and one capacitor. (b) Charge reset circuit during reset phase. (c) Signal amplifying circuit during integrating phase.

is known that $V_{1/f}$ is a narrow-band noise source while both $V_R$ and $V_{eq}$ are broad-band thermal noise sources, and the $f_{3\,dB}$ of $V_R$ and $V_{eq}$ is $1/(2\pi R_{on}C_f)$ and $g_m/(2\pi C_L)$, respectively. Also, sources $V_{eq}$ and $V_{1/f}$ will not be accumulated on $C_f$ because there is no current path across $C_f$ from amplifier output and one terminal of $C_f$ is connected to virtual ground. Therefore, when the reset switch is turned off, the final noise power density $S_b$ on $C_L$ of this component is

$$S_b(f) \approx \frac{1}{4f_s}\left(\frac{1}{R_{on}C_f}4kTR_{on} + \frac{g_m}{C_L}\frac{8\gamma kT}{g_m}\right) + V_{1/f}^2 \approx \frac{kT}{C_f f_s} + \frac{2\gamma kT}{C_L f_s} + V_{1/f}^2. \quad (2)$$

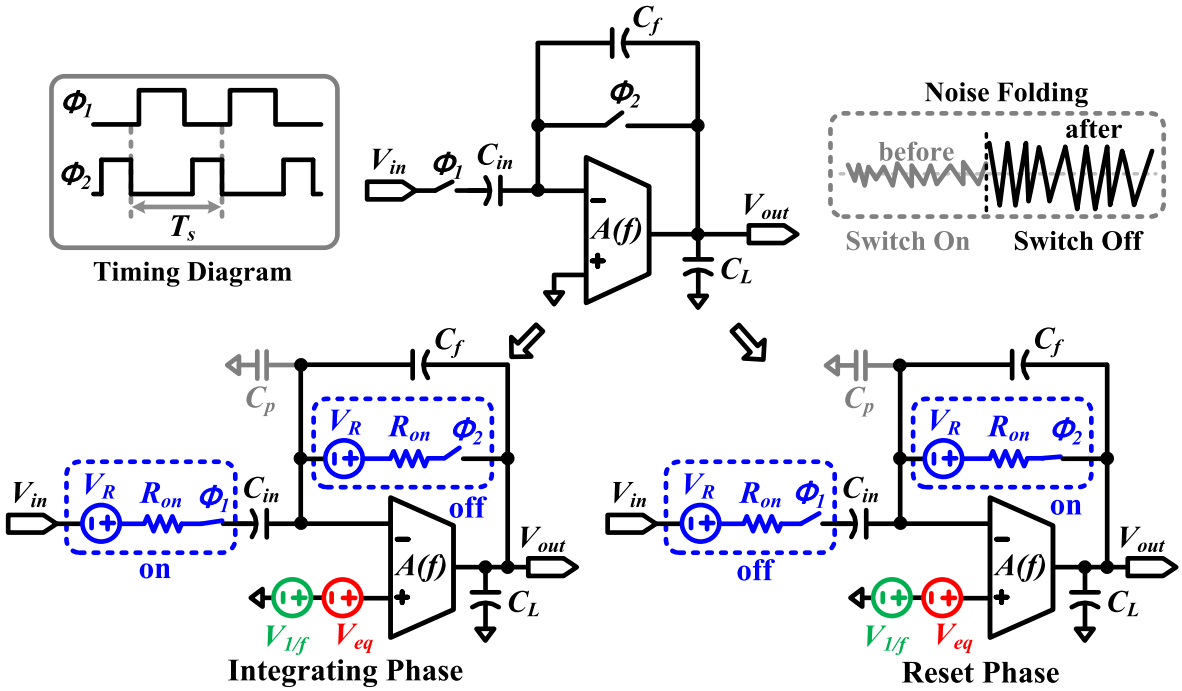


Fig. 3. Proposed switched-capacitor based neural amplifier structure, timing diagram, and simplified noise mode during integrating phase $\phi_1$ and reset phase $\phi_2$.

Fig. 2(c) gives one signal amplifying circuit component during $\phi_2$. It includes three capacitors ($C_{in}$, $C_f$ and $C_L$), one switch, and one amplifier. Based on the PSD distribution as shown in Fig. 2(c), it is found that the $f_{3\,dB}$ of this component is further reduced to $g_m C_f/(2\pi C_L C_{in})$. After considering the noise folding as shown in Fig. 2(c), the final noise power density $S_c$ on $C_L$ is calculated as

$$\begin{aligned} S_c(f) &\approx \frac{g_m}{4\beta C_L f_s}\left[\beta^2 4kTR_{on} + (1+\beta)^2\frac{8\gamma kT}{g_m}\right] \\ &\quad + (1+\beta)^2 \tilde{} V_{1/f}^2 \\ &= \frac{kT}{C_L f_s}\frac{1}{\beta}\left[R_{on}g_m\beta^2 + 2\gamma(1+\beta)^2\right] \\ &\quad + (1+\beta)^2 \tilde{} V_{1/f}^2, \end{aligned} \tag{3}$$

where $\beta$ is the capacitor ratio of $C_{in}/C_f$.

In this design, CHS technique [26] is used to remove the majority of flicker noise and further optimize noise performance of SC circuits. Thus, the input-referred noise of two basic circuit components as shown in Fig. 2(b) and (c) are modified as

$$S_{b,in}(f) \approx \frac{kT}{C_f f_s} + \frac{2\gamma kT}{C_L f_s}, \tag{4}$$

$$S_{c,in}(f) \approx \frac{kT}{C_L f_s}\frac{1}{\beta}\left[R_{on}g_m + 2\gamma\left(1+\frac{1}{\beta}\right)^2\right]. \tag{5}$$

Equation (4) shows that the input noise of the circuit component in Fig. 2(b) is slightly larger than the summation of $kT/C_f$ and $kT/C_L$ noise. Also, as shown in (5), the input noise of the circuit component in Fig. 2(c) is approximate to $2\gamma kT/(\beta C_L)$ when $\beta > 10$, and its input noise floor is not related to input capacitor $C_{in}$ but mostly depends on the value of $f_s$, $C_L$, and $\beta$. To simultaneously achieve low input noise, low power consumption, and high input impedance for SC based neural interfaces, the circuit schematic in Fig. 2(c) is preferred with large $f_s$ and $\beta$, and the value of $C_L$ is also chosen to be similar to $C_{in}$.

After considering the parasitic capacitor $C_p$ as shown in Fig. 1, the input-referred noise of the typical SC amplifier can be calculated as

$$\begin{aligned} S_{in} &\approx \frac{kT}{C_{in}f_s} + \frac{1}{\beta^2}\left[\frac{kT}{C_f f_s} + \frac{2\gamma kT}{C_L f_s}\right] \\ &\quad + \frac{2kT}{C_L f_s}\frac{1}{\beta}\left[R_{on}g_m + \gamma\left(1+\frac{1}{\beta}+\frac{C_p}{C_{in}}\right)^2\right], \end{aligned} \tag{6}$$

where the input noise of the typical amplifier mostly depends on $kT/C_{in}$ when $\beta \gg 10$, and the effect of the capacitance in the typical amplifier can be ignored when the capacitance ratio of $(C_{in}/C_p)$ is larger than 10.

### *B. Proposed Frequency-Shaping Amplifier*

After the noise analysis of several basic components in Section II.A, Fig. 3 proposes one novel SC based neural amplifier structure, namely FSA. The basic operation is introduced as follows. During amplifying phase $\phi_1$, the input signal $V_{in}$ and circuit noise ($V_R$, $V_{eq}$, and $V_{1/f}$) are sampled on $C_{in}$, and the amount of charge transferred to $C_f$ is proportional to the change of the input signal and sampled noise. During reset phase $\phi_2$, $C_f$ is shorted while the charge on $C_{in}$ remains. Assuming the signal frequency $f$ is much lower than the sampling frequency $f_s$, the closed-loop gain $A_{CL}$ of the proposed FSA in $z$-domain

is

$$A_{CL} = \left| -\frac{C_{in}}{C_f}(1 - z^{-1}) \right| \approx \frac{2\pi f}{f_s}\frac{C_{in}}{C_f} \approx \frac{2\pi\beta f}{f_s}. \quad (7)$$

As shown in (7), the closed-loop gain of the proposed FSA is near zero at ultra-low frequencies ($< 0.1$ Hz). Consequently, the proposed FSA can inherently suppress electrode DC offset without needing a sub-1 Hz high-pass filter. Also, our previous works [21]–[23] have demonstrated that the FSA core could increase input impedance, extend system dynamic range, and simultaneously acquire LFPs, extracellular spikes, power line noise interference, and motion artifacts. In this work, we will discuss how to further optimize the input noise performance of the FSA core and also develop one SC based amplifier structure that is suitable for low noise neural recording.

In mixed-signal circuit designs, thermal noise accumulated on a capacitor is the product of the Boltzmann constant $k$ and the absolute temperature $T$ divided by the capacitance value $C$, referred as $kT/C$ noise. If $kT/C$ noise appears in the SC circuits, a direct trade-off between input noise and input sampling capacitance would prohibit impedance improvement. For example, assuming $C_{in} = 1\ pF$ in Fig. 2(a), the input-referred $kT/C$ noise is 64 $\mu$V, which is too high to accurately acquire neural activity. To suppress $kT/C$ noise, Fig. 2(c) inserts an amplifier to the sampling path, where $C_{in}$ is disconnected from the ground and the frequency span of the sampled noise on $C_{in}$ is confined to that of the amplifier. As a result, the reduction of $C_{in}$ will not compromise the input noise floor when the capacitor ratio of $C_{in}/C_f$ is not changed, which has been verified in (5).

As shown in Fig. 3, it is found that the proposed FSA core is periodically switched between two phases: it acts as a typical amplifier (Fig. 2(c)) with a loop gain equal to $C_{in}/C_f$ during $\phi_1$ and an unity-gain buffer (Fig. 2(b)) during $\phi_2$. Therefore, before the switch is turned off, the unsampled output noise floor of the proposed FSA core during $\phi_1$ ($S_{un1}$) and $\phi_2$ ($S_{un2}$) is given as

$$S_{un1} \approx \left[\beta^2 4kTR_{on} + (1+\beta)^2\frac{8\gamma kT}{g_m}\right]\frac{1}{1+f^2/f_{3\,dB}^2} + (1+\beta)^2 V_{1/f}^2\frac{1}{1+f^2/f_{3\,dB}^2}, \quad (8)$$

$$S_{un2} \approx 4kTR_{on}\frac{1}{1+f^2/f_{3\,dB,R}^2} + \frac{8\gamma kT}{g_m}\frac{1}{1+f^2/f_u^2} + V_{1/f}^2\frac{1}{1+f^2/f_u^2}, \quad (9)$$

where $f_{3\,dB} = f_u/\beta$, $f_u = g_m/(2\pi C_L)$ is the unity-gain bandwidth of an amplifier, $f_{3\,dB,R} = 1/(2\pi R_{on}C_f)$. The $-3$ dB bandwidth of the proposed FSA core during $\phi_1$ and $\phi_2$ is set by $f_{3\,dB}$ and $f_u$, respectively. As mentioned in Section II, $f_{3\,dB}$ or $f_u$ is usually chosen to be a few times larger than $f_s$ to achieve high-accuracy signal setting. Also, according to Nyquist theorem, broad-band noise will be aliased to signal baseband when the switch is turned off, thus increasing the noise floor. For the primary noise sources as shown in Fig. 3, $V_{1/f}$ is narrow-band noise while both $V_R$ and $V_{eq}$ are broad-band noise.

During $\phi_1$, the FSA core is configured with a loop gain of $\beta$ and the broad-band noise starts to attenuate at $f_{3\,dB}$. Also, an inverse transform of noise spectrum shows that the broad-band noise will fold by a ratio of $0.5\pi f_{3\,dB}/f_s$ when the switch is turned off. During $\phi_2$, the FSA core is in its unity-gain configuration and the $-3$ dB frequency core of the broad-band noise is extended to $f_u$ or $f_{3\,dB,R}$. Consequently, during $\phi_2$, the amplifier equivalent thermal noise $V_{eq}$ and switch-on resistor thermal noise $V_R$ will be folded by $0.5\pi\beta f_{3\,dB}/f_s$ times and $0.5\pi f_{3\,dB,R}/f_s$ times, respectively. To calculate the total noise power, we tentatively assume there is no noise accumulation in the previous cycles. Modified from (8) and (9), the sampled-and-hold output noise during $\phi_1$ ($S_{sn1}$) and $\phi_2$ ($S_{sn2}$) are given as

$$S_{sn1} \approx \left[\beta^2 R_{on} + (1+\beta)^2\frac{2\gamma}{g_m}\right]\frac{2\pi kTf_{3\,dB}}{f_s} + (1+\beta)^2 V_{1/f}^2, \quad (10)$$

$$S_{sn2} \approx \frac{kT}{C_f f_s} + \frac{2\gamma}{g_m}\frac{2\pi\beta kTf_{3\,dB}}{f_s} + V_{1/f}^2. \quad (11)$$

After using the CHS technique in the FSA stage, (10) and (11) are revised as

$$S_{sn1} \approx \left[\beta^2 R_{on} + (1+\beta)^2\frac{2\gamma}{g_m}\right]\frac{2\pi kTf_{3\,dB}}{f_s}, \quad (12)$$

$$S_{sn2} \approx \frac{kT}{C_f f_s} + \frac{2\gamma}{g_m}\frac{2\pi\beta kTf_{3\,dB}}{f_s}. \quad (13)$$

Fig. 3 shows that $C_{in}$ is always connected to a virtual ground and the charge on $C_{in}$ is never reset. As a result, the sampled-and-hold output noise during $\phi_1$ will be accumulated based on the transfer function of $A_{CL} \approx 2\pi\beta f/f_s$, while the sampled-and-hold output noise during $\phi_2$ will not be accumulated since the charge on $C_f$ is periodically reset. Therefore, the accumulated output noise during $\phi_1$ ($S_{sn1}$) is rewritten as

$$S_{sn1} \approx \left[A_{CL}^2 R_{on} + (1+A_{CL})^2\frac{2\gamma}{g_m}\right]\frac{2\pi kTf_{3\,dB}}{f_s}, \quad (14)$$

while the accumulated output noise during $\phi_2$ ($S_{sn2}$) remains unchanged.

The total amount of the accumulated noise $S_{in}$ that appears at the input of the FSA stage is the sum of $S_{sn1}$ and $S_{sn2}$, and it can be calculated as

$$S_{in} \approx (R_{on}g_m + 2\gamma)\frac{kTC_f}{C_L C_{in} f_s} + \left[\frac{2\gamma kT}{C_L f_s}\left(1 + \frac{C_f}{C_{in}}\right) + \frac{kT}{C_f f_s}\right]\left(\frac{C_f f_s}{2\pi C_{in} f}\right)^2 + \frac{2\gamma kT}{\pi C_L f}\left(\frac{C_f}{C_{in}}\right)^2, \quad (15)$$

where the total input noise of the FSA core includes three parts: first, $(R_{on}g_m + 2\gamma)kTC_f/(C_L C_{in} f_s)$ is the thermal noise that is independent to signal frequency $f$; second, $[2\gamma kT(1 + C_f/C_{in})/(C_L f_s) + kT/(C_f f_s)][C_f f_s/(2\pi C_{in} f)]^2$ is inversely proportional to $f^2$; third, $2\gamma kT(C_f/C_{in})^2/(\pi C_L f)$ is

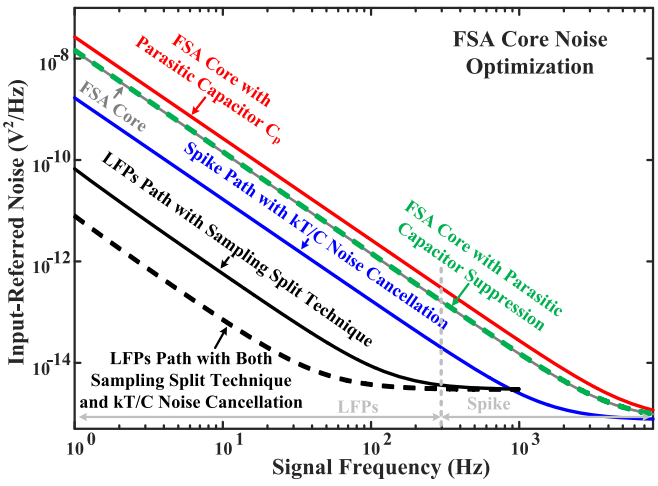


Fig. 4. Simulated input-referred noise of the FSA core with noise optimization techniques in Simulink. The gray curve is the input noise of FSA core as shown in Fig. 3 without considering the parasitic capacitor $C_p$ at the amplifier input terminal. After considering $C_p$, the red curve and the green dotted line curve show the input noise of the FSA core with $C_p$ and with parasitic capacitance suppression, respectively. After using $kT/C$ noise cancellation, the input noise is reduced as shown in the blue curve. For LFPs path, the input noise with sampling split technique is given in the black curve while the black dotted line curve gives the optimized input noise with both sampling split technique and $kT/C$ noise cancellation.

also inversely proportional to $f$. Fig. 4 (gray curve) shows the simulated input-referred noise of the FSA core, where $R_{on} = 2\ k\Omega,\ g_m = 50\ \mu S,\ \gamma = 2/3,\ k = 1.38 * 10^{-23},\ T = 300\ K,\ C_{in} = 3\ pF,\ C_f = 30\ fF,\ C_L = 2\ pF$, and $f_s = 40\ kHz$. From the gray curve, it is seen that the input-referred noise of the FSA core is high at low frequencies due to small gain at low frequencies ($< 100$ Hz) and large $kT/C$ noise on $C_f$. Therefore, several circuit techniques will be presented to optimize the noise performance for the FSA core.

After considering the parasitic capacitor $C_p$ as shown in Fig. 3, the input-referred noise of the FSA core is rewritten as

$$S_{in} \approx (R_{on}g_m + 2\gamma)\frac{kTC_f}{C_LC_{in}f_s} + \left[\frac{2\gamma kT}{C_Lf_s}\left(1+\frac{C_f}{C_{in}}\right)+\frac{kT}{C_ff_s}\right]\left(\frac{C_ff_s}{2\pi C_{in}f}\right)^2 + \frac{2\gamma kT}{\pi C_Lf}\left(\frac{C_f}{C_{in}}\right)^2 + \frac{2\gamma kT}{C_Lf_s}\left(\frac{C_p}{C_f}\right)^2\left(\frac{C_ff_s}{2\pi C_{in}f}\right)^2, \quad (16)$$

where the effect of the parasitic capacitance cannot be neglected because $[2\gamma kT/(C_Lf_s)](C_p/C_f)^2[C_ff_s/(2\pi C_{in}f)]^2$ is inversely proportional to $f^2$ and the value of $C_p$ is larger than $C_f$.

## III. Proposed Noise Optimization Techniques

According to the noise analysis in Section II, several noise optimization techniques will be developed in this section to reduce thermal noise folding ratio and also suppress $kT/C$ noise on $C_f$.

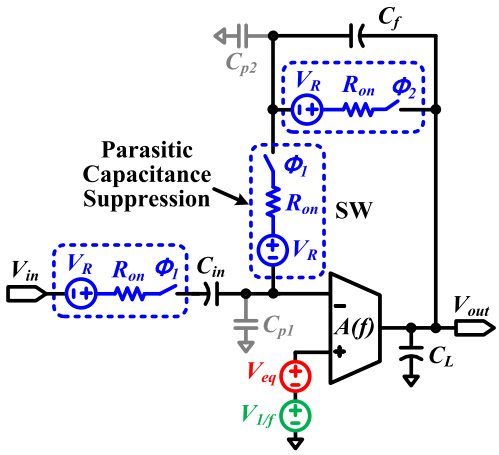


Fig. 5. Circuit schematic of one parasitic capacitance suppression scheme, where a series switch SW controlled by $\phi_1$ is added in the FSA stage to block noise transfer from a parasitic capacitor $C_{p1}$ to amplifier output, and $C_{p2}$ is another parasitic capacitor.

### A. Parasitic Capacitance Suppression

Post-layout simulation shows that the value of $C_p$ at the amplifier input terminal is several hundreds of $fF$, and (16) demonstrates that large parasitic capacitor $C_p$ will degrade noise performance. Fig. 4 (red curve) gives the simulated input-referred noise of the FSA core when $C_p$ is set to be 200 $fF$. To suppress the effect of the parasitic capacitors, Fig. 5 presents one efficient parasitic capacitance suppression scheme, where a series switch SW controlled by $\phi_1$ is added in the FSA stage to block noise charge transfer from the parasitic capacitor $C_{p1}$ to $C_f$. Therefore, the input noise as shown in (16) is modified as

$$S_{in} \approx \left[R_{on}g_m + 2\gamma + 2\gamma\left(\frac{C_{p1}}{C_{in}}\right)^2\right]\frac{kTC_f}{C_LC_{in}f_s} + \left(\frac{2\gamma kTC_f}{C_LC_{in}f_s}+\frac{kT}{C_ff_s}\right)\left(\frac{C_ff_s}{2\pi C_{in}f}\right)^2 + \frac{2\gamma kT}{\pi C_Lf}\left(\frac{C_f}{C_{in}}\right)^2 + \frac{2\gamma kT}{C_Lf_s}\left(\frac{C_{p2}}{C_f}\right)^2\left(\frac{C_ff_s}{2\pi C_{in}f}\right)^2, \quad (17)$$

where the parasitic capacitance effect can be ignored when $C_{p1}$ and $C_{p2}$ are small enough in comparison with $C_{in}$ and $C_f$.

In Fig. 5, $C_{p1}$ occupies most of parasitic capacitance at the amplifier input terminal and the value of $C_{p2}$ is only tens of $fF$. Fig. 4 (green dotted line curve) shows the simulated input-referred noise of the modified FSA with the proposed parasitic capacitance suppression scheme, where $C_{p1}$ and $C_{p2}$ are chosen to be 170 $fF$ and 30 $fF$, respectively. Simulation results demonstrate that the proposed suppression scheme can efficiently block noise charge transfer from parasitic capacitors to amplifier output. Also, to further reduce $C_{p1}$ and $C_{p2}$, all the switches are designed with small size. In this design, two methods have been used to reduce charge injection and harmonic distortion. First, dummy transistors are added at the both sides of the small switches at the FSA stage. Second, the circuit

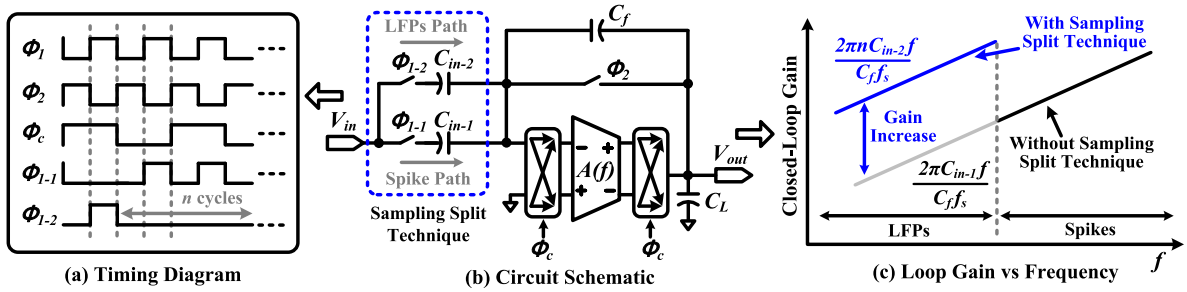


Fig. 6. Proposed recording path splitting scheme for low frequency noise optimization. (a) Timing diagram, where $\phi_{1-1}$ and $\phi_{1-2}$ are two sampling clock signals derived from $\phi_1$ ($\phi_{1-1} \cup \phi_{1-2} = \phi_1$, $\phi_{1-1} \cap \phi_{1-2} = 0$), $\phi_c$ is one clock signal for CHS technique. (b) Circuit schematic with sampling split technique. $C_{in-1}$ and $C_{in-2}$ are two input sampling capacitors. (c) Closed-loop gain vs. frequency. The closed-loop gain of the LFPs path is $2\pi n C_{in-2} f/(C_f f_s)$ while that of the spike path is $2\pi C_{in-1} f/(C_f f_s)$.

implementation of the proposed FSA is fully differential, and the switches at the main signal transfer loop are controlled by some delayed clock signals to suppress the charge injection associated with the input signal $V_{in}$.

### B. Recording Path Splitting

To selectively acquire LFPs, extracellular spikes, or both with low noise floor and low power consumption, a new path-splitting technique has been developed in Fig. 6, where input data are split into two data streams (LFPs path and spike path) with different loop gains set by two capacitor ratios ($C_{in-1}/C_f$ and $C_{in-2}/C_f$) and two clock signals as shown in Fig. 6(a) ($\phi_{1-1}$ and $\phi_{1-2}$, $\phi_1 = \phi_{1-1} \cup \phi_{1-2}$, $\phi_{1-1} \cap \phi_{1-2} = 0$). In this circuit implementation, the frequency of $\phi_{1-2}$ is set to be $f_s/n$ ($n \geq 2$) for sampling LFPs while that of $\phi_{1-1}$ is approximately $f_s$ for recording extracellular spikes. After the FSA stage, the sampled data from both paths are combined together and transferred to the gain stage for total loop gain adjustment and to the analog-to-digital converter (ADC) stage for signal digitization. After that, on-chip digital circuits capture the digitized data based on $\phi_{1-2}$, where $n-1$ out of every $n$ samples are used for reconstructing spikes and the single remaining sample is adopted for restoring LFPs. As the FSA stage oversamples neural spikes several times, a periodically missing sample can be recovered with low distortion ($<-60$ dB in measurement). Also, the CHS technique controlled by $\phi_c$ is employed in the FSA stage to remove amplifier flicker noise, and the frequency of $\phi_c$ is chosen to be $f_s/2$ in this work.

As shown in Fig. 6(c), assuming $C_{in-1} = C_{in-2} = C_{in}$, the closed-loop gain $A_{CL}$ of the spike recording path is still $2\pi\beta f/f_s$ while that of the LFPs recording path is increased to $2\pi n\beta f/f_s$. As a result, the input-referred noise for the spike path is still similar to (15) while that of the LFPs path is given as

$$S_{in} \approx (R_{on} g_m + 2\gamma)\frac{nkTC_f}{C_L C_{in} f_s} + \left[\frac{2\gamma nkT}{C_L f_s}\left(1+\frac{C_f}{C_{in}}\right)+\frac{nkT}{C_f f_s}\right]\left(\frac{C_f f_s}{2\pi n C_{in} f}\right)^2 + \frac{2\gamma kT}{\pi C_L f}\left(\frac{C_f}{C_{in}}\right)^2, \quad (18)$$

where the noise floor at low frequencies($<100$ Hz) is approximately reduced by $n$-fold in comparison with (15).

Fig. 4 (black curve) gives the simulated input-referred noise of the LFPs path with the proposed sampling split technique ($n = 16$). Compared to the FSA core, the input noise floor from several Hz to 300 Hz is greatly reduced after using the proposed technique. Besides, although the path-splitting technique can increase the loop gain of the LFPs path, the proposed neural interface can still effectively suppress electrode DC offset. For example, assume $C_{in-1} = C_{in-2} = C_{in} = 3$ pF, $C_f = 30$ fF, $f_s = 40$ kHz, and $n = 16$, the loop gain of the LFPs path is $0.08\,\pi f$, which corresponds to 0.025 V/V at 0.1 Hz, 0.125 V/V at 0.5 Hz, and 0.25 V/V at 1 Hz, respectively.

### C. Auto-Zero $kT/C$ Noise Cancellation

According to the circuit operation in Fig. 3, the switch-on resistor $R_{on}$ only brings in the sampled noise on $C_f$ from $\phi_2$ to $\phi_1$. Because $R_{on}$ and $C_f$ together form a loop without passing through the amplifier, the appeared noise is quite large ($kT/C_f$) and added to the signal output during $\phi_1$. In order to make the FSA core have competitive noise performance, it demands to remove the $kT/C$ noise on $C_f$, which is seemingly a formidable task at first glance. However, the $kT/C$ noise on $C_f$ always appears at the clock transition edge from $\phi_2$ to $\phi_1$ and remains constant during $\phi_1$. Therefore, the $kT/C$ noise on $C_f$ is uncorrelated with the signal transfer and it becomes possible to remove this noise. In this design, to suppress the $kT/C$ noise on $C_f$ for further input noise reduction, a new delayed-signaling noise cancellation scheme based on an auto-zero technique is developed in Fig. 7 to sample the appeared $kT/C$ noise and subtract the noise in the subsequent stage. To fully remove the $kT/C$ noise on $C_f$, the falling edge of $\phi_3$ as shown in Fig. 7 is designed to be slightly earlier than $\phi_2$. The operation principle of the proposed noise cancellation scheme is shown in Fig. 8 with three steps: first, during $\phi_3$, the charge on $C_f$, $C_1$, and $C_3$ are reset, and the FSA output before noise aliasing is sampled on $C_2$; second, when $\phi_3$ is low and $\phi_2$ is still high, the $kT/C$ noise on $C_f$ is sampled on $C_2$ while the charge on both $C_1$ and $C_3$ are still reset; third, during $\Phi_1$, the proposed FSA output data including the recorded signals and $kT/C$ noise on $C_f$ are sent to the subsequent stage with a negative gain

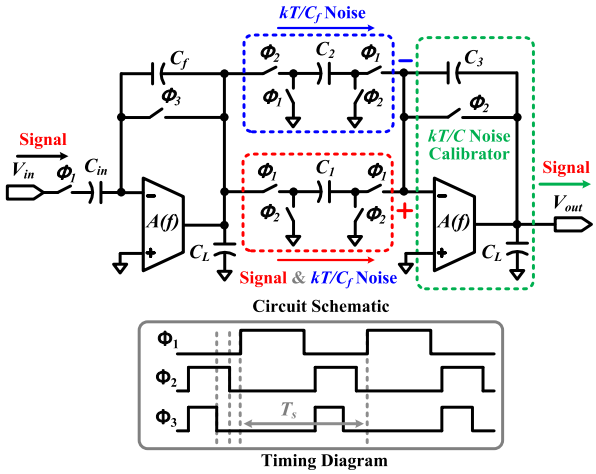


Fig. 7. Circuit schematic and timing diagram of the proposed auto-zero $kT/C$ noise cancellation. $\phi_3$ is another sampling clock signal and its falling edge is designed to be a little earlier than $\phi_2$. $C_1$, $C_2$, and $C_3$ are three capacitors used in the subsequent stage.

of $-C_1/C_3$ while the previous $kT/C$ noise sampled on $C_2$ is simultaneously processed by the subsequent stage with a positive gain of $C_2/C_3$. Assuming $C_1 = C_2$, the proposed technique can eliminate the $kT/C$ noise on $C_f$ to further improve noise performance. Therefore, (15) and (18) are modified as

$$S_{in} \approx (R_{on}g_m + 2\gamma)\frac{kTC_f}{C_L C_{in} f_s} + \left[\frac{2\gamma kT}{C_L f_s}\left(1+\frac{C_f}{C_{in}}\right) + (1-\alpha)\frac{kT}{C_f f_s}\right]\left(\frac{C_f f_s}{2\pi C_{in} f}\right)^2 + \frac{2\gamma kT}{\pi C_L f}\left(\frac{C_f}{C_{in}}\right)^2, \quad (19)$$

$$S_{in} \approx (R_{on}g_m + 2\gamma)\frac{nkTC_f}{C_L C_{in} f_s} + \frac{nkT}{f_s}\left[\frac{2\gamma}{C_L}\left(1+\frac{C_f}{C_{in}}\right) + \frac{1-\alpha}{C_f}\right]\left(\frac{C_f f_s}{2\pi n C_{in} f}\right)^2 + \frac{2\gamma kT}{\pi C_L f}\left(\frac{C_f}{C_{in}}\right)^2, \quad (20)$$

where $\alpha$ is used to denote the effect of the proposed auto-zero $kT/C$ noise cancellation and $0 < \alpha < 1$.

Fig. 4 (blue curve) and (black dotted line curve) show the optimized input-referred noise of the spike path and the LFPs path with the proposed auto-zero $kT/C$ noise cancellation technique respectively, where $\alpha$ is set to be 0.9 and the input noise floor is sufficiently low to acquire high-fidelity, full-spectrum neural activity.

## IV. Circuit Measurement and Animal Experiment

The proposed 2-channel SC based neural interface modified from our previous work [22], [27] has been designed and fabricated in a 0.13 $\mu$m CMOS process. Fig. 9 shows the chip micrography of the designed neural interface, where each channel includes an optimized FSA core, a programmable gain amplifier

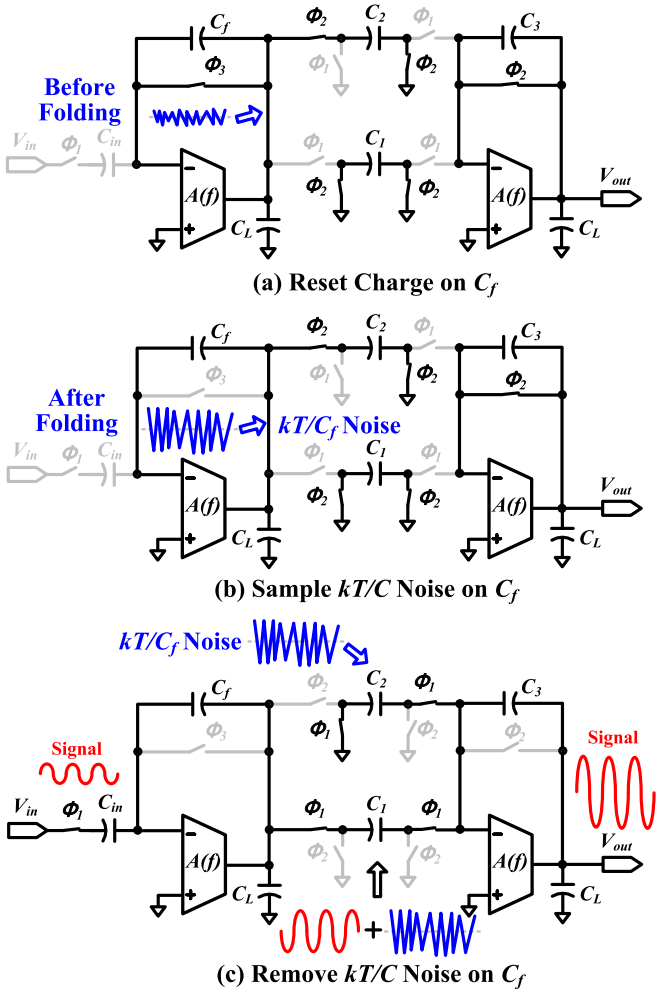


Fig. 8. Proposed $kT/C$ noise cancellation scheme with three steps. First, the charge on $C_f$ is reset. Second, when $\phi_3$ is low and $\phi_2$ is still high, the $kT/C$ noise on $C_f$ is sampled on $C_2$. Third, during $\phi_1$, the FSA outputs including the recorded signals and $kT/C$ noise on $C_f$ are sent to the input capacitor $C_1$ of the subsequent stage with a negative gain of $-C_1/C_3$ while the previous $kT/C$ noise sampled on $C_2$ is simultaneously processed by the subsequent stage with a positive gain of $C_2/C_3$.

with buffer, a 12-bit successive approximation (SAR) ADC, a digital filter for signal reconstruction. On-chip bias circuits and clock generator are shared by the 2-channel recordings. The core circuit area of the designed interface is 1.5 × 0.6 $mm^2$. To achieve low noise performance, the designed recorder chip adopts both the proposed noise optimization techniques presented in Section III and the amplifier bandwidth adjustment technique mentioned in [1].

Fig. 10 shows the measured input noise of the designed recorder chip with/without the proposed noise optimization techniques when the input is shorted to one common mode voltage $V_{cm}$. Measurement results show that the input noise of the LFPs path and the spike path is 4.8 $\mu$V from 1 Hz to 300 Hz and 2.3 $\mu$V from 300 Hz to 8 $kHz$ respectively after using the proposed noise techniques, where the power supply voltage is 1.2 $V$, $f_s$ is 40 $kHz$, $n$ for LFPs path is 16, $C_{in-1} = C_{in-2} = C_{in} = 3$ $pF$, $C_f = 30$ $fF$, and $V_{cm} = 0.6$ $V$. Fig. 11 gives the measured input noise of both the LFPs path and spike path from 10 chips,

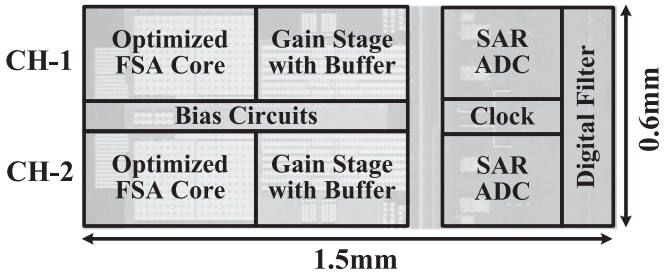


Fig. 9. Chip micrography of the designed 2-channel switched-capacitor neural interface. For each channel, it includes an optimized FSA core, a programmable gain amplifier with buffer, a 12-bit successive approximation (SAR) ADC, and a digital filter for signal reconstruction.

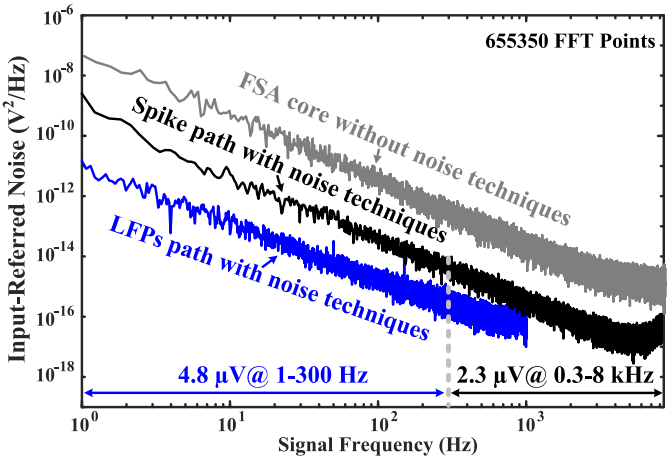


Fig. 10. Measured input-referred noise of the designed chip with/without the proposed noise optimization techniques. After using the proposed noise techniques, the input noise for LFPs path and spike path is 4.8 $\mu$V from 1 Hz to 300 Hz and 2.3 $\mu$V from 300 Hz to 8000 Hz, respectively.

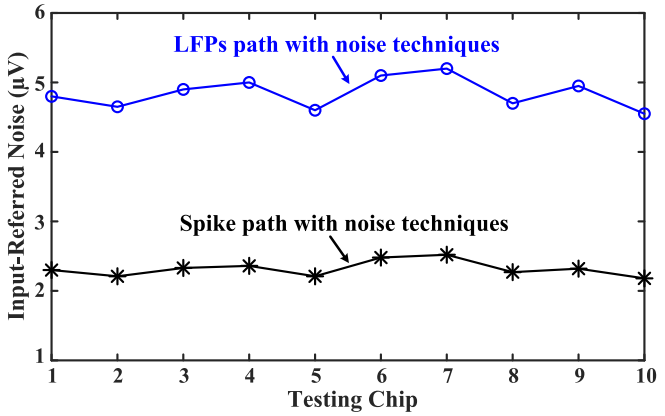


Fig. 11. Measured input-referred noise of both the LFPs path and spike path from 10 chips.

where the averaged input noise of the LFPs path is around 5 $\mu$V from 1 Hz to 300 Hz while that of the spike path is slightly larger than 2 $\mu$V from 300 Hz to 8000 Hz. The total power consumption of the frontend circuits depends on the value of $f_s$ and bias current, where the maximum total power consumption is 16 $\mu W$ per channel, including 6.4 $\mu W$ for the FSA, 5.6 $\mu W$ for the filter, and 4 $\mu W$ for the SAR ADC, when $f_s$ is 40 $kHz$ and

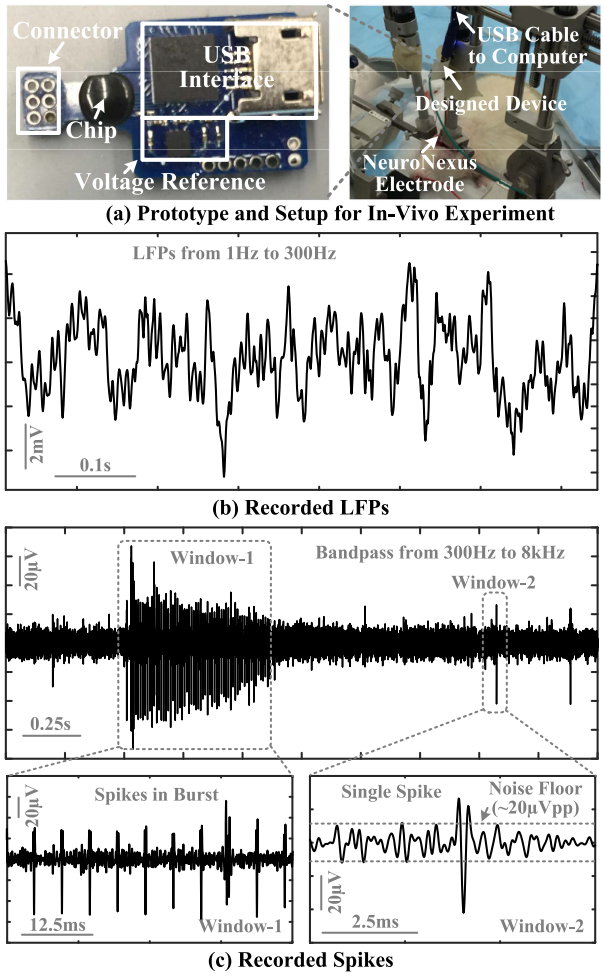


Fig. 12. (a) Designed prototype and setup for *In-Vivo* experiment. (b) The recorded LFPs that are filtered at $1 - -300$ Hz. (c) The recorded extracellular spikes from 300 Hz to 8 $kHz$.

the bias current is 100 $nA$. For data reconstruction, most digital blocks operate at an extremely low duty cycle, thus their power consumption can be ignored compared to the analog frontend circuits. Table I gives the performance summary and comparison with other state-of-the-art works. Due to the frequency-shaping technique, the proposed FSA can compress the recorded neural data dynamic range by around 4.5-bit. Also, the effective number of bits (*ENOB*) of the designed ADC in this work is around 11-bit. Thus, the system dynamic range of the designed neural interface reaches (11 + 4.5)-bit. Besides, because the loop gain of the designed neural interface is proportional to signal frequency $f$, so the measured common mode rejection ratio (*CMRR*) and power supply rejection ratio (*PSRR*) are also related to signal frequency $f$. Other circuit testing results can be found in our previous works [21], [22]. In comparison with these continuous-time based neural interface designs [24], [28]–[30], our designed discrete-time based neural interface architecture can achieve similar input noise floor, lowest input capacitance, and widest system dynamic range.

Fig. 12(a) shows the designed prototype and its setup for animal experiment. The designed prototype consists of the designed

TABLE I
PERFORMANCE SUMMARY OF NEURAL INTERFACES

| Chip | Parameter | [24] | [28] | [29] | [30] | This Work |
|---|---|---|---|---|---|---|
| Interface Chip | Process | 2P3M 0.5 $\mu$m | 1P8M 0.13 $\mu$m | 1P6M 0.18 $\mu$m | 1P8M 0.13 $\mu$m | 1P8M 0.13 $\mu$m |
| | Die Size | 4.7x5.9 mm$^2$ | 4x3 mm$^2$ | 6.08x2.48 mm$^2$ | 5x2.4 mm$^2$ | 1.5x0.6 mm$^2$ |
| | Channel Count | 100 | 64 | 128 | 32 | 2 |
| | Dynamic Range | <10-bit | <8-bit | <8-bit | <10-bit | (11+4.5)-bit |
| | CMRR | $\geq$86 dB | 75 dB | 60 dB | N/A | 50-107 dB |
| | PSRR | $\geq$80 dB | N/A | N/A | 41 dB | 40-98 dB |
| | Supply | 3.3 V | 1.2 V | 1.0 & 1.8 V | 1.0 V | 1.2 V |
| | Total Power | 135 $\mu$W/Ch | 14.5 $\mu$W/Ch | 15.35 $\mu$W/Ch | 1093.75 $\mu$W/Ch | 16 $\mu$W/Ch |
| Neural Amplifier | Structure Type | Continuous Time | Continuous Time | Continuous Time | Continuous Time | Discrete Time |
| | Gain | 60 dB | 54-60 dB | 45.4-60.9 dB | 51.6-76 dB | $3200\pi f/f_s$ for LPFs<br>$200\pi f/f_s$ for spike |
| | Bandwidth | 1-5000 Hz | 10-5000 Hz | 0.4-10300 Hz | 20-15000 Hz | 1-8000 Hz |
| | Input Capacitance | 20 pF | 11.7 pF | 5.85 pF | 61 M$\Omega$ @ 1 kHz | 3 pF |
| | Input Noise | 5.1 $\mu$V<br>for 1-5000 Hz | 6.9 $\mu$V<br>for 10-5000 Hz | 5.18 $\mu$V<br>for 0.4-10300 Hz | 3.0 $\mu$V<br>for 20-15000 Hz | 4.8 $\mu$V for 1-300 Hz<br>2.3 $\mu$V for 300-8000 Hz |
| | Total Power | 42.24 $\mu$W/Ch | 4.5 $\mu$W/Ch | 1.045 $\mu$W/Ch | 11 $\mu$W/Ch | 6.4 $\mu$W/Ch |
| | Circuit Area | <0.16 mm$^2$/Ch | <0.09 mm$^2$/Ch | 0.059 mm$^2$/Ch | <0.07 mm$^2$/Ch | 0.125 mm$^2$/Ch |
| | NEF | 9.92 | 7.2 | 2.56 | 2.95 | 2.33 for 300-8000 Hz |
| ADC | $f_s$ | 15 kHz/Ch | 57 kHz/Ch | 25 kHz/Ch | 50 kHz/Ch | 40 kHz/Ch |
| | *SNDR* | <60 dB | 48.5 dB | 48.76 dB | <60 dB | 71.1 dB |
| | ENOB | <10-bit | 7.8-bit | 7.81-bit | <10-bit | 11.53-bit |
| | Total Power | <100 $\mu$W/Ch | 1.8 $\mu$W/Ch | 0.11 $\mu$W/Ch | 0.7 $\mu$W/Ch | 4.0 $\mu$W/Ch |

chip, one connector for neural probe, one low-noise voltage reference chip, and one universal serial bus (USB) interface for data transfer. In the animal experiment, one NeuroNexus probe is connected to our designed recorder for acquiring neural activity, and the recorded signals are transferred to one computer for further data processing and analysis. Fig. 12(b) gives the recorded LFPs with a peak-to-peak amplitude from $-5$ mV to 5 mV, which are filtered at 1–300 Hz. Fig. 12(c) shows the recorded extracellular spikes filtered from 300 Hz to 8 $kHz$, and the peak-to-peak amplitude of the total noise floor including neural activity, electrode interface noise, and electronic circuit noise is only around 20 $\mu$V. In addition, both spikes in burst (Window-1) and single spontaneous spike activity (Window-2) are acquired during the experiment, and their zoom-in waveforms are also given in Fig. 12(c). Therefore, *In-Vivo* experiment has also demonstrated that our proposed SC based neural interface architecture is suitable for ultra-low noise recording.

## V. CONCLUSION

Several noise optimization techniques, including parasitic capacitance suppression, recording path-splitting scheme, and auto-zero $kT/C$ noise cancellation, have been developed in this work to achieve low input noise floor (around 2 $\mu$V) for switched-capacitor (discrete-time) based neural interface designs. Also, both the circuit measurement and *In-Vivo* experiment have well demonstrated that our designed switched-capacitor based neural interface can feature low input noise, low power consumption, wide system dynamic range, and high input impedance, thus extending the application range of switched-capacitor circuits to high-performance neural data acquisition.

To develop a high-density, low power switched-capacitor based neural interface, several methods will be explored in our future research. First, higher-density metal-insulator-metal (MIM) or MOS capacitors will be preferred to reduce the circuit area occupied by the capacitors. Second, during the chip layout design, some circuit blocks will be put under the capacitor array. Third, we will develop a new neural interface architecture that can allow one single neural recording channel to simultaneously acquire neural activity from multiple electrode recording sites. Fourth, opamp-sharing technique or switched-opamp technique will be employed to further reduce the circuit area and power consumption of the proposed interface.

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