Multicell Reconfigurable Multi-Input Multi-Output Energy Router Architecture

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***Abstract*—This article presents a multicell reconfigurable multi-input multi-output (MR-MIMO) power conversion architecture for multiport applications such as multisource energy router, battery balancer, and photovoltaic optimizer. The MR-MIMO architecture couples a large number of modular dc–ac cells with a single magnetic core which processes multiway bidirectional power flow. The system voltage and current ratings can be linearly extended and reconfigured by connecting the dc–ac cells in series or parallel. The MR-MIMO architecture decouples the voltage rating and current rating of the basic cells, and offers much lower device stress than traditional wide-operation range multiport dc–dc converters. The key contributions of this article include: 1) a multicell reconfigurable 12-winding MIMO converter with high performance across a wide range; 2) a hybrid time-sharing and phase-shift control strategy; and 3) a systematic method of designing multiwinding PCB transformers. The MR-MIMO architecture allows one power converter being used for multiple purposes through software reconfiguration. The work presented in this article proved that it is possible to gain significantly design flexibility in a multicell reconfigurable architecture without sacrificing the efficiency or power density. A 500-W 4-port energy router with 12 modular cells and a 12-winding transformer has been built and tested to verify the effectiveness of the proposed MR-MIMO architecture. The energy router maintains over 95% efficiency across a wide range of input and output voltage options.**

***Index Terms*—Multi-input-multi-output (MIMO), multiport energy router, multicell, power electronics building block.**

I. Introduction

MULTI-INPUT multi-output (MIMO) power converters are needed in many important and emerging applications including photovoltaic (PV) energy systems [1]–[5], microgrids with multiple sources and integrated energy storage [6]–[12], battery management system [13]–[16], electric traction [17], and data centers [18], [19]. Fig. 1 shows three examples of multiport dc–dc power conversion applications including: 1) maximum power point tracking (MPPT) systems for PV arrays; 2) battery management systems; and 3) an energy router for dc power delivery in microgrids managing multiway bidirectional power flow among multiple sources and loads.

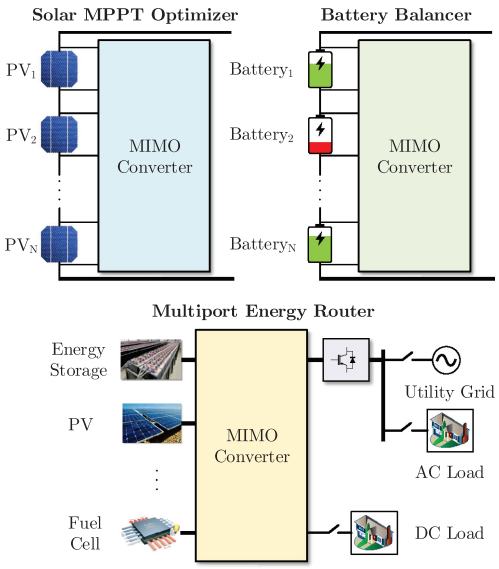

Fig. 1. Three example applications of MIMO power converters, including MPPT optimizer for PV energy systems, battery balancer, and multiport energy router for dc microgrid.

There are two ways of implementing a MIMO system: dc-coupled MIMO architecture, and ac-coupled MIMO architecture. As illustrated in Fig. 2, in a dc-coupled MIMO system, each source/load unit is connected to a public dc bus capacitor through a standalone dc–dc isolated converter with an internal "dc–ac–dc" power conversion stage or a dc–dc nonisolated stage. The dc-coupled MIMO architecture is a combination of several conventional single-input single-output (SISO) dc–dc converters. Due to the existence of the dc bus capacitor, each port can be independently controlled and the power flow is decoupled. In an ac-coupled MIMO architecture, each source/load is connected to a multiwinding transformer through a dc–ac converter, which has only one "dc–ac" power conversion stage. The ac-coupled MIMO architecture uses one magnetic component to perform multiple functions, including voltage conversion and galvanic isolation. It offers reduced stress and higher efficiency,

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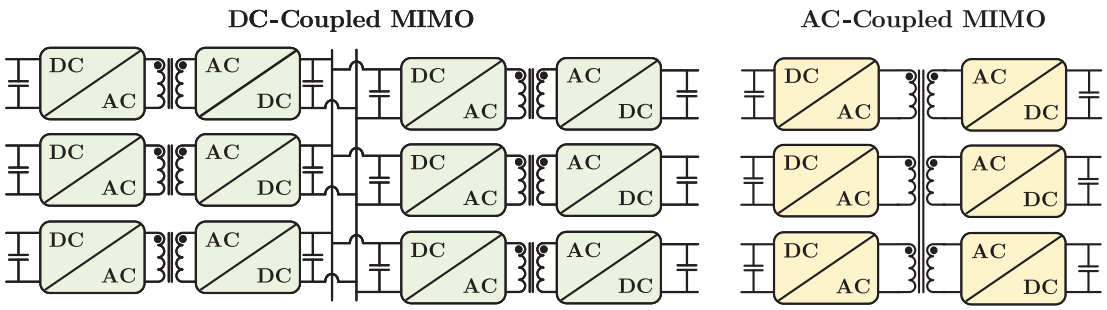

Fig. 2. DC-coupled and ac-coupled MIMO power conversion architecture. The ac-coupled architecture has lower component count and reduced power conversion stress, but requires more precise magnetic models and more sophisticated power flow control strategy.

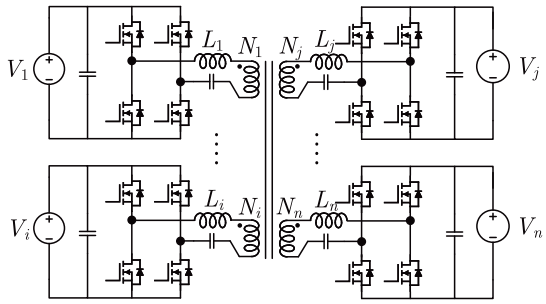

Fig. 3. MAB converter as one specific example of the MR-MIMO converter. The ac–dc cells are implemented as full-bridge inverters driving an inductor and a blocking capacitor.

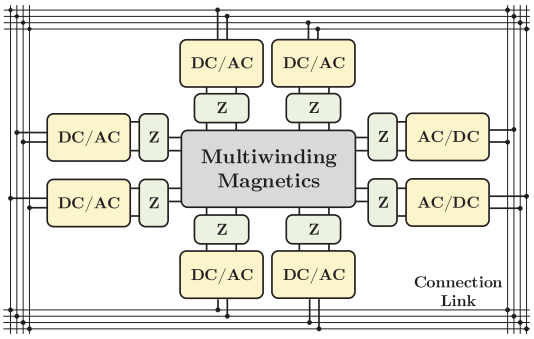

Fig. 4. Key principles of the MR-MIMO architecture with modular dc–ac cells, multiwinding transformer, linking impedance (Z), and connection link which link multiple input/output ports in series or parallel.

but requires precise magnetic modeling and sophisticated power flow control.

Many ac-coupled MIMO topologies have been previously explored [7]–[19]. Most of them are straight forward extensions of the well-known dual-active-bridge or multiactive-bridge (MAB) family [20], [21]. Fig. 3 shows the topology of an MAB converter. The dc–ac converters function as square-wave voltage sources, which drive the multiwinding transformer. Existing demonstrations of MAB converters are usually limited to three or four cells with nonreconfigurable magnetics. This article further extends the MAB converter into a multicell reconfigurable architecture with more than ten cells. These cells can be configured in series or parallel. The control complexities of the power flow are orders-of-magnitude higher. Fig. 4 shows an example MR-MIMO design with eight modular dc–ac cells coupled to a multiwinding transformer through an impedance network "Z." The dc–ac cells are connected in series or parallel into a few ports through external connection links, which can be fabricated on a printed circuit board (PCB). The MR-MIMO architecture couples multiple dc–ac cells with a single magnetic core, which carries multiway bidirectional power flow. We experimentally verified that the output voltage of a large number of dc–ac cells can be precisely regulated by distributed phase-shift control and time-sharing control. The MR-MIMO architecture decouples the voltage rating and current rating of the dc–ac cells, improves the utilization of the magnetic core, and offers much lower device stress than traditional solutions with multiple standalone converters.

The key contributions of this article include: 1) a multicell reconfigurable 12-winding MIMO converter with high performance across a wide range; 2) a hybrid time-sharing and phase-shift control strategy; and 3) a systematic method of designing multiwinding PCB transformers. The MR-MIMO architecture allows one power converter being used for multiple purposes. We show that it is possible to gain significantly design flexibility in a multicell reconfigurable architecture without sacrificing the efficiency or power density, opening the potential of future software-defined power electronics.

The MR-MIMO architecture is particularly applicable to energy systems with a large number of modular cells, such as differential power processing systems for server racks [19], solar panels [22], battery cells [23], and modular multilevel converters (MMCs) [24]. These modular cells usually have identical voltage and current ratings. The dc–ac cells can be duplicated to interconnect large numbers of modular targets. A MR-MIMO converter is also applicable to power management systems in dc microgrids, hybrid electric vehicles or more electric airplanes, where a multiport power converter may interface with many sources and loads. The dc–ac cells can be connected in series/parallel according to the targeting voltage rating and current rating, and can be reconfigured to cover a wide operation range without sacrificing the performance.

The remainder of this article is organized as follows: Section II introduces the operation principles of the MR-MIMO architecture. Section III presents the modeling and analysis of

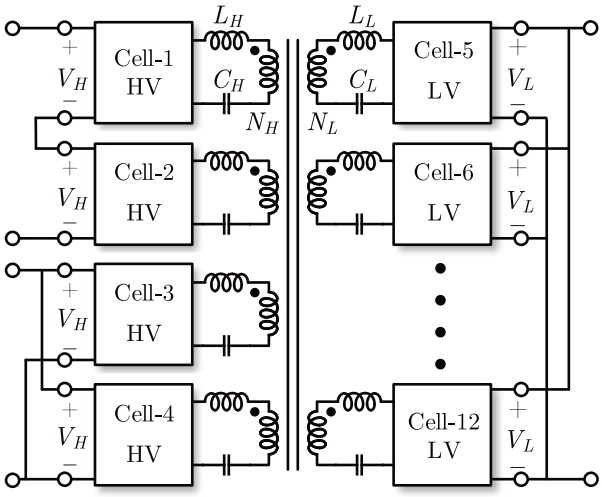

Fig. 5. Example multiport system with MR-MIMO architecture. A large number of HV and LV cells can be connected in series or parallel to create input/output ports with software reconfigurable voltage and current ratings.

the MIMO power flow. Section IV describes the power flow control strategies with a matrix reduction method to simplify the control complexity. Section V presents the design methods for the multiwinding magnetics. Experimental results of a 500-W 12-winding four-port MR-MIMO converter are summarized in Section VI. Finally, Section VII concludes this article.

II. Multicell Reconfigurable MIMO Architecture

As illustrated in Fig. 4, an MR-MIMO architecture comprises many dc–ac cells connected with a linking impedance (Z), a multiwinding magnetic core, and a few connection links, which can be used to implement series–parallel connections. The dc–ac cells can be implemented as half/full-bridge, Class-D, or other typical dc–ac conversion circuits. The dc–ac cells can interface with the multiwinding transformer with series resonant, parallel resonant, LLC, or other related principles. The voltage and current rating of each port can be linearly extended by connecting multiple cells in series or parallel as illustrated by the multicell concepts in [25]–[27].

Fig. 5 shows the schematic of an MR-MIMO architecture with 12 modular cells. Two types of modular cells are implemented as examples: four high-voltage (HV) cells, and eight low-voltage (LV) cells. The HV cells can be stacked in series to interface with HV ports (e.g., the 400-V dc bus in a power factor correction (PFC) converter), and the LV cells can be connected in parallel to interface with high current ports (e.g., a 12 V, 20 A port as needed for LV loads). For all the dc–ac cells in the same port, the dc bus voltage and cell power are equally shared (V_H for all HV cells and V_L for all LV cells) so that the port voltage and port power can be linearly extended by adding more dc–ac cells. The dc–ac cells in the same port are controlled by the same gate driver signals for "plug-and-play" extensions in the voltage rating and current rating. The MR-MIMO architecture has the following advantages.

1) Reduced switch stress: As illustrated in Fig. 6(a), the switches and passive components in a wide operation range power converter must be rated for the maximum voltage ($V_{\max}$) and maximum current ($I_{\max}$). The total power rating of the device (the product of voltage rating and current rating) is much higher than the actual system power rating (constant power curve P_o) [28], which is usually thermal related. By dividing the system into multiple cells each rated for a fraction of the voltage rating and current rating [see Fig. 6(b)], the device rating of the system can be much closer to the actual constant system power rating curve. This "multicell" configuration is particularly useful for universal input power factor correction circuits [29], and wide input multiport energy routers that need to operate across a wide range.
2) Reduced magnetic component size: A traditional MIMO converter usually has multiple transformers performing voltage conversion or galvanic isolation. In an MR-MIMO architecture, voltage conversion and galvanic isolation is realized by a single multiwinding transformer. The cross-sectional area of the core is determined by the maximum volt-second-per-turn of all windings of the multiwinding transformer, and is not related to the number of windings or input/output ports [19]. The total core loss of multiwinding transformer is the same as a two-winding transformer [17]. The magnetic core volume in an n port ac-coupled MIMO architecture is n times smaller than the total magnetic core volume needed by a dc-coupled MIMO architecture.
3) Better heat distribution: The MR-MIMO architecture inherits the advantages of distributed (granular) power processing. By dividing the power conversion stress among multiple modules with evenly shared voltage rating and current rating, the heat is uniformly generated on a few LV rating (current rating) devices, instead of concentrating on a few heavy rated bulky devices. Better heat distribution translates to smaller heat sinks, smaller volume, and lower cost. Moreover, lower voltage rating devices can usually offer better devices characteristics (lower on resistance per die area) than HV rating devices (i.e., "Baliga Figure-of-Merit" [28], [30], [31]).

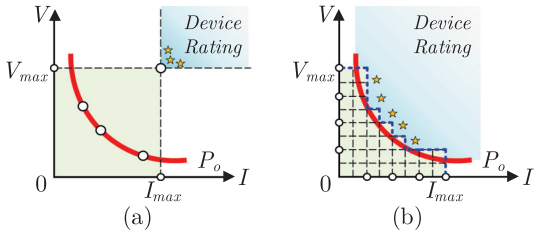

Fig. 6. Power rating of semiconductor devices across a wide operation range compared to a constant power curve (P_o): (a) the device ratings must be higher than $V_{\max}$ and $I_{\max}$ in a nonreconfigurable power converter; (b) converter with many flexible cells can cover the operation range with much lower device rating (very close to the P_o curve).

Fig. 7 shows an example implementation of a modular dc–ac converter as the basic cell, comprising one full-bridge circuit with isolated gate drivers and an isolated auxiliary power supply, a dc decoupling capacitor C_{dc}, a branch inductor, a dc blocking capacitor, and a PCB winding. All PCB windings are coupled to

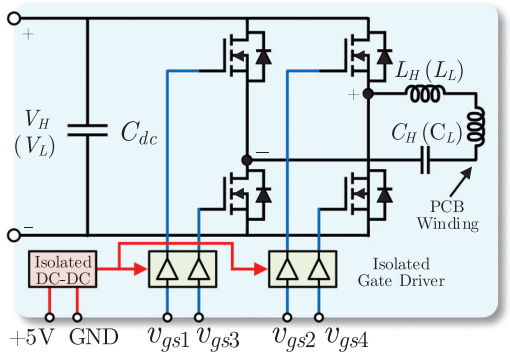

Fig. 7. Circuit schematic of an example dc–ac cell including a power stage and a control stage. Both the power stage and the control stage are highly modular to enable "plug-and-play" extensions and reconfigurations.

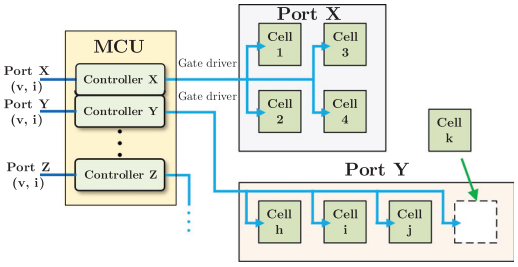

Fig. 8. Principles of the group-control strategy for the MR-MIMO architecture. Modular cells are connected in series and in parallel, and can be linearly extended without changing the overall control strategy.

a single magnetic core. All dc–ac cells are controlled by phase-shift modulation using a common clock signal as the reference. A leading phase-shift from the common clock will allow the cell to feed power into the magnetic core, and a lagging phase-shift from the common clock will allow the cell to extract power from the magnetic core.

Fig. 8 shows the "group-control" diagram of the MR-MIMO architecture. An input/output port may include an arbitrary number of dc–ac cells controlled by one set of gate driver signals. This configuration enables "plug-and-play" function for the MR-MIMO architecture. The controller of each port only senses the port voltage and/or port current for making local switching actions. Without loss of generality, no effort is made to balance the dc bus voltage of series-stacked dc–ac cells or equalize the output current of each parallel-connected dc–ac cells. As long as strong coupling of the magnetic core is guaranteed, and the system is designed with high symmetry, voltage balancing and current balancing are maintained.

III. Modeling and Analysis of MIMO Power Flow

One key challenge of the MR-MIMO design is to control the sophisticated power flow in the multiwinding transformer. Conceptually, controlling the power flow in the multiwinding transformer of a multiport ac-coupled converter is similar to controlling the power flow in a traditional 60-Hz ac grid, except that the system frequency is much higher [32], [33]. The power flow in a multiport ac-coupled converter can be controlled by time-domain multiplexing (time-sharing), frequency-domain

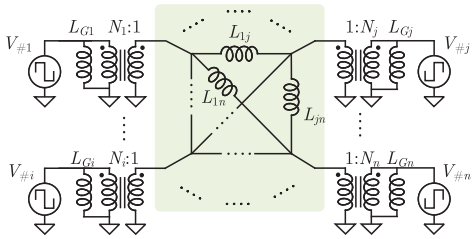

Fig. 9. Cantilever model of a multiwinding transformer in the MR-MIMO architecture. Each dc–ac cell is modeled as a square-wave voltage source. The external inductors as needed by the MAB operation are merged into the cantilever model.

multiplexing, or phase-shift [7]–[10], [17], depending on the specific implementation of the dc–ac cells. All the control methods require precise model of the multiport converter with the multiwinding transformer.

A. MIMO Cantilever Model and Multiway Power Flow

The dc–ac cells are modeled as square wave voltage sources $V_{\#1}$–$V_{\#n}$, which drive the multiwinding transformer in Fig. 9. The ac voltage of each dc–ac cell is the summation of external inductor voltage and winding voltage

$$\begin{bmatrix} V_{\#1} \\ \vdots \\ V_{\#n} \end{bmatrix} = j\omega \begin{bmatrix} L_{11}+L_1 & \cdots & M_{1n} \\ \vdots & \ddots & \vdots \\ M_{n1} & \cdots & L_{nn}+L_n \end{bmatrix} \begin{bmatrix} I_{W1} \\ \vdots \\ I_{Wn} \end{bmatrix} \quad (1)$$

where I_{Wi} is the winding current, L_i is the external inductor, L_{ii} is the self-inductance of Winding-i, and $M_{ij} = M_{ji}$ is the mutual-inductance between Winding-i and Winding-j. The impedance matrix ($\boldsymbol{M_Z}$) in (1) includes the external inductors and the impedance of multiwinding transformer.

As illustrated in Fig. 9, the interconnect of the multiple windings can be also represented by a network of equivalent inductance L_{ij} connecting Cell-i and Cell-j (see [34]). Each cell has an equivalent magnetizing inductance L_{Gi}. The equivalent inductance L_{ij} is related to the admittance matrix ($\boldsymbol{M_Y}$) of the ac voltages of cells and the winding currents, which is the inverse of the impedance matrix $\boldsymbol{M_Z}$

$$\boldsymbol{M_Y} = \frac{1}{j\omega} \begin{bmatrix} Y_{11} & \cdots & Y_{1n} \\ \vdots & \ddots & \vdots \\ Y_{n1} & \cdots & Y_{nn} \end{bmatrix} = \boldsymbol{M_Z}^{-1}. \quad (2)$$

The equivalent inductance L_{ij} and L_{Gi} are

$$L_{ij} = \frac{-1}{N_i N_j Y_{ij}}, L_{Gi} = \left(Y_{ii} + \frac{1}{N_i} \sum_{j \neq i} (N_j Y_{ij}) \right)^{-1}. \quad (3)$$

Here, N_i and N_j are the turns numbers of the transformer windings. Following the derivations in [1], [32], the average power delivered to Cell-i from the transformer is

$$P_i = \frac{1}{2\pi^2 f_s} \frac{V_i}{N_i} \sum_{j \neq i} \frac{V_j}{N_j} \frac{(\Phi_i - \Phi_j)(\pi - |\Phi_i - \Phi_j|)}{L_{ij}}. \quad (4)$$

Here Φ_i and Φ_j are the phase-shift angles of cell-i and cell-j, respectively; and f_s is the switching frequency.

B. Voltage Balancing and Current Sharing

Equation (4) indicates that the power flow among the dc–ac cells can be controlled by their phase-shift angles. Based on the group-control concept, the cells in the same port are controlled by the same phase-shift angle no matter how they are connected. No active balancing control is applied to the single dc–ac cell. Equally distributed cell power can ensure voltage balancing for the series-connected cells and current balancing for the parallel-connected cells. Equation (4) represents the general MIMO power flow with arbitrary dc bus voltage, turns number, and phase-shift angles. In the MR-MIMO architecture, the power flow equation can be expressed as the summation of power from all other ports

$$P_{X.i} = P_{X-i} + P_{Y-i} + P_{Z-i} + \cdots . \tag{5}$$

$P_{X.i}$ is the total power received by Cell-i in Port-X, $P_{X-i}, P_{Y-i}, P_{Z-i}$ are the power from Port-X, Y, Z. Obviously $P_{X-i} = 0$ since there is no phase difference between cells in the same port. Assuming each port only has one type of cells (HV or LV), the power distribution among cells in one port can be analyzed in the following three cases.

1) Both Port-X and Port-Y have parallel cells: The port voltages are V_{Px} and V_{Py}, the phase-shift angels are Φ_x and Φ_y, the winding turns numbers are N_x and N_y, respectively. The power fed into Cell-i in Port-X from Port-Y is

$$P_{Y-i} = K\frac{V_{Px}}{N_x}\frac{V_{Py}}{N_y}\sum_{j\in Y}\frac{1}{L_{ij}}$$

$$K = \frac{(\Phi_x - \Phi_y)\left(\pi - |\Phi_x - \Phi_y|\right)}{2\pi^2 f_s}. \tag{6}$$

Cell-j is one cell in Port-Y. Power balancing among the cells in Port-X is guaranteed if

$$\sum_{j\in Y}\frac{1}{L_{ij}} = \sum_{j\in Y}\frac{1}{L_{kj}} = \cdots, \{i,k,\ldots\} \in X. \tag{7}$$

A stronger condition for power balancing is: the inductance matrix between Port-X and Port-Y is symmetrical. For any L_{ij} between Cell-i in Port-X and Cell-j in Port-Y, there is always a L_{kl} (Cell-k belongs to Port-X and Cell-l belongs to Port-Y) which equals L_{ij}.

2) Port-X has all series cells and Port-Y has parallel cells. The average output currents of Cell-i and Port-X are

$$I_i = \frac{P_{Y-i}}{V_i} = K\frac{1}{N_x}\frac{V_{Py}}{N_y}\sum_{j\in Y}\frac{1}{L_{ij}}$$

$$I_x = \frac{\sum_{i\in X}P_{Y-i}}{\sum_{i\in X}V_i} = K\frac{1}{N_x}\frac{V_{Py}}{N_y}\frac{\sum_{i\in X}\left(V_i\sum_{j\in Y}\frac{1}{L_{ij}}\right)}{\sum_{i\in X}V_i}. \tag{8}$$

As shown in Fig. 10, the average current of each series cell equals to the average output current of the port. Otherwise the charge difference will accumulate on the dc bus capacitor of each series cell and result in voltage unbalancing. Solving $I_i = I_x$, the voltage balancing condition for series cells can be found same as (7). Unbalanced cell voltage leads to higher current ripple (i_{31} and i_{32}) and circulating current (i_{12}) among cells in the same port. Similarly, the power of Cell-j in Port-Y from Port-X is

$$P_{X-j} = K\frac{1}{N_x}\frac{V_{Py}}{N_y}\sum_{i\in X}\frac{V_i}{L_{ij}}. \tag{9}$$

With (7), the voltage balancing in Port-X is ensured and the power sharing in Port-Y is guaranteed.

3) Both Port-X and Port-Y have series power cells. Similar to Case 2, the average output current of Cell-i in Port-X and the average port current are

$$I_i = K\frac{1}{N_xN_y}\sum_{j\in Y}\frac{V_j}{L_{ij}}$$

$$I_x = K\frac{1}{N_xN_y}\frac{\sum_{i\in X}\left(V_i\sum_{j\in Y}\frac{V_j}{L_{ij}}\right)}{\sum_{i\in X}V_i}. \tag{10}$$

The average output current of Cell-j in Port-Y (I_j) and the average output current of Port-Y (I_y) can be presented in the same way. Solving $I_i = I_x$ and $I_j = I_y$, the condition for simultaneously balancing the cell voltage in both Port-X and Port-Y is the same as (7).

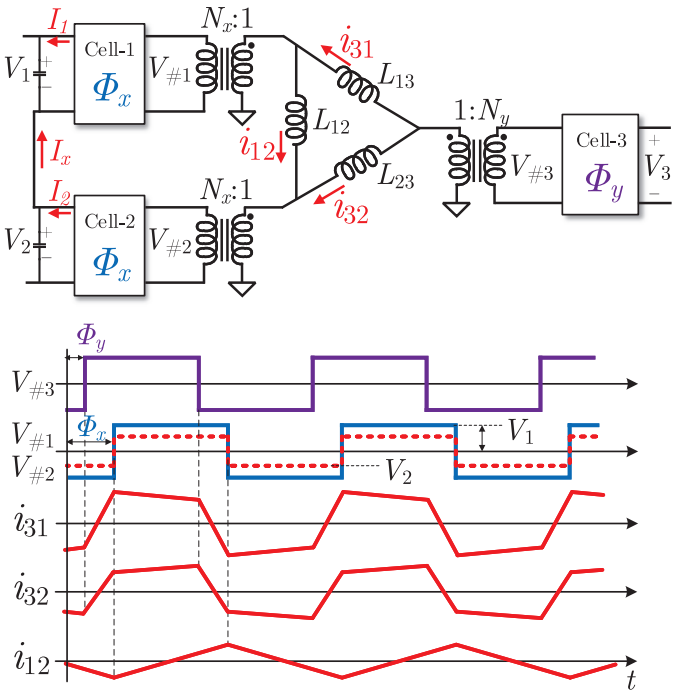

Fig. 10. Simplified example of power distribution in the port with all series cells: Cell-1 and Cell-2 are series-connected in Port-X, and Cell-3 is the only dc–ac cell in Port-Y. Unbalanced voltage causes circulating current between cells in the same port even if they are operating in phase.

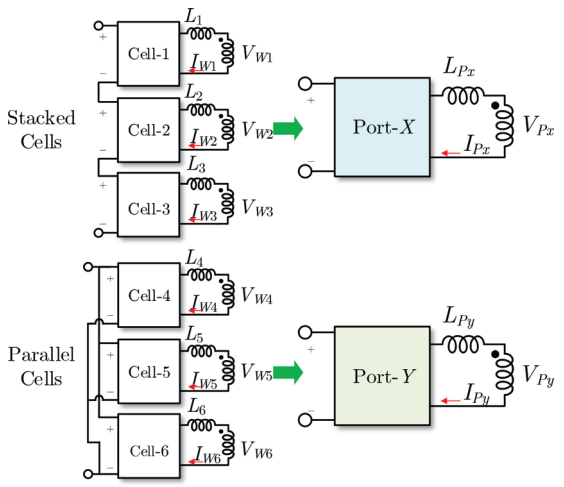

Fig. 11. Equivalent circuits of a port with three series-connected dc–ac cells and a port with three parallel-connected dc–ac cells. A matrix reduction method is developed to simplify the inductance matrix of the transformer.

A practical MR-MIMO design may comprise both series and parallel configurations. The condition to achieve voltage balancing and current balancing is given by (7). A sufficient condition for achieving automatic voltage balancing and current balancing is to ensure a symmetric inductance matrix for the multi-winding transformer. Active voltage and current control for each single dc–ac cell is not necessary with automatic balanced voltage and current across the series and/or parallel connected cells.

IV. Control Strategies of the MIMO Power Flow

The power flow analysis becomes extremely sophisticated if there are a large number of cells in the MR-MIMO architecture. Chen *et al.* [1] investigated the phase-shift control and time-sharing control for the MR-MIMO converter. It can greatly reduce the control complexity by introducing additional design degree of freedoms. In this work, we further introduce a matrix reduction method to simplify the power flow control in the MR-MIMO architecture by leveraging the fact that multiple ports are connected in series/parallel with commonly shared voltage and current.

A. Matrix Reduction Method

Fig. 11 shows the equivalent circuit model of three stacked cells in Port-X and three parallel cells in Port-Y. The equivalent winding voltage of Port-X is the summation of winding voltage of all series-connected cells

$$V_{Px} = V_{W1} + V_{W2} + V_{W3}. \tag{11}$$

With the same gate-driver signals and the symmetric inductance matrix, the winding current in all cells are equal

$$I_{Px} = I_{W1} = I_{W2} = I_{W3}. \tag{12}$$

The equivalent external branch inductance L_{Px} is the summation of the series inductance of all branch inductors

$$L_{Px} = L_{W1} + L_{W2} + L_{W3}. \tag{13}$$

The equivalent winding voltage of Port-Y equals the winding voltage of all parallel connected cells

$$V_{Py} = V_{W4} = V_{W5} = V_{W6}. \tag{14}$$

The equivalent winding current is the summation of all the individual winding current

$$I_{Py} = I_{W4} + I_{W5} + I_{W6}. \tag{15}$$

The equivalent branch inductance is equal to the parallel inductance of all branch inductors

$$L_{Py} = L_{W4}||L_{W5}||L_{W6}. \tag{16}$$

If n dc–ac cells are grouped into m ports ($m < n$), a vector of the winding voltage with n elements can be converted into a vector of the equivalent winding voltage with m elements by an $m \times n$ matrix $\boldsymbol{Q_V}$

$$\begin{bmatrix} V_{P1} \\ \vdots \\ V_{Pm} \end{bmatrix} = \begin{bmatrix} Q_{V11} & \cdots & Q_{V1n} \\ \vdots & \ddots & \vdots \\ Q_{Vm1} & \cdots & Q_{Vmn} \end{bmatrix}_{m\times n} \begin{bmatrix} V_{W1} \\ \vdots \\ V_{Wn} \end{bmatrix}. \tag{17}$$

Each element of $\boldsymbol{Q_V}$ can be identified by the following.

1) If Port-i consists series-connected cells, and Cell-j belongs to Port-i, then $Q_{Vij} = 1$; Otherwise, $Q_{Vij} = 0$.
2) If Port-i consists parallel-connected cells, and Cell-j, k, l belong to Port-i, set any one of Q_{Vij}, Q_{Vik}, Q_{Vil} be 1, and all other elements on the same row as 0.

The equivalent port winding current can be extracted by current conversion matrix $\boldsymbol{Q_C}$

$$\begin{bmatrix} I_{W1} \\ \vdots \\ I_{Wn} \end{bmatrix} = \begin{bmatrix} Q_{C11} & \cdots & Q_{C1m} \\ \vdots & \ddots & \vdots \\ Q_{Cn1} & \cdots & Q_{Cnm} \end{bmatrix}_{n\times m} \begin{bmatrix} I_{P1} \\ \vdots \\ I_{Pm} \end{bmatrix}. \tag{18}$$

Each element of $\boldsymbol{Q_C}$ can be identified by the following.

1) If Cell-i belongs to a series-connected Port-j, then $Q_{Cij} = 1$; Otherwise $Q_{Cij} = 0$.
2) If Cell-i, k, l belong to a parallel-connected Port-j, then set $Q_{Vij} + Q_{Vkj} + Q_{Vlj} = 1$.

The $m \times m$ "port-to-port" impedance matrix $\boldsymbol{M_{P2P}}$ is

$$\boldsymbol{M_{P2P}} = \boldsymbol{Q_V} \begin{bmatrix} L_{11} & \cdots & M_{1n} \\ \vdots & \ddots & \vdots \\ M_{n1} & \cdots & L_{nn} \end{bmatrix} \boldsymbol{Q_C}. \tag{19}$$

If one port has both series-connected cells and parallel-connected cells, the matrix reduction can be performed in the following two steps: 1) convert the port to several subports with parallel-connected cells, and 2) convert these series-connected subports to one port. With the $m \times m$ impedance matrix, the n-winding transformer can be simplified to a cantilever model with m-equivalent windings as shown in Fig. 12. N_{Pi} is the equivalent turns number, which is equal to the total turns number of series-connected cells and the identical turns number of parallel-connected cells. Similar to (1) and (2), the impedance and admittance matrices of the resulting port are

$$\boldsymbol{M_{PZ}} = \boldsymbol{M_{P2P}} + \text{diag}\{L_{P1}, L_{P2}, \ldots, L_{Pm}\} \tag{20}$$

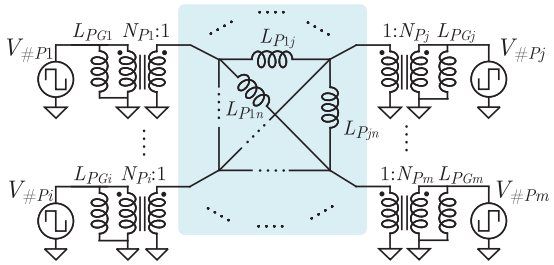

Fig. 12. Simplified cantilever model with m ports which can be used to model the large-signal and small-signal dynamic behaviors of the system.

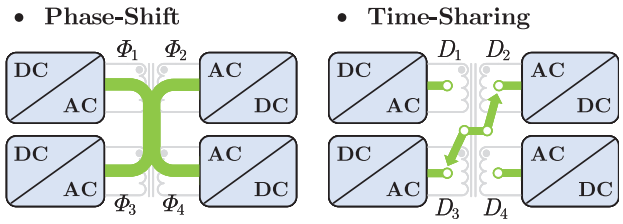

Fig. 13. Principles of the phase-shift and time-sharing control of the MR-MIMO architecture [1].

$$\boldsymbol{M_{PY}} = \boldsymbol{M_{PZ}}^{-1}. \tag{21}$$

The equivalent "port-to-port" inductance L_{Pij} and magnetizing inductance L_{PGi} in Fig. 12 can be calculated in the same way as (3). Replacing V_i, V_j, N_i, N_j, and L_{ij} in (4) with V_{Pi}, V_{Pj}, N_{Pi}, N_{Pj}, and L_{Pij} results in the average power delivered to Port i from the other ports.

B. Hybrid Phase-Shift and Time-Sharing Control

Fig. 13 shows the principles of the phase-shift control and time-sharing control. Phase-shift control regulates phase-shift angles of all ports simultaneously to route the MIMO power flow. While only single input port and single output port are activated with fixed phase-shift angle under time-sharing control. The delivered/received power of one port is regulated by the duty ratio in the time-sharing cycle. As investigated in [1], phase-shift control achieves higher efficiency at heavy load; time-sharing control achieves higher efficiency at light load; combining time-sharing control with phase-shift control can maintain high performance across a wide operation range.

Fig. 14 shows the diagram of distributed phase-shift control [1], [35]. The phase-shift angle of all dc–ac cells in the same port is adjusted by a PI controller. Z_x, Z_y, ..., are the load impedance and $K_{\Phi xy}$, $K_{\Phi yz}$, ..., are the small signal transfer functions from the phase-shift angle to port current [1]. The phase-shift control of each port is closely coupled and requires all the small signal transfer functions to design the PI controller. For example, in the MIMO converter with 12 dc–ac cells, the transfer functions from phase-shift angle to cell current forms a 12×12 matrix. With the matrix conversion, the order of the small signal transfer matrix reduces to 4×4 (with four input and output ports), which significantly mitigates the control complexity.

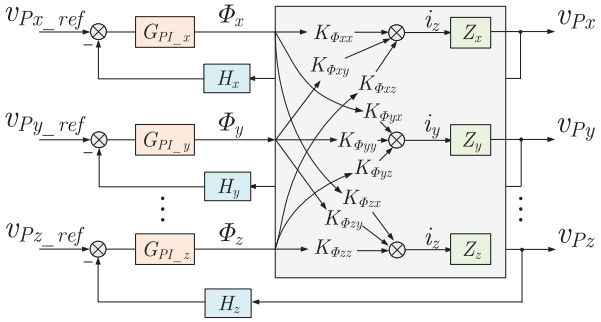

Fig. 14. Diagram of the close-loop phase-shift control for the port voltage. The voltage of each port is modulated by a PI controller which adjusts the phase-shift angle of all dc–ac cells in this port.

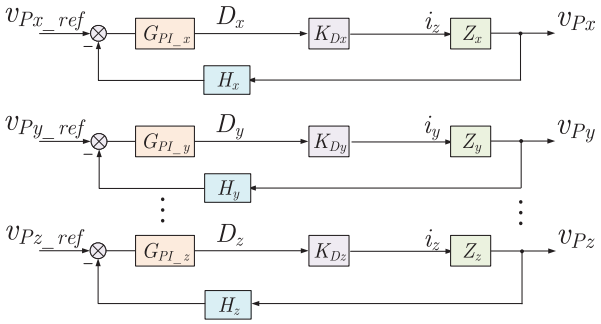

Fig. 15. Diagram of the close-loop time-sharing control for the port voltage. The PI controller adjusts time-sharing duty-ratio of all dc–ac cells in this port.

Time-sharing control offers additional control degree of freedom. Time-sharing control is completely decoupled from phase-shift control when there are only one input port and one output port working at one time. Fig. 15 shows the PI control of time-sharing duty ratio (D) for port voltage regulation. The phase-shift angles are fixed. K_{Dx}, K_{Dy}, ..., are the small signal transfer functions from the time-sharing duty ratio to port current [1]. There exists one constraint for the time-sharing duty ratio of all output ports: $D_x + D_y + D_z + \cdots \leq 1$. Time-sharing control is the extension of "Burst Operation" in typical SISO power converters. It helps improve the light load efficiency and can be mixed with the previously described matrix reduction method.

V. Multiwinding Transformer Design

A. Magnetic Core and Winding Loss

The transformer used in existing MAB converters are usually limited to three or four windings. The MR-MIMO architecture requires a multiport transformer with a large number of windings (i.e., >10), placing new opportunities and challenges in magnetics design. Fig. 16 shows a prototype MR-MIMO converter including eight modular dc–ac boards, one UU-type magnetic core, one motherboard (bottom), and one controller board. A modular dc–ac board comprises one HV dc–ac cell or two LV dc–ac cells. There are four HV cells and eight LV cells in this prototype. The dc–ac boards are coupled together with the magnetic core. The motherboard connects the cells in series or in

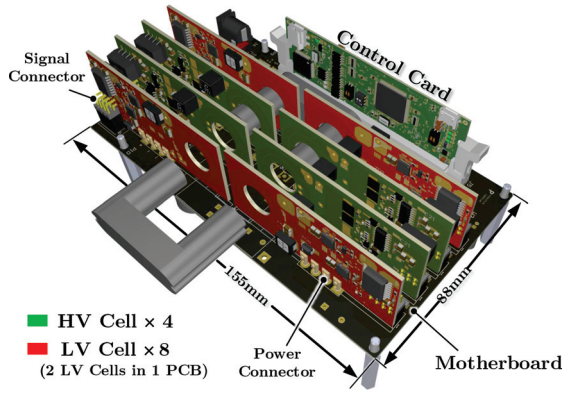

Fig. 16. 3-D assembly drawing of a 500-W MR-MIMO converter with 12 cells, including 4 HV cells (in green) and 8 LV cells (in red) with interleaved winding structure. The system is reconfigurable and extendable.

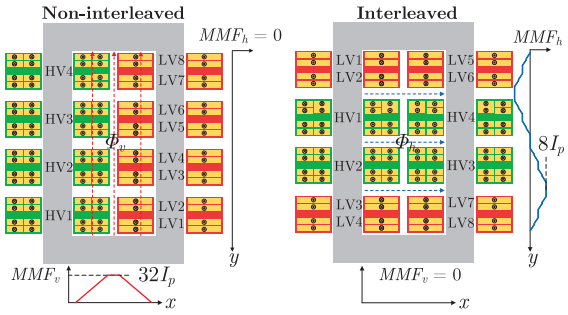

Fig. 17. Winding cross-sectional view and MMF distribution in an ideal multiwinding transformer with infinite permeability and high coupling coefficient. Left: noninterleaved winding placement; Right: interleaved winding placement. The interleaved winding placement has more evenly distributed magnetic flux density.

TABLE I
PARAMETERS OF THE MR-MIMO PROTOTYPE

Specifications & Symbol	Description
HV Cell Voltage V_H	72 V
HV Winding Turns N_H	8
HV Branch Inductor L_H	Coilcraft XEL6060 – 2.7 μH
HV Blocking Capacitor C_H	200 μF
HV Bus Capacitor C_{dch}	4 μF
HV MOSFETs	GS61004B 100 V
LV Cell Voltage V_L	9 V
LV Winding Turns N_L	1
LV Branch Inductor L_L	Coilcraft SLC7530S – 64 nH
LV Blocking Capacitor C_L	440 μF
LV Bus Capacitor C_{dcl}	44 μF
LV DrMOS	SIC632 24 V
Switching Frequency f_s	200 kHz
Transformer Core	0P4413UC, $\mu_r = 2500$

parallel as input or output ports. The motherboard can be made reconfigurable with relays or MOSFETs, and can be replaced for different voltage conversion ratios. The key parameters of the MR-MIMO converter are listed in Table I.

There are many ways of placing the HV and LV cells around the magnetic core. Two winding placements are investigated and compared in this article as examples. Fig. 17 shows the cross-sectional view of an interleaved winding placement and a noninterleaved winding placement. The HV cells are labeled in green and the LV cells are labeled in red. The modular PCB board comprises four copper layers. Each one-turn winding of the LV cells comprises two parallel-connected copper layers. If all HV cells are on the primary side and all LV cells are on the secondary side, the primary side current I_p and secondary side current I_s in the multiple windings of this transformer with an ungapped core with infinite permeability is

$$32 \times I_p = 16 \times \frac{1}{2} \times I_s. \tag{22}$$

Fig. 17 also illustrates the magnetomotive force (MMF) in this multiwinding transformer with interleaved and noninterleaved winding placements. In the noninterleaved placement, the horizontal flux Φ_h is canceled by the same winding current of two adjacent HV or LV windings and the MMF at the same position is zero. However, the opposite currents of one HV cell on the left-hand side and one LV cell on the right-hand side enhance the vertical flux Φ_v and the maximum MMF is $32I_p$ at the central vertical axis of the window area. In the interleaved placement, the flux and MMF distribution are very different from those in the noninterleaved structure. The horizontal flux in the window area is enhanced while the vertical flux is canceled. The maximum MMF is only $8I_p$. Both the magnetic field strength and the core loss are reduced with interleaved winding structure.

The interleaved structure can also reduce the ac winding resistance and winding loss with canceled vertical flux. Eddy current is induced on the horizontal plane by the vertical flux Φ_v and makes the winding current accumulate at the rim of the copper trace. The horizontal flux Φ_h induces eddy current on the vertical plane and makes winding current accumulate on the top or the bottom surface of the copper trace. The copper thickness used in this design is 70 μm, which is smaller than the skin depth (170 μm) at the switching frequency (200 kHz) and much smaller than the width of PCB trace (2.75 mm for HV winding and 6 mm for LV winding). As a result, it is more important to equally distribute current along the radius of circular PCB winding with canceled vertical flux to reduce the ac resistance. Thus, the interleaved winding structure is much better than the noninterleaved option with smaller MMF, proper flux distribution and lower ac resistance.

We use ANSYS Maxwell to verify the analysis and the key principles. The relative permeability of the core is 2500. The excitation current is 4 A on the primary side (I_p) and 16 A on the secondary side (I_s). The excitation frequency is 200 kHz. The magnetic field strength H in the window area and core flux density B are shown in Fig. 18. The magnetic field strength in the noninterleaved structure is much stronger than the field strength in the interleaved structure. The distribution of H also matches the flux distribution analysis. The flux density in the core of the interleaved structure is significantly lower than that in the noninterleaved structure, especially on the two vertical sides. Fig. 19 shows the current density in the PCB windings. The outer edge of the PCB winding in the noninterleaved structure has higher current density due to the eddy current induced by the

TABLE II
EQUIVALENT INDUCTANCE MATRIX INCLUDING EXTERNAL INDUCTORS AMONG THE CELLS OF THE INTERLEAVED 12-WINDING TRANSFORMER

	HV1	HV2	HV3	HV4	LV1	LV2	LV3	LV4	LV5	LV6	LV7	LV8
HV1	1.37 mH	304.85 nH	4.505 μH	2.223 μH	522.07 nH	450.64 nH	1.481 μH	1.664 μH	3.249 μH	3.472 μH	11.11 μH	9.936 μH
HV2		1.37 mH	2.223 μH	4.505 μH	1.663 μH	1.481μH	450.65 nH	522.08 nH	9.936 μH	11.11 μH	3.472 μH	3.284 μH
HV3			1.37 mH	304.85 nH	9.936 μH	11.11 μH	3.472 μH	3.428 μH	1.664 μH	1.481 μH	450.65 nH	522.09 nH
HV4				1.37 mH	3.249 μH	3.473 μH	11.11 μH	9.935 μH	522.07 nH	450.65 nH	1.481 μH	1.664 μH
LV1					29.07nH	202.30 nH	6.336 μH	6.841 μH	2.083 μH	2.303 μH	25.91 μH	23.86 μH
LV2						30.46 μH	5.829 μH	6.336 μH	2.303 μH	2.531 μH	28.66 μH	25.91 μH
LV3							30.46 μH	202.30 nH	259.12 nH	286.57 nH	2.530 μH	2.303 μH
LV4								29.07 μH	238.59 nH	259.10 nH	2.303 μH	2.083 μH
LV5									29.07 μH	202.30 nH	6.336 μH	6.841 μH
LV6										30.46 μH	5.829 μH	6.337 μH
LV7											30.46 μH	202.3 nH
LV8												29.07 μH

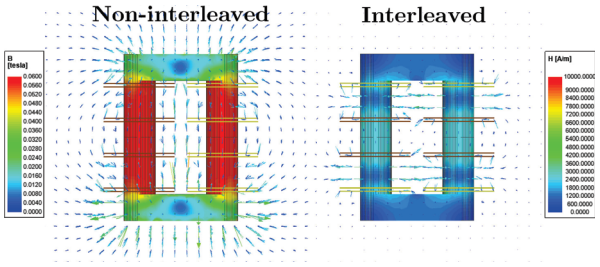

Fig. 18. 3-D FEM simulation of the magnetic field strength and core flux density in the interleaved and noninterleaved winding structures.

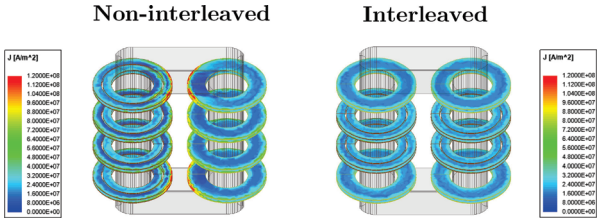

Fig. 19. 3-D FEM simulation of the current density in the PCB windings of the interleaved and noninterleaved winding structures.

vertical flux, which matches the theoretical analysis and the finite element method (FEM) simulation in Fig. 18. The simulated winding loss in the interleaved structure is only 56% of the winding loss in the noninterleaved structure. Since layer-to-layer interleaving is not feasible in an MR-MIMO configuration, one should always interleave the cells to minimize the loss induced by skin and proximity effects.

B. Voltage Balancing and Current Sharing

Another challenge in the multiwinding transformer design is to maintain voltage balancing and current sharing among the series or parallel connected cells. The voltage balancing and current balancing among the cells are determined by the symmetry of the impedance matrix. A symmetric winding impedance matrix would enable automatic voltage balancing and current balancing. As a result, the geometry and the winding configuration of the magnetic structure should be carefully designed to achieve the highest level of symmetry among the cells.

Table II lists the equivalent inductance matrix of the interleaved magnetic structure in Fig. 17. The winding impedance matrix is extracted from FEM simulation and the equivalent inductance is calculated by (3). The elements labeled in gray is the equivalent magnetizing inductance L_{Gi}. The equivalent inductance is related to the "magnetic distance" between two windings. Take cell LV_1 as the example, the equivalent inductance between LV_1 and LV_2 is low and the inductance between LV_1 and LV_7 is high. Power tends to flow between windings that are physically closer to each other (the smaller equivalent inductance).

As shown in Fig. 17, the geometry position of all the HV cells is symmetrical in the interleaved winding structure. Table II also shows that four HV cells in the interleaved structure have symmetrical equivalent inductance between all the LV cells and satisfy the power balancing condition of (7)

$$\begin{aligned} &L_{H1L1} = L_{H2L4} = L_{H3L8} = L_{H4L5} \\ &L_{H1L2} = L_{H2L3} = L_{H3L7} = L_{H4L6} \\ &\cdots \\ &L_{H1L8} = L_{H2L5} = L_{H3L1} = L_{H4L4}. \end{aligned} \tag{23}$$

The equivalent inductances between HV cells are symmetric

$$L_{H1H2} = L_{H3H4}, L_{H1H3} = L_{H2H4}, L_{H1H4} = L_{H2H3}. \tag{24}$$

Similarly, two groups of four LV cells are symmetrical in both geometry and equivalent inductance: 1) LV_1–LV_5–LV_4–LV_8; and 2) LV_2–LV_6–LV_3–LV_7.

In the noninterleaved structure, fewer cells have the symmetrical geometry position and equivalent inductance: HV_1–HV_4, HV_2–HV_3, LV_1–LV_8, LV_2–LV_7, LV_3–LV_6, LV_4–LV_5. That means voltage and current unbalancing will occur in most port configurations of a noninterleaved structure.

The dc–ac cells can be evenly distributed among several ports to ensure voltage balancing and current balancing. Fig. 20 shows three example port configurations with a fully symmetric inductance matrix. Equal power distribution can be guaranteed among these cells with either series or parallel connection in the same port. This design rule can be also applied to the multiwinding structure design for many other magnetic cores such as EE and toroid cores.

VI. EXPERIMENTAL RESULTS

A 500-W prototype with four HV cells and eight LV cells is built and tested. The PCB layout with all components is shown in Fig. 21. Each HV cell is designed to block 72 V and carry 2 A.

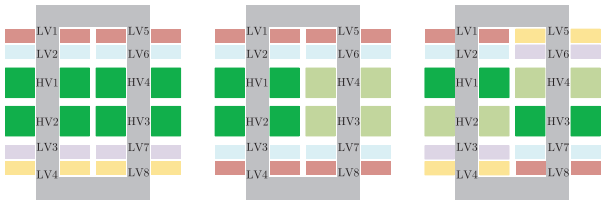

Fig. 20. Three example configurations with symmetric impedance matrix between any two ports in the interleaved winding structure. Cells in the same port are color labeled and can be connected either in series or in parallel.

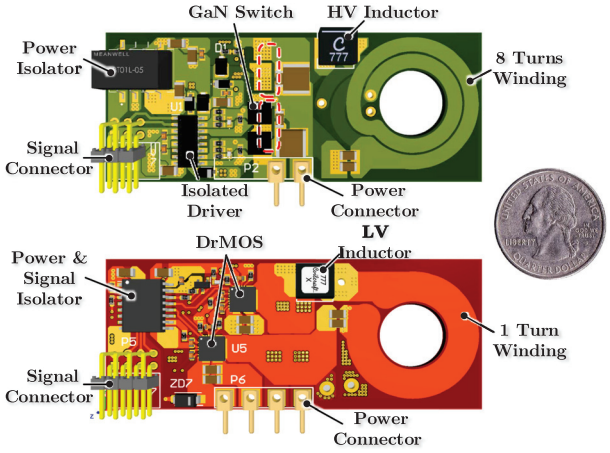

Fig. 21. Annotated view of HV (top) and LV (bottom) cell PCB. The size of each PCB is 74 mm × 30 mm. One HV PCB has one full-bridge cell and one LV PCB has two full-bridge cells.

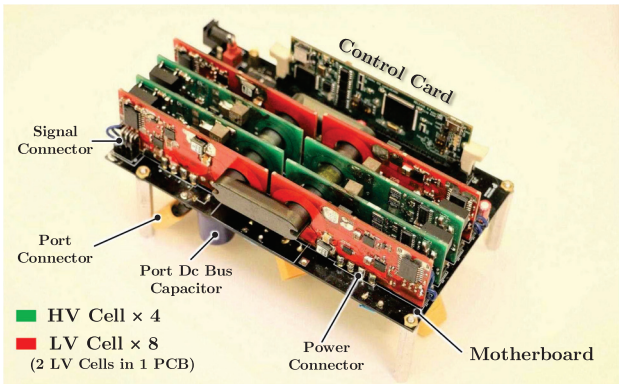

Fig. 22. Physical photograph of the 500-W MR-MIMO prototype.

Each LV cell can block 9 V and carry 7 A. The auxiliary power supply and isolated gate divers are mature solutions with safety voltage up to thousands of volts. The insulation considerations for the MR-MIMO architecture is very similar to those for MMC, which have been proved effective for HV grid-interface applications[36].

Fig. 22 is the physical photograph of the MR-MIMO prototype. Fig. 23 shows a few different ways of configuring the cells, which were tested in the experiment. Four HV cells are connected in series to interface with a 288-V dc bus. In LV port

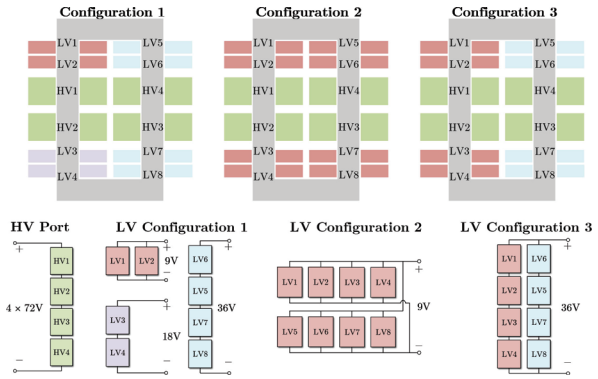

Fig. 23. Three tested configurations of the cells in the MR-MIMO prototype and their corresponding positions in the multiwinding structure: 1) two LV cells in parallel, two LV cells in series, and four LV cells in series; 2) eight LV cells in parallel; and 3) each four LV cells in series, and two series-strings connected in parallel.

configuration 1, two LV cells (LV_1 and LV_2) are connected in parallel to support a 9 V bus with 14 A of current; LV_3 and LV_4 are series-connected as an 18 V/7 A port; LV_5–LV_8 are connected in series as a 36 V/7 A port. LV configuration 1 cannot guarantee symmetrical inductance matrix for LV ports comparing with Fig. 20, however, enables the shortest connecting trace for cells in the same port. Four external capacitors are employed as the bus capacitors of each port (120 μF for the HV port and 1 mF for all the LV ports). In configuration 2, all of the LV cells are reconfigured into a high power 9 V/56 A port with a partially symmetrical inductance matrix (LV_1–LV_4–LV_5–LV_8 and LV_2–LV_3–LV_6–LV_7 are two sets of symmetrical cells but these two sets are asymmetric). In configuration 3, all of the LV cells are reconfigured into a high power 36 V/14 A port with a partially symmetrical impedance matrix. All the port configurations are reconfigurable with the same motherboard.

The operation range of this MR-MIMO prototype can be further extended with different port configurations. The HV port can support current up to 8 A (highest port voltage 72 V) with four HV cells in parallel. The maximum voltage of the LV port is 72 V with eight LV cells connected in series.

Fig. 24 shows the branch inductor current of four HV cells with 288 V input and 9, 18, and 36 V output. The current waveforms are all in phase because all the HV cells are controlled by synchronized gate-driver signals. The current of the HV cells in the interleaved winding structure are more like an ideal trapezoidal waveform than the current in noninterleaved structure (due to the structural symmetry and balanced power distribution).

Fig. 25 shows the thermal images of the magnetic core with the noninterleaved and interleaved winding structures. The thermal images are captured by a thermography camera (FLIR E6) after the converter running for 8 min with output power of 80 W and natural convection cooling. The ambient temperature is 20 °C. The interleaved winding structure has lower core temperature owing to the lower magnetic field strength. The hottest spot is 51.7 °C in the noninterleaved structure and is 45.1 °C in the interleaved structure.

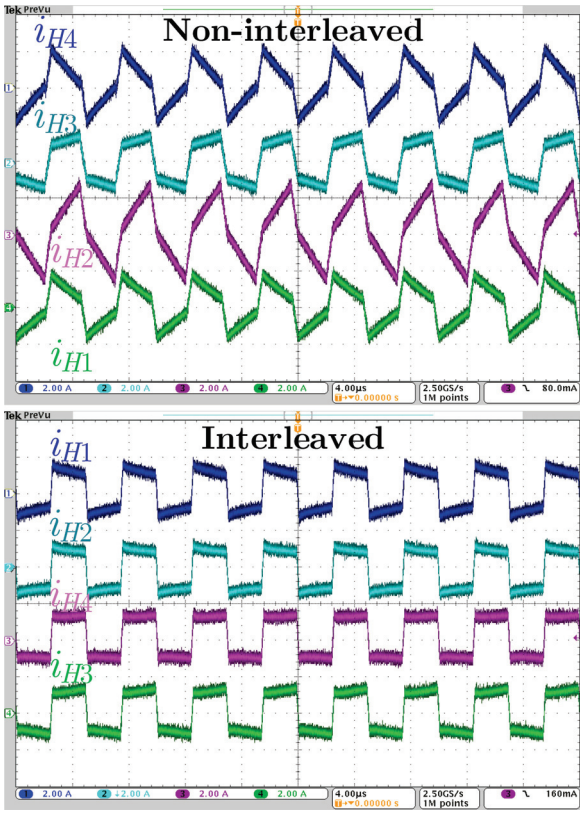

Fig. 24. Measured inductor currents in the four HV cells at an output power of 300 W with noninterleaved and interleaved winding structures. The HV port is the input port and three LV ports connected using configuration 1 (see Fig. 23) are the output ports.

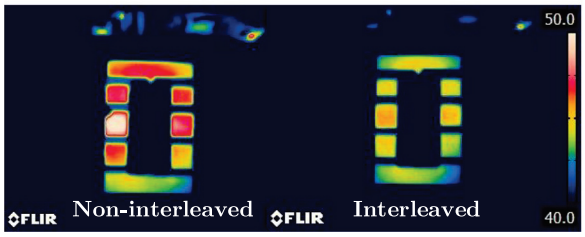

Fig. 25. Thermal images of the core with the interleaved and non-interleaved structures. The output power is 80 W. The ambient temperature is 20 °C.

Fig. 26 shows the measured efficiency of the MR-MIMO converter with the interleaved and noninterleaved winding structures. The input port is the 288 V HV port and three output ports offer 9, 18, and 36 V with configuration 1 in Fig. 23. All LV cells are controlled by the same phase-shift angle. The interleaved structure offers higher system efficiency and power rating because of the balanced power distribution and lower current ripple. The peak system efficiency is 96%. The maximum power that the system can deliver is 500 W. Time-sharing control offers higher efficiency with light load.

Fig. 27 shows the measured power at each LV port. Based on the inductance matrix in Table II and the winding structure in Fig. 23, the relationship of the power of the cells with the same

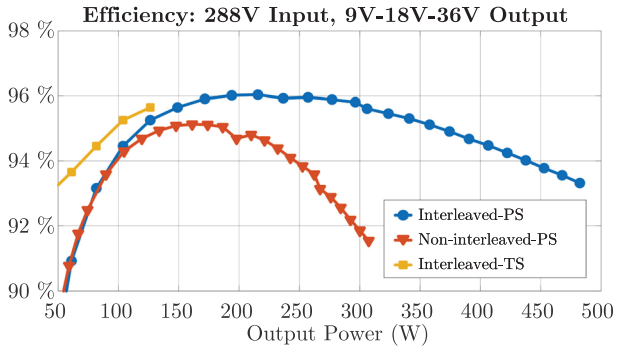

Fig. 26. Measured efficiency of the MR-MIMO prototype with two winding structures and two control strategies: phase-shift (PS) and time-sharing (TS). The output ports are configured into 9, 18, and 36 V (see Fig. 23).

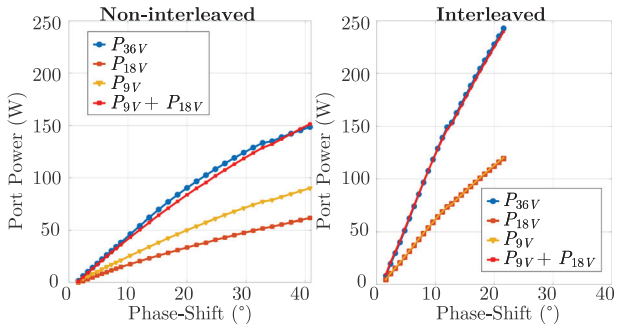

Fig. 27. Measured power delivered by the 9, 18, and 36 V ports. Unbalanced power exists in the non-interleaved structure. Power is well distributed in the interleaved structure due to symmetry.

phase-shift angle in the interleaved windings are

$$P_{\mathrm{LV1}} = P_{\mathrm{LV4}} = P_{\mathrm{LV5}} = P_{\mathrm{LV8}}$$
$$P_{\mathrm{LV2}} = P_{\mathrm{LV3}} = P_{\mathrm{LV6}} = P_{\mathrm{LV7}}$$
$$P_{\mathrm{LV1}} \neq P_{\mathrm{LV2}}. \tag{25}$$

Thus, the relationship of LV port power is: $P_{36\mathrm{V}} = 2P_{9V} = 2P_{18V}$. With port configuration 1, the power of the LV cells in the same PCB is different ($P_{\mathrm{LV1}} \neq P_{\mathrm{LV2}}$) while the total power processed by each LV PCB is equal to each other ($P_{\mathrm{LV1}} + P_{\mathrm{LV2}} = P_{\mathrm{LV3}} + P_{\mathrm{LV4}} + \cdots$). This helps equally distribute the heat among multiple PCBs. The measured port power shown in Fig. 27 matches with this equation and verifies the theoretical analysis for the power distribution.

Similarly, the power of the cells with the same phase-shift angle in a noninterleaved winding structure (see Fig. 17) are

$$P_{\mathrm{LV1}} = P_{\mathrm{LV8}}, P_{\mathrm{LV2}} = P_{\mathrm{LV7}}$$
$$P_{\mathrm{LV3}} = P_{\mathrm{LV6}}, P_{\mathrm{LV4}} = P_{\mathrm{LV5}}$$
$$P_{\mathrm{LV1}} \neq P_{\mathrm{LV2}} \neq P_{\mathrm{LV3}} \neq P_{\mathrm{LV4}}. \tag{26}$$

The port power $P_{18\mathrm{V}}$ and $P_{9\mathrm{V}}$ are no longer equal, but $P_{36\mathrm{V}}$ still equals $P_{9\mathrm{V}} + P_{18\mathrm{V}}$ in the noninterleaved case. The measured port power also matches this relationship. The two winding structures with the same phase-shift angle deliver different

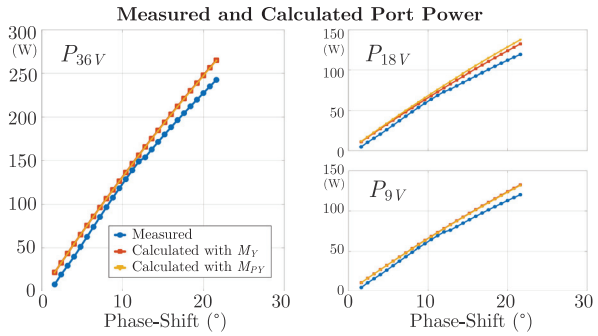

Fig. 28. Measured and calculated power of the 9, 18, and 36 V ports in the interleaved structure. The port power is calculated by (4) with the 12×12 admittance matrix $\boldsymbol{M_Y}$ and the reduced-order 4×4 matrix $\boldsymbol{M_{PY}}$. The calculation results of both two methods match the measured port power. The effectiveness of the reduced order approach is verified.

power in the two cases. This is because the noninterleaved winding structure has higher equivalent cell-to-cell inductance than the interleaved winding structure (verified by FEM simulations).

The port power measurement also verifies the effectiveness of the matrix reduction method introduced in Section IV. The port power can be calculated either by (4) with the original 12×12 admittance matrix $\boldsymbol{M_Y}$ or by the reduced-order 4×4 matrix $\boldsymbol{M_{PY}}$. The calculation results of these two methods are presented together with the experiment results in Fig. 28. The calculation results from the reduced-order matrix $\boldsymbol{M_{PY}}$ matches the results from the original admittance matrix $\boldsymbol{M_Y}$ and the experiment results. The calculated port power is slightly higher than the measured power owing to the circulating power loss that is not captured by the model.

The power comparison in Fig. 28 indicates that the power level of the MR-MIMO architecture is linearly extendable by increasing the quantity of the series/parallel cells as long as the magnetic winding structure is symmetric enough and the coupling coefficient is high.

Fig. 29 shows the measured inductor current waveforms of four LV cells with the three output port configurations in Fig. 23. In port configuration 1, the bus voltages of LV_1 and LV_2 are clamped to the port voltage and regulated to 9 V. There is no circulating current between them. The current waveform of i_{L2} is close to an ideal trapezoidal current. The voltage of the 18 V port and the 36 V port are regulated; however, the voltage within each individual cell is not regulated. $P_{\mathrm{LV3}} \neq P_{\mathrm{LV4}}$ in the 18 V port and $P_{\mathrm{LV5}} \neq P_{\mathrm{LV7}}$ in the 36 V port. The unbalanced power leads to unbalanced voltage for series-connected cells and further results in high peak current due to the circulating current between multiple cells in the same port. In the case of port configuration 2, all the LV cells are parallel-connected and all their bus voltages are equal. There is no circulating current among them. In port configuration 3, voltage unbalancing still exists among the LV cells since none of them are individually regulated. The current ripple is also high.

Fig. 30 compares the efficiency of the three output port configurations with phase-shift control. Port configuration 2 achieves the highest efficiency, especially with higher output power,

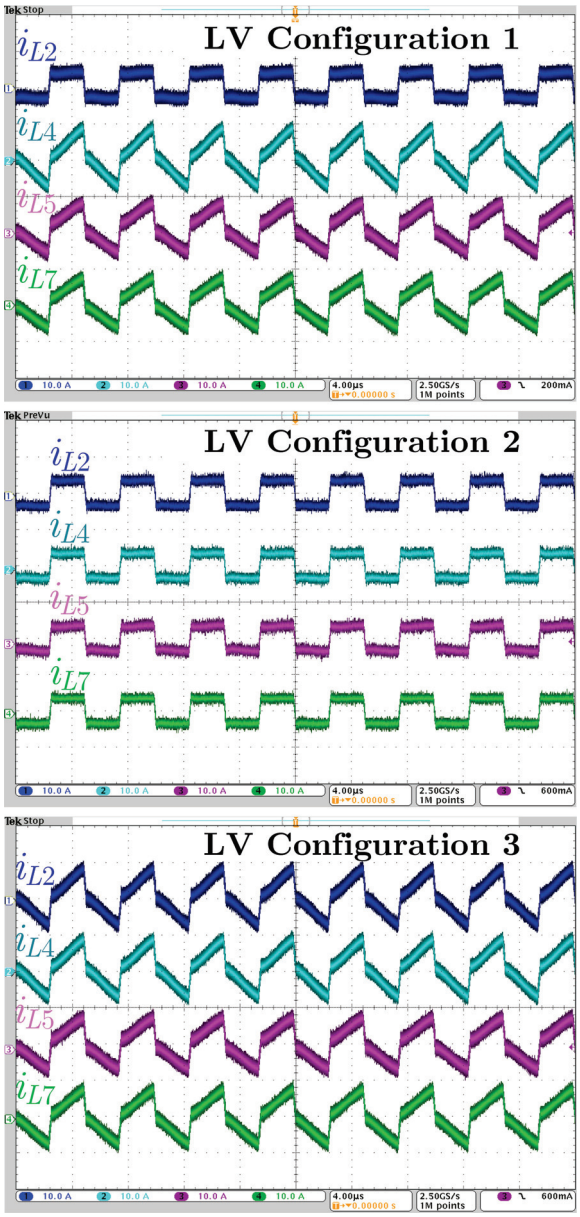

Fig. 29. Measured inductor currents of the four LV cells at an output power of 300 W with interleaved winding structure. HV port is the input port. The output ports are 9, 18, and 36 V with port configuration 1.

because of the well-balanced port voltage and lower current amplitudes. The maximum efficiency of port configuration 2 is 96.7% with an output power of 300 W. Port configuration 3 has the lowest efficiency because all the LV inductor currents have high peak-to-peak ripple.

Fig. 31 shows the thermal image of the MR-MIMO converter when it is configured as one HV input and three LV outputs (configuration 1). The image is captured after 20 min operating with an output power of 500 W. A left to right 21.9 cubic feet per minute (CFM) air flow is applied. The temperature of the prototype is below 45°C. The hottest components are the HV external inductors and the LV DrMOS. Since power is processed in a distributed manner in the MR-MIMO architecture, heat is

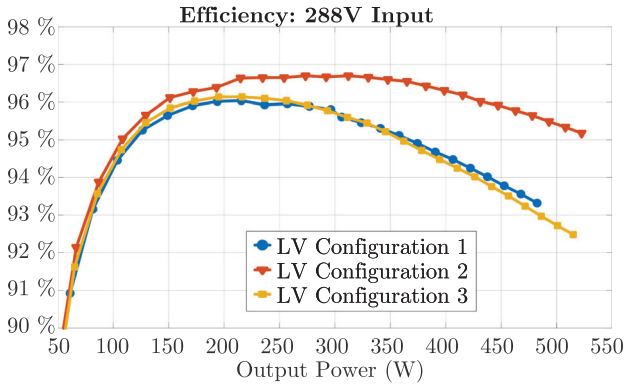

Fig. 30. Measured efficiency of the three output port configurations with phase-shift control. The 288 V HV port is the input port. LV port configuration 2 achieved the highest efficiency because of the highest symmetry.

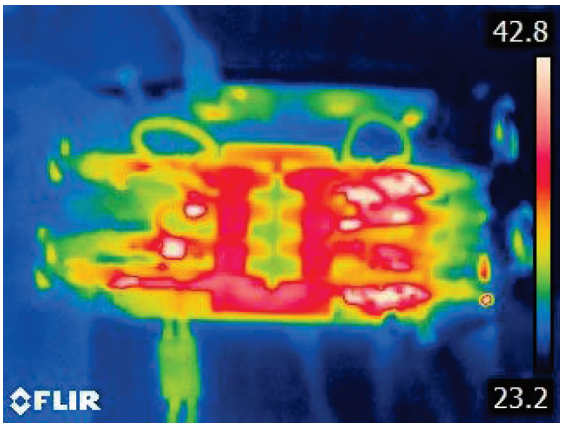

Fig. 31. Thermal image of the MR-MIMO converter with $P_o = 500$ W. The output ports are 9, 18, and 36 V with port configuration 1. The airflow is 21.9 CFM from left to right with a 23 ° C ambient temperature.

naturally distributed and no additional heat sink is needed, which helps to improve the power density.

To demonstrate the MIMO energy router functions, the cells are reconnected: two HV cells (HV_3 and HV_4) are connected in parallel as a 72 V input port. The other LV cells are connected as port configuration 1 and the 36 V port is configured as the second input port. Fig. 32 shows the measured efficiency contour of the MR-MIMO prototype across a wide operation range. The 18 V port and 9 V port are controlled by the same phase-shift angle to provide the same output power. The input power of the 72 V port and the 36 V port are controlled separately with two phase-shift angles. The efficiency remains constant while shifting the power from input to another. The maximum efficiency is over 95% and the MIMO efficiency is higher than 94% across a wide range.

Fig. 33 shows the open-loop transient response of the system to a step change of phase-shift angle in one output port. The phase-shift step change on one output port triggers the power change on both output ports because the power flow between them is also changed. It takes about 25 ms for the open-loop system to reach to a new steady state. Fig. 34 shows the close-loop transient response of the system to a 2 A load step change.

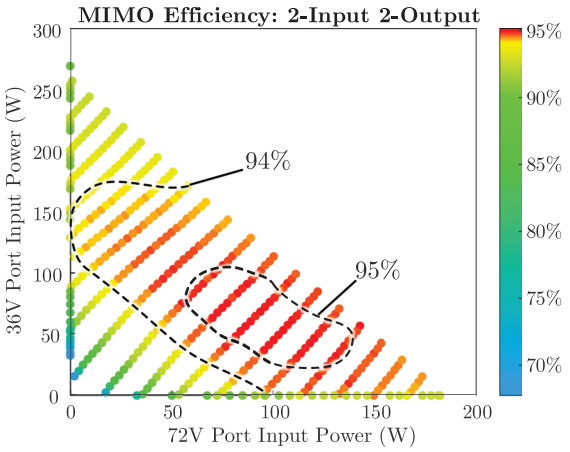

Fig. 32. Measured efficiency of the MR-MIMO prototype with two input ports (72 and 36 V) and two output ports (18 and 9 V). HV_3 and HV_4 are connected in parallel as the 72 V input port, HV_1 and HV_2 are removed.

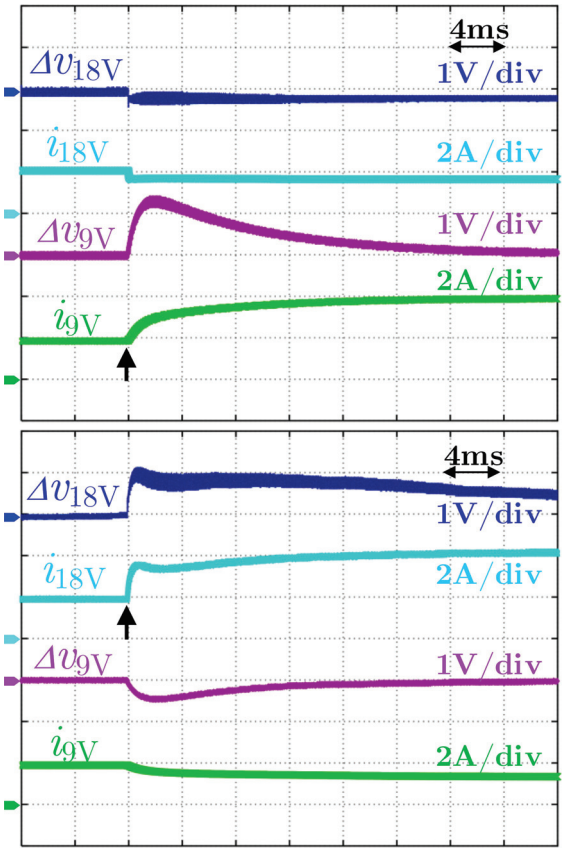

Fig. 33. Open-loop transient waveforms of port voltage ripples and port currents during step change on the phase-shift angle of the 9 V port and 18 V port. The 72 V port and 36 V port are the input ports and the 18 V port and 9 V port are the output ports.

The voltages of 9 V port and 18 V port are regulated by the distributed phase-shift control, as shown in Fig. 14. When any output port faces a load step change, voltage fluctuations occur simultaneously on both output ports because the power flows of all ports are coupled by the multiwinding transformer. The

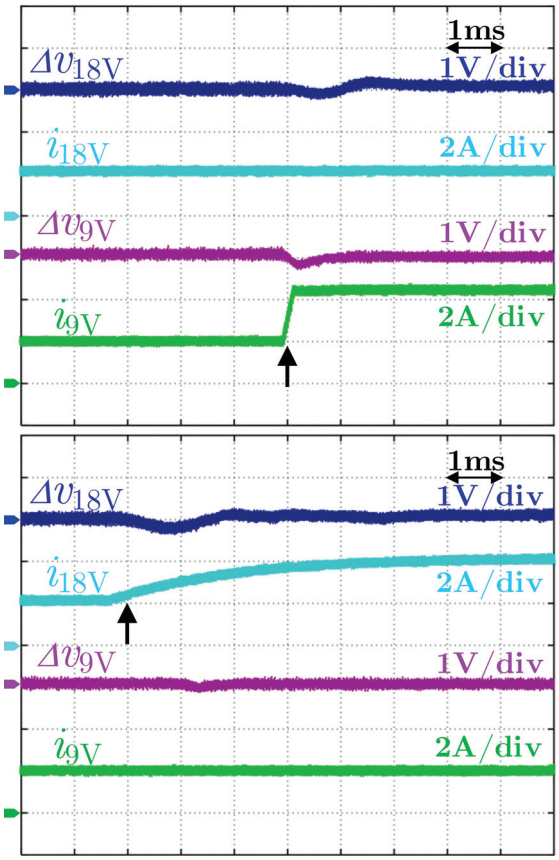

Fig. 34. Close-loop transient waveforms of port voltage ripples and port currents during load current step change on the 9 V port and 18 V port. The input/output port configuration is the same as Fig. 33. The electronic loads of two output ports have different dynamic slope.

port voltages recover in less than 2 ms with a ripple below 0.4 V. Other control strategies with power decoupling algorithms [9], [17], [32] also provide fast dynamic response. With hybrid time-sharing and phase-shift control, the MR-MIMO architecture is capable of performing power flow modulation and voltage regulation simultaneously.

VII. Conclusion

This article presents an MR-MIMO architecture for multiport ac-coupled dc energy routers. The key contributions of this article include: 1) a multicell reconfigurable 12-winding multiport ac-coupled MIMO converter maintaining high performance across a wide range; 2) a hybrid time-sharing and phase-shift control strategy; and 3) a systematic method of designing multiwinding planar transformers. The MR-MIMO architecture is highly modular and is linearly extendable. It offers a simple control interface, lower power conversion stress, and reconfigurable input/output capability. We performed power flow analysis on the multiwinding transformer, developed a matrix-reduction method to reduce the control complexity, and built a four-port prototype with 12 cells and a variety of configurations. The MIMO magnetic structure with a large number of coupled windings is investigated and optimized to achieve high efficiency and balanced power sharing. The prototype maintains over 95% efficiency and good current balancing across a wide operation range, and can be reconfigured and extended to cover a variety of voltage conversion ratios.

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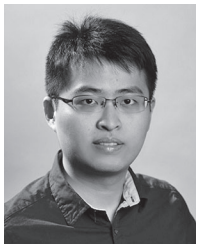

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