Performance Limits of Differential Power Processing

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***Abstract*—This paper explores performance limits of differential power processing (DPP) for large-scale modular dc energy systems with stochastic loads. An analytical stochastic model is developed to estimate the average power loss of a DPP topology under probabilistic load distributions. A scaling factor $\mathcal{S}(\bullet)$ is introduced to describe how power loss scales as the system size or load power variance increases. The average power losses of several example DPP topologies are analyzed and compared against conventional dc-dc converters given the same total switch die area and magnetic volume. The performance limits for various DPP topologies are derived and verified by Monte-Carlo simulations in SPICE, and the results indicate that the ac-coupled DPP converter stands out from all the representative DPP topologies discussed here in terms of the lowest power loss. The paper provides an analytical framework to evaluate the performance of different DPP topologies in a methodical way, offering insights for the design of DPP systems with large-scale stochastic loads.**

***Index Terms*—Differential power processing (DPP), stochastic models, dc-dc converters, performance limits**

I. Introduction

Differential power processing (DPP) has been effectively implemented in many applications, including solar photovoltaics, battery management systems, and servers in data centers [1]–[10]. In these systems, numerous loads or sources are connected in series, with a set of series voltage domains. Each voltage domain usually comprises many parallel units, resulting in a large-scale modular load array as shown in Fig. 1. A DPP converter operates to process power differences between the voltage domains. This differential power should be a small fraction of the total load power, so the overall power conversion is greatly reduced and the energy efficiency of DPP-based dc energy systems can improve substantially.

In a general DPP system, the power of each load changes with time as a random process. In this situation, the performance of a DPP converter is closely related to power variance among voltage domains. Previous work has been done to analyze how the performance of DPP converters changes as load power distribution changes, mainly based on numerical simulations [2], [3]. Also, a DPP system usually comprises more switches and magnetic components than in a conventional dc-dc converter system. A rigorous analytical method that evaluates DPP performance and cost when supporting stochastic loads and systematically compares various DPP topologies with conventional N:1 dc-dc converters is needed.

Based on a stochastic modeling approach, this paper explores performance limits of DPP. A performance scaling factor, $\mathcal{S}(\bullet)$, is introduced to describe the change in power loss in a DPP system as the system size or the load power variance increases. A stochastic loss model that describes the average power loss of a DPP converter when supporting a large array of stochastic loads is developed. The model employs a minimum set of assumptions and offers rich design insights. Several representative DPP topologies are analyzed and compared with an N:1 dual-active-bridge (DAB) dc-dc converter given the same total switch die area and magnetic core size. The performance limits and stochastic loss model of various DPP topologies are verified with Monte-Carlo simulations in SPICE. In this work, the ac-coupled DPP converter stands out from others in terms of the lowest average power loss.

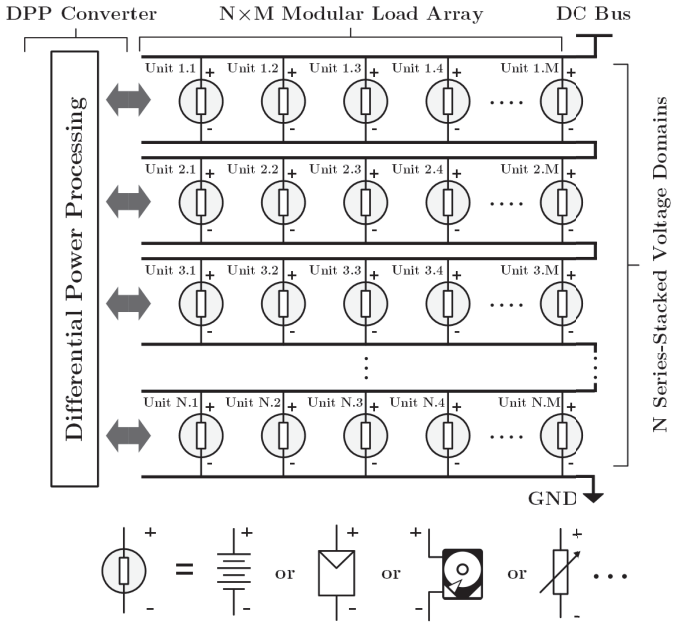

Fig. 1. An $N \times M$ differential power processing system with N series-stacked voltage domains, each comprising M modular loads. The modular load units can be battery cells, PV panels, hard disk drives (HDD), etc.

This paper provides an analytical framework for performance limit evaluation of DPP systems, offering useful design guidelines to select a DPP topology for a given application with a probabilistic load profile. Section II introduces a stochastic modeling approach for two typical DPP architectures. Based on the stochastic loss model, Section III compares several example circuit implementations of the two DPP architectures against an N:1 DAB converter. Simplified

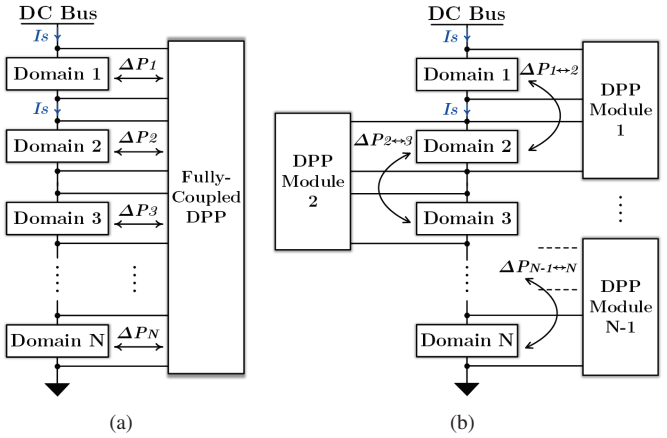

Fig. 2. Typical DPP architectures: (a) fully-coupled DPP; (b) ladder DPP.

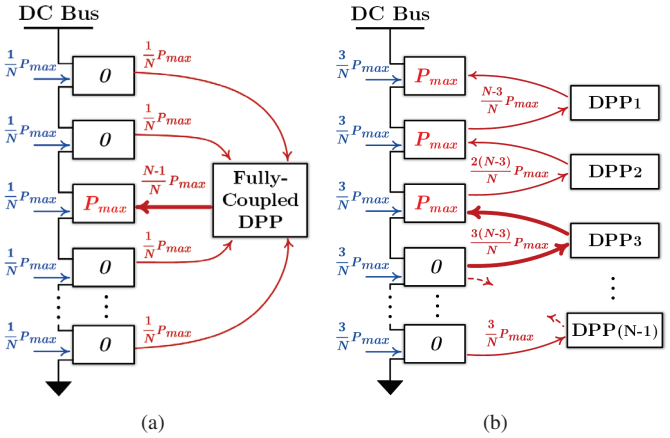

Fig. 3. Example load conditions which require the maximum instantaneous differential power at the 3^{rd} port/submodule of the DPP stack from the top: (a) fully-coupled DPP; (b) ladder DPP. Power injected from the series voltage domains are labeled in blue, and the differential power are labeled in red.

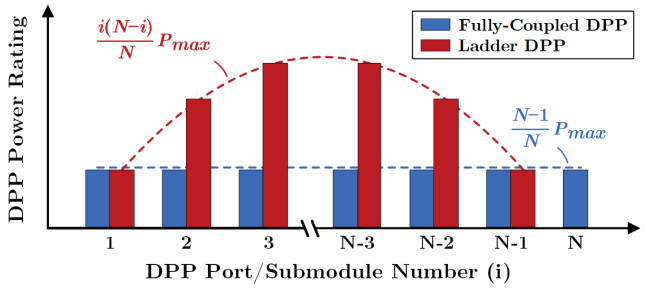

Fig. 4. Maximum differential power rating of the i^{th} port or submodule in a fully-coupled DPP converter and a ladder DPP converter with N series-stacked voltage domains.

circuit models are developed to quantify the loss analysis. The performance limits of different DPP topologies are derived and verified by Monte Carlo simulations in Section IV. Finally, Section V concludes this paper.

II. Stochastic Loss Model for DPP

Fig. 1 shows an overview of a typical DPP system. An $N \times M$ modular array of stochastic loads is configured in N series-stacked voltage domains. Each voltage domain comprises M modular loads connected in parallel. For a case with matched domain voltages, let the voltage of each domain be V_0. The instantaneous power of the j^{th} load in the i^{th} voltage domain is $P_{ij}(t)$. All $P_{ij}(t)$'s ($i = 1, ..., N; j = 1, ..., M$) are taken as statistically *independent* and *identically distributed* (i.i.d.) random variables, so the load power mean value $\mu(P_{ij}(t))$ and variance $\sigma^2(P_{ij}(t))$ are identical for all load units (denoted as μ and σ^2 for short). The total power consumed by the i^{th} voltage domain is the sum of M random load powers: $P_i(t) = P_{i1}(t) + P_{i2}(t) + ... + P_{iM}(t)$, so the power levels $P_i(t)$ of the N voltage domains are also independent. A DPP converter is utilized to process differential power among the N series voltage domains, in this case seeking to balance the voltage of each domain. A more general case allows various voltages (as when each domain has its own power droop characteristics), but matched voltages are explored here for clarity.

A. Fully Coupled DPP and Ladder DPP

Various DPP topologies have been explored, with design tradeoffs in efficiency, size, cost, and control complexity [1]–[10]. They can be generally classified into two typical categories as shown in Fig. 2. Fig. 2a depicts the architecture of a fully-coupled DPP converter system, in which all voltage domains are coupled by the DPP converter circuitry. A typical fully-coupled DPP converter functions as a multiport dc-dc converter, and there is a direct power flow path between any two voltage domains. Due to the series architecture, the same current $I_s(t) = \sum_{k=1}^{N} P_k(t)/NV_0$ flows through each voltage domain. The instantaneous differential power processed by a fully-coupled DPP system for the i^{th} voltage domain is

$$\Delta P_i(t) = I_s(t)V_0 - P_i(t) = \overline{P}(t) - P_i(t). \quad (1)$$

Here $\overline{P}(t)$ is the average power consumption of all voltage domains. Equation (1) indicates that in a fully-coupled DPP converter, the differential power processed at each port is symmetric, so the differential power rating and the average power loss of each DPP port are the same.

Fig. 2b shows the architecture of a domain-to-domain or ladder DPP system, in which multiple standalone dc-dc converters (termed *DPP submodules*) are used to connect neighboring voltage domains. The differential power processed in one voltage domain is related to multiple DPP submodules,

$$P_i(t) + \Delta P_{i\leftrightarrow i+1}(t) - \Delta P_{i-1\leftrightarrow i}(t) = I_s(t)V_0 = \overline{P}(t), \quad (2)$$

where $\Delta P_{i\leftrightarrow i+1}(t)$ is the differential power that the i^{th} DPP submodule delivers from the i^{th} domain to the $(i+1)^{th}$ domain ($\Delta P_{i\leftrightarrow i+1}(t) = 0$, if $i = 0$ or N). Reorganizing (2),

$$\Delta P_{i\leftrightarrow i+1}(t) = \sum_{k=1}^{i}(\overline{P}(t) - P_k(t)) = i\times\overline{P}(t) - \sum_{k=1}^{i} P_k(t). \quad (3)$$

In a ladder DPP converter, there is no direct power flow between two non-neighboring voltage domains. Differential power must go through multiple DPP submodules from a domain to non-neighboring domains, resulting in differential

power accumulation — each DPP submodule needs to process both the power difference between $P_i(t)$ and $\overline{P}(t)$ and the accumulated differential power from other DPP submodules as indicated in (2). This causes additional power to be processed in a ladder DPP converter compared to that of a fully-coupled DPP converter. Eq. (3) also reflects that the differential power processed by each DPP submodule is unsymmetric. Thus, both the power ratings and the average power loss vary among DPP submodules in a ladder configuration.

Assume that the power consumption of each voltage domain $P_i(t)$ is within a range $[0, P_{max}]$. Fig. 3 shows example load conditions and detailed power flow when the maximum instantaneous differential power is reached at a specific port or submodule in a fully-coupled DPP and a ladder DPP converter. In the fully-coupled DPP converter, the maximum instantaneous differential power processed by the i^{th} port is reached when the i^{th} domain consumes full load power and the other domains have no load or when the i^{th} domain has no load and the others consume full load power. The maximum is $\frac{N-1}{N}P_{max}$, which is identical for all the ports in the fully-coupled DPP converter. For a ladder DPP converter, the maximum differential power processed by the i^{th} submodule is reached when top i domains (i.e., domain $1 \sim i$) consume full load power and all the other domains have no load or top i domains have no load and all the other domains consume full power. The maximum is $\frac{i(N-i)}{N}P_{max}$, which is varied with different DPP submodules. Fig. 4 shows the maximum differential power rating of each port or submodule in a fully-coupled DPP converter and in a ladder DPP converter. The maximum power rating requirement for a ladder DPP submodule increases if it is closer to the middle of the series-stacked voltage domains. In most cases, the power rating of a ladder DPP submodule is larger than that of each port in a fully-coupled DPP system.

B. Stochastic Loss Model and Scaling Factor

In a DPP system with a modular load array, the dimensions of the load array and the load power variation impact the differential power to be processed. To quantify the performance of a DPP system as the size of load array or variance of load power scales up, a stochastic loss model can be developed. The power losses of fully-coupled and ladder DPP architectures are derived as a function of the processed differential power, i.e., $\Delta P_i(t)$ or $\Delta P_{i\leftrightarrow i+1}(t)$. Since the power loss is a time-dependent random variable, its expected value $\mathbb{E}[\bullet]$ is used to evaluate the long-term average power loss of the DPP system. For comparison, a stochastic loss model is derived for a conventional N:1 dc-dc converter based on the total load power $\sum_{i=1}^{N} P_i(t)$.

Fig. 5 shows equivalent circuit models of various DPP architectures and of the N:1 dc-dc converter. In the developed stochastic loss model, only conduction loss is considered and is captured by an effective output resistance in Fig. 5. Switching loss, core loss, and other non-ideal effects can be added to enhance accuracy, but the model procedure follows from that presented below.

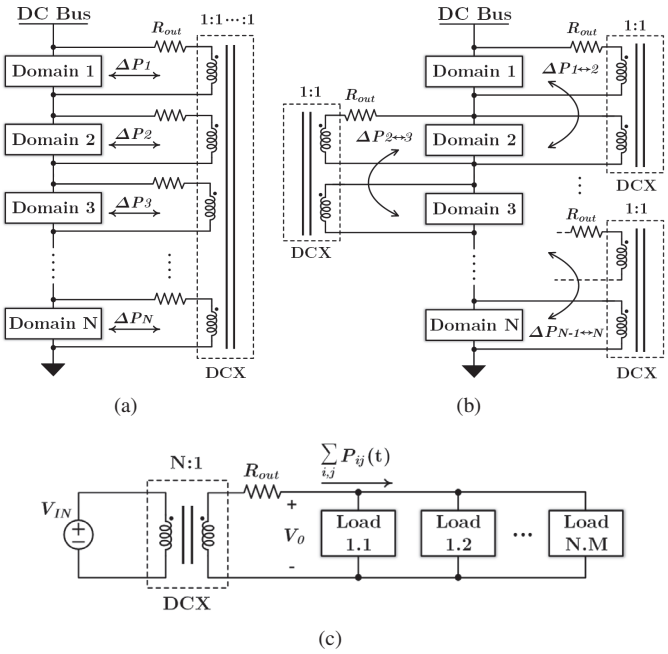

Fig. 5. Equivalent circuit model for loss estimation of: (a) fully-coupled DPP; (b) ladder DPP; (c) conventional N:1 dc-dc converter.

- *Fully-Coupled DPP Converter:* As illustrated in Fig. 5a, a fully-coupled DPP topology can be modeled as an N-port network with all ports connected to an N-winding ideal transformer with uniform turns ratios. The conduction loss in each port is captured by an equivalent output resistance R_{out} located at each port as labeled in Fig. 5a. Considering linear scalability of this DPP architecture, each port is assumed to be identical with the same R_{out}. In a fully-coupled DPP converter, the i^{th} port is processing $\Delta P_i(t)$. The instantaneous conduction loss and average conduction loss at the i^{th} port are

$$\begin{aligned} P_{loss.i}(t) &= \Delta I_i(t)^2 R_{out} = \left(\frac{\Delta P_i(t)}{V_0}\right)^2 R_{out} \\ &= R_{out}\left(\frac{\overline{P}(t) - P_i(t)}{V_0}\right)^2, \end{aligned} \tag{4}$$

$$\mathbb{E}[P_{loss.i}(t)] = \frac{M(N-1)R_{out}}{NV_0^2}\sigma^2(P_{ij}(t)). \tag{5}$$

Here $\sigma^2(P_{ij}(t))$ is the variance of P_{ij}. Eqs. (4) and (5) indicate that the average processed differential power and the conduction loss are identical at each port in a fully-coupled DPP converter. The expected value of the total conduction loss for the entire fully-coupled DPP system is

$$\begin{aligned} \mathbb{E}[P_{loss}(t)] &= \sum_{i=1}^{N} \mathbb{E}[P_{loss.i}(t)] \\ &= M(N-1)\sigma^2(P_{ij}(t)) \times \frac{R_{out}}{V_0^2} \Rightarrow \underbrace{\mathcal{S}(MN\sigma^2)}_{scaling\ factor}. \end{aligned} \tag{6}$$

We use symbol $\mathcal{S}(\bullet)$ to represent the performance scaling factor of a DPP system, which illustrates the growth rate of

the loss as the dimension of the DPP system or variance of load power increases. Eq. (6) indicates that the performance scaling factor of an $N \times M$ fully-coupled DPP system is $\mathcal{S}(MN\sigma^2)$. The expected conduction loss of a fully-coupled DPP converter is determined by the variance σ^2 of the stochastic loads, and scales linearly with N and M. It is independent of the average load power μ.

- *Ladder DPP Converter:* In a ladder DPP topology, each DPP submodule is a bidirectional dc-dc converter. Each can be modeled as an 1:1 ideal transformer with an output resistance R_{out} to capture its conduction loss, as illustrated in Fig. 5b. The i^{th} DPP submodule is processing a differential power of $\Delta P_{i\leftrightarrow i+1}(t)$. The instantaneous and average conduction loss of the i^{th} submodule are

$$P_{loss.i}(t) = R_{out}\Delta I_{i\leftrightarrow i+1}(t)^2 = R_{out}\left(\frac{\Delta P_{i\leftrightarrow i+1}(t)}{V_0}\right)^2 = R_{out}\left(\frac{i\times\overline{P}(t) - \sum_{k=1}^{i} P_k(t)}{V_0}\right)^2, \tag{7}$$

$$\mathbb{E}[P_{loss.i}(t)] = \left(i - \frac{i^2}{N}\right) M\sigma^2(P_{ij}(t)). \tag{8}$$

Eqs. (7) and (8) indicate that the average processed differential power and power loss differ among the DPP submodules. The submodules located closer to the middle of the series-stacked voltage domains tend to process more power and generate more loss, similar to the maximum differential power rating in Fig. 4. The total average conduction loss of the entire ladder DPP system is

$$\mathbb{E}[P_{loss}(t)] = \sum_{i=1}^{N-1}\mathbb{E}[P_{loss.i}(t)] = \frac{M(N-1)(N+1)}{6}\sigma^2 \times \frac{R_{out}}{V_0^2} \Rightarrow \underbrace{\mathcal{S}(MN^2\sigma^2)}_{scaling\ \ factor}. \tag{9}$$

As shown in Eq. (9), the conduction loss of a ladder DPP increases linearly with M, and quadratically with N, so the performance scaling factor of a ladder DPP system with an $N \times M$ stochastic load array is $\mathcal{S}(MN^2\sigma^2)$. Compared to a fully-coupled DPP converter, the conduction loss of a ladder DPP converter has a higher loss scaling factor as N increases because differential power accumulates along the series-stacked voltage domains. The expected loss of a ladder DPP topology is linked to the variance (σ^2) of the individual loads. Loss scales linearly with M, scales quadratically with N, and is independent of the average load power μ.

- *Conventional N:1 Dc-Dc Converter:* To compare the performance of DPP solutions against conventional step-down converter, a stochastic loss model for a conventional N:1 dc-dc converter can be derived. This converter can be modeled as an N:1 ideal transformer with an output resistance R_{out} [11], as shown in Fig. 5c. All loads are connected in parallel at the output, and the full power of the $N \times M$ load array must be processed. The conduction loss of this converter when processing power for $N \times M$ loads is

$$\mathbb{E}[P_{loss}(t)] = \mathbb{E}[R_{out}I_{out}^2(t)] = \frac{R_{out}}{V_0^2}\cdot\mathbb{E}\left[\left(\sum_{i=1}^{n} P_i(t)\right)^2\right] = \left(MN\sigma^2(P_{ij}(t)) + M^2N^2\mu^2(P_{ij}(t))\right)\times\frac{R_{out}}{V_0^2} \Rightarrow \underbrace{\mathcal{S}(M^2N^2\mu^2)}_{scaling\ \ factor}, \tag{10}$$

where $\mu(P_{ij}(t))$ is the average power of each load. The expected conduction loss of a conventional N:1 dc-dc converter is mainly determined by the total average load power ($MN\mu$), and it scales quadratically with N and M. Eq. (6) and (9) reveal that the average conduction loss of DPP architectures is independent of the average power μ, and determined by the load variance σ^2. This is consistent with the fundamental benefit of DPP solutions: the loss of a DPP system is only determined by differential power, and this is only a fraction of the total load power. If the module load power values are uniform with $\sigma = 0$, a DPP system imposes no conduction loss.

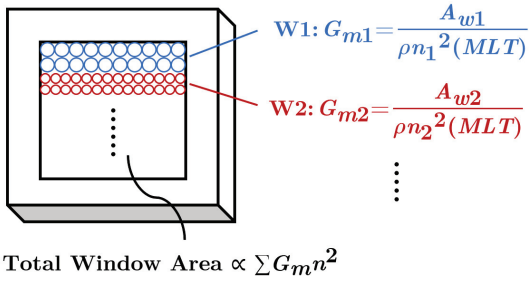

Fig. 6. Magnetic core window area distribution and winding conductance. Total core window area is proportional to $\sum G_m n^2$. n is the effective number of turns in each winding; ρ is the winding resistivity; MLT is the mean length per turn and is assumed to be identical for all the windings.

III. Simplified Circuit Model for Loss Analysis

In a DPP architecture, total switch count and magnetic component volume increase as the number of voltage domains (N) increases. A reasonable comparison between DPP converters and a conventional N:1 dc-dc converter would be to compare their performance given the same size and volume. In this section, several DPP topologies are analyzed and compared with an N:1 dual-active-bridge (DAB) converter with the following assumptions:

1) *Identical Total Semiconductor Die Area:* For both discrete and integrated switches, semiconductor die area scales linearly with the $G_{sw}V_{sw}^X$ product [12]. G_{sw} is the switch conductance; V_{sw} is the switch blocking voltage; the coefficient X, typically 2, depends on material and process. We represent the total semiconductor die area as the sum of $G_{sw}V_{sw}^2$ for all switches: $\sum G_{sw}V_{sw}^2$, which is required to be identical for all topologies compared here and is normalized to $G_{SW}V_0^2$.

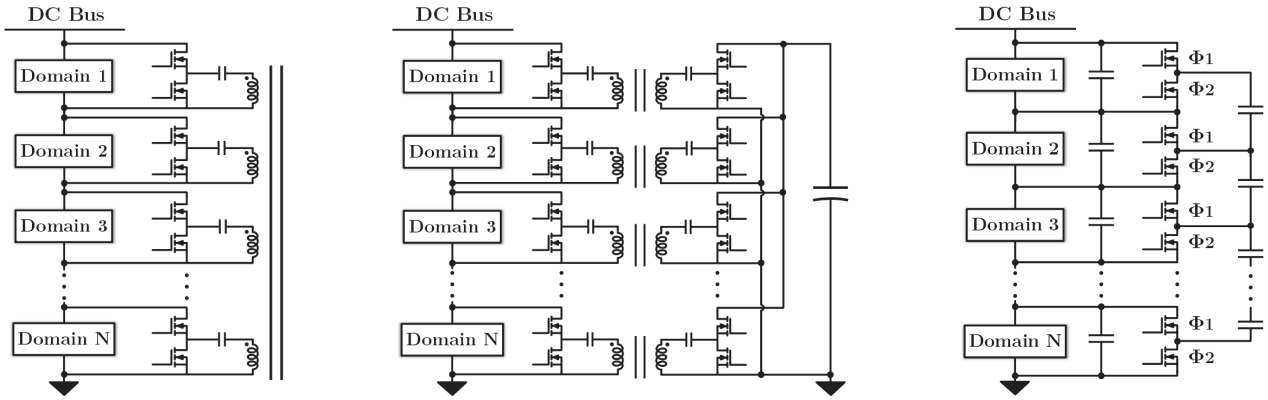

Fig. 7. Fully-coupled DPP topologies: (a) ac fully-coupled DPP [8]; (b) dc fully-coupled DPP [9]; (c) switched-capacitor (SC) based DPP [4], [10].

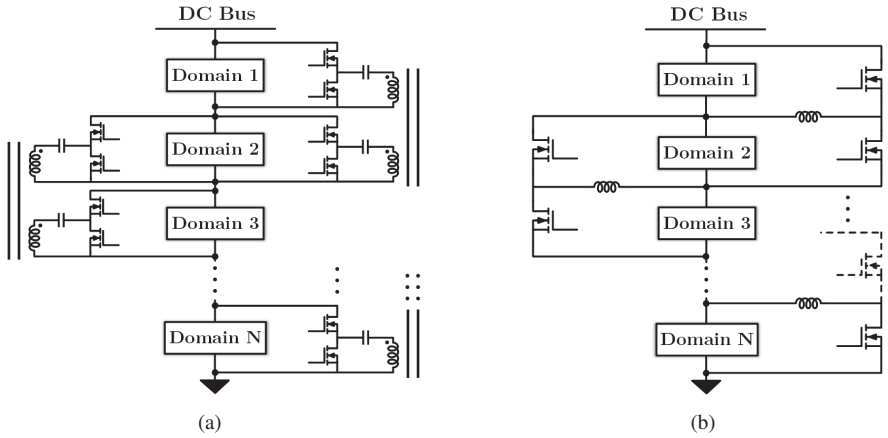

Fig. 8. Example topologies of the ladder DPP architecture: (a) ladder DPP with DAB cells; (b) ladder DPP with buck-boost cells [5], [6].

2) *Identical Total Winding Area:* The magnetic component size depends on the winding area and cross-sectional area of the core. In this paper, the total volume of magnetic components is evaluated using the total winding area, which can be estimated by the magnetic core window area (assuming a fixed filling factor for each winding). As illustrated in Fig. 6, the distributed window area of each winding is proportional to $G_m n^2$. G_m is the conductance of each winding; n is the effective number of series turns (parallel turns can be equivalent to one turn in terms of dc resistance), and each winding is assumed to have the same volt-second-per-turn value. The total magnetic core window area is represented as the sum of $G_m n^2$ over all the windings. $\sum G_m n^2$ is required to be identical for all topologies compared here that contain magnetic components and is normalized to G_M.

Based on these two assumptions, output resistance R_{out} and performance limits of various DPP topologies were derived and verified by Monte Carlo simulations in SPICE.

Figs. 7 and 8 exhibit several typical circuit implementations of a fully-coupled DPP architecture and a ladder DPP architecture, respectively. To model the output resistance R_{out} as defined in Fig. 5, the $R_{ds(on)}$ of each switch and winding dc resistance are included in a unified equivalent.

Fig. 7a shows an ac fully-coupled DPP converter in which all voltage domains are ac-coupled to a multiwinding transformer through half-bridge circuits. In applications with N series-stacked voltage domains, an ac fully-coupled DPP comprises $2N$ switches with identical voltage rating V_0 and N windings with identical turns ratio (the effective number of turns of each winding can be set to one). Therefore, the resistance of each switch and each winding are $\frac{2N}{G_{SW}}$ and $\frac{N}{G_M}$. Port-to-port power is transferred in the same way as in a DAB converter [8]. The conduction loss generated at the i^{th} port is

$$P_{loss.i} = (2\Delta I_i)^2 \times \left(\frac{2N}{G_{SW}} + \frac{N}{G_M}\right) = \Delta I_i^2 R_{out} \qquad (11)$$

Based on (11), the output resistance of each port in an ac fully-coupled DPP is $\frac{8N}{G_{SW}} + \frac{4N}{G_M}$. Similarly, the output resistance of a dc fully-coupled DPP as in Fig. 7b can be obtained as $\frac{32N}{G_{SW}} + \frac{16N}{G_M}$, which is four times of that in the ac fully-coupled DPP due to doubling of switch and winding counts and doubling of "dc-ac-dc" differential power conversion stages [8]. A switched-capacitor DPP system (in Fig. 7c) has the same switch count and switch voltage rating as an ac fully-coupled DPP. If it is working in the fast switching limit without capacitor charge sharing loss [12], each switch

TABLE I
COMPARISON BETWEEN DIFFERENT DPP TOPOLOGIES AND AN N:1 DAB CONVERTER ($M \geq 1$, $N \geq 2$)

	Topology	Output Resistance	Expected Loss	Scaling Factor
Fully-Coupled DPP	Ac-Coupled	$\frac{8N}{G_{SW}} + \frac{4N}{G_M}$	$M(N-1)\sigma^2(P_{ij}(t)) \times \frac{R_{out}}{V_0^2}$	$\mathcal{S}(MN\sigma^2)$
	Dc-Coupled	$\frac{32N}{G_{SW}} + \frac{16N}{G_M}$		
	SC-based	$\frac{8N}{G_{SW}}$		
Ladder DPP	DAB-cell Buck-Boost-cell	$\frac{32N-32}{G_{SW}} + \frac{16N-16}{G_M}$	$\frac{M(N-1)(N+1)}{6}\sigma^2(P_{ij}(t)) \times \frac{R_{out}}{V_0^2}$	$\mathcal{S}(MN^2\sigma^2)$
N:1 Converter	DAB	$\frac{32}{G_{SW}} + \frac{16}{G_M}$	$\left(MN\sigma^2(P_{ij}(t)) + M^2N^2\mu^2(P_{ij}(t))\right) \times \frac{R_{out}}{V_0^2}$	$\mathcal{S}(M^2N^2\mu^2)$

at the i^{th} port conducts $2\Delta I_i$ for half a switching cycle and the output resistance is $\frac{8N}{G_{SW}}$.

Fig. 8a shows an example of the ladder DPP converter in which each DPP submodule is implemented as a DAB converter. It contains $4N-4$ switches (rated at V_0) and $2N-2$ windings with one effective turn per winding. The output resistance in the ac fully-coupled DPP converter was $\frac{8N}{G_{SW}} + \frac{4N}{G_M}$, but now the currents will be higher. The conduction loss in the i^{th} DPP submodule is

$$\begin{aligned} P_{loss.i} &= (2\Delta I_{i\leftrightarrow i+1})^2 \times \left(\frac{4N-4}{G_{SW}} + \frac{2N-2}{G_M}\right) \times 2 \\ &= \Delta I_{i\leftrightarrow i+1}^2 \cdot R_{out}. \end{aligned} \tag{12}$$

Thus the effective output resistance of each submodule in a ladder DPP with DAB cells is $\frac{32N-32}{G_{SW}} + \frac{16N-16}{G_M}$. For a ladder DPP with buck-boost cells (Fig. 8b), assume that the inductor of each buck-boost cell has the same volt-second-per-turn value as that of each DAB cell in Fig. 8a, and that the inductor current is approximately constant. The effective output resistance of each buck-boost cell is $\frac{32N-32}{G_{SW}} + \frac{16N-16}{G_M}$, the same as that of the DAB cell.

For an N:1 DAB converter, the optimal configuration is to equally allocate semiconductor die area ($G_{SW}V_0^2$) and winding window area (G_M) between the primary side and secondary side. On the primary side, each switch is rated at NV_0 and the effective number of turns is N; on the secondary side, each switch is rated at V_0 and effective number of turns is one. Therefore, the resistances of each switch and winding are $\frac{4N^2}{G_{SW}}$ and $\frac{2N^2}{G_M}$ on the primary side, and $\frac{4}{G_{SW}}$ and $\frac{2}{G_M}$ on the secondary side. Denote the output current as I_{out}. The conduction loss of a DAB converter becomes

$$\begin{aligned} P_{loss} = &\underbrace{\left(\frac{2}{N}I_{out}\right)^2 \times \left(\frac{4N^2}{G_{SW}} + \frac{2N^2}{G_M}\right)}_{primary\ side} \\ &+ \underbrace{(2I_{out})^2 \times \left(\frac{4}{G_{SW}} + \frac{2}{G_M}\right)}_{secondary\ side} = I_{out}^2 \cdot R_{out}. \end{aligned} \tag{13}$$

The effective output resistance of this N:1 DAB converter is $\frac{32}{G_{SW}} + \frac{16}{G_M}$. Table I summarizes the output resistance, expected conduction loss and scaling factors for various DPP topologies as well as for the N:1 DAB converter.

IV. PERFORMANCE LIMITS AND LOSS ANALYSIS

Since only part of the power is processed, a DPP system processes much less power than a conventional N:1 dc-dc converter. A DPP system offers advantages in energy efficiency as N and M scale up, but its advantages in terms of output resistance gradually diminish (as shown in Table I), given a system-level constraint on total device area and magnetic core volume. To evaluate performance limits of DPP topologies, the expected loss of a DPP converter was compared to that of an N:1 DAB at the same total semiconductor die area and core volume (which should reflect converter cost). The normalized loss β ($\beta = \frac{P_{loss,DPP}}{P_{loss,DAB}}$) is used as a performance metric to show the limitations. A lower β indicates lower loss and better performance. The coefficient of variance $C_V = \frac{\sigma(P_{ij}(t))}{\mu(P_{ij}(t))}$ was used to normalize the variance of $P_{ij}(t)$. A Monte Carlo simulation in SPICE was performed to validate the analytical model. Ideal switches and transformers, with series resistors to model $R_{ds(on)}$ and winding resistance, are included. Transformer loss was not included in the analysis of the SC-based DPP topology. Parasitic components and other nonlinear effects are neglected.

In the simulation, the power of each load is set to follow a binary distribution: $P_{ij} = X \cdot P_{work} + (1-X) \cdot P_{idle}$. P_{work} and P_{idle} are the power consumption in the working state and idling state, respectively. Parameter X follows a Bernoulli distribution, $\mathrm{Bernoulli}(p)$, in which p is the probability of being in the working state. Load analysis with other probability distributions, such as $\mathrm{Gaussian}$ or $\mathrm{Poisson}$, leads to similar results. In each case, predefined M, N, and C_V (C_V is in the range of [0,1]) are set, and the simulation is executed 10,000 times to obtain an estimate of average conduction loss of each topology. The simulated β for each DPP topology is obtained through dividing the simulated average loss by the calculated loss in the N:1 DAB converter.

Figs. 9 – 11 illustrate the calculated and simulated β for various DPP topologies as the dimensions of the load array (N and M) and the coefficient of variance of load power (C_V)

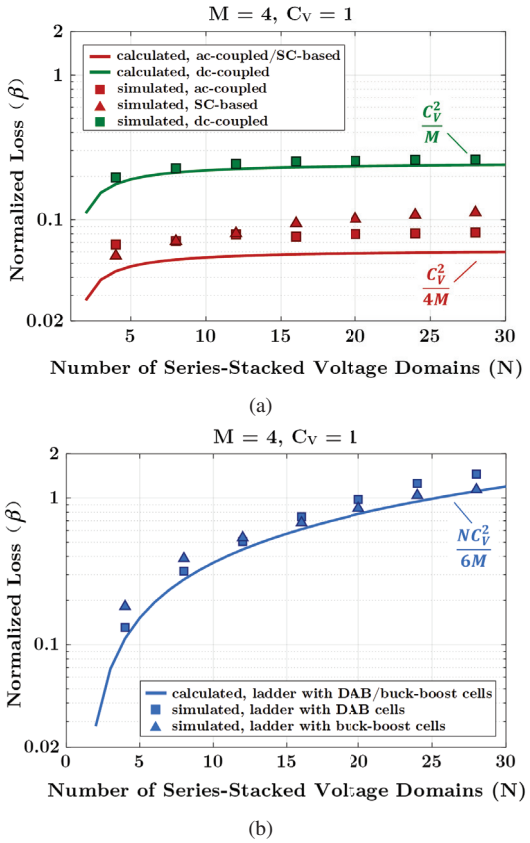

Fig. 9. Calculated and simulated normalized loss β as a function of the number of the series-stacked voltage domains N in: (a) fully-coupled DPP converters; (b) ladder DPP converters.

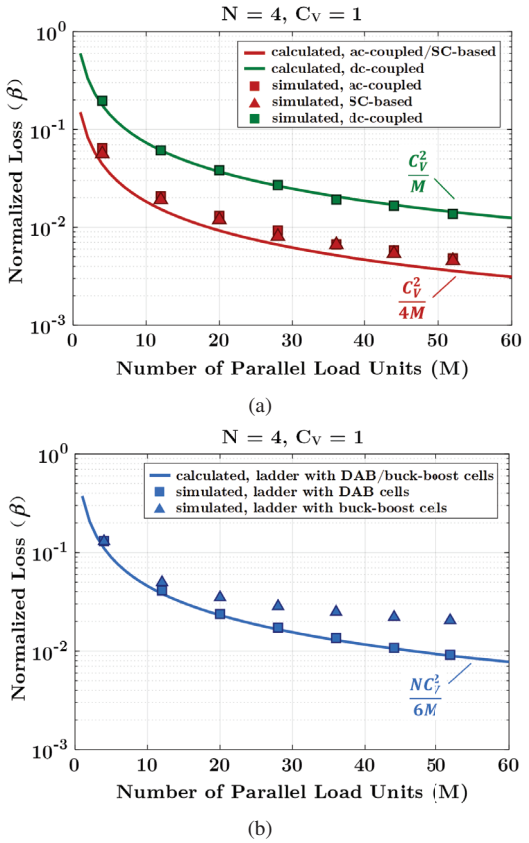

Fig. 10. Calculated and simulated normalized loss β as a function of the number of the parallel loads M in: (a) fully-coupled DPP converters; (b) ladder DPP converters.

scale up. The calculated β matches the simulated results well, supporting the effectiveness of the stochastic model. A small mismatch is caused by the trapezoidal current waveform in the active bridges (Fig. 7a-7b, Fig. 8a), capacitor charge sharing loss in the SC-based DPP (Fig. 7c), and inductor current ripple in the buck-boost cells (Fig. 8b). If M becomes larger or C_V becomes smaller, the average differential power of each buck-boost cell is reduced. In this case, the ripple current of the inductor becomes comparable to the dc average current, and increases the mismatch (Fig. 10b and Fig. 11b).

Figs. 9 and 10 illustrate the scaling of β for various DPP topologies as the load array dimensions (N and M) scale up. Under the fixed constraint of total device area and magnetic core volume, the modeled R_{out} in a DPP topology increases linearly with N, but the modeled R_{out} of an N:1 DAB converter remains unchanged theoretically, as shown in Table I. Considering the scaling of R_{out}, when N increases, the expected loss of fully-coupled DPP topologies increases at the rate of N^2, the same growth rate as that of the N:1 DAB converter, while the expected conduction loss of the ladder DPP topologies grows at the rate of N^3. Therefore, as N scales up, β of the fully-coupled DPP topologies converges to an upper limit, but β of the ladder DPP topologies keeps increasing, as labeled in Fig. 9.

If the number of parallel load units M increases, the expected loss in both fully-coupled DPP and ladder DPP circuits increases at the rate of M, while the expected loss in the DAB grows at the rate of M^2. Thus, β decreases with increasing M for both fully-coupled DPP and ladder DPP circuits, as shown in Fig. 10. This indicates that power variation among different voltage domains reduces if more random loads with the same probability distribution are parallelled in each voltage domain. Figs. 9 and 10 reveal performance limits of these DPP topologies as the DPP system size (N or M) increases. The asymptotic limits are β: $\beta \to \frac{C_V^2}{4M}$ for an ac-coupled or SC-based DPP; $\beta \to \frac{C_V^2}{M}$ for a dc-coupled DPP; and $\beta \to \frac{NC_V^2}{6M}$ for a ladder DPP with DAB or buck-boost cells.

Fig. 11 plots β for various DPP topologies as a function of C_V. When C_V increases, power variation among voltage domains increases, so the DPP converters need to process more differential power. Thus, β increases with C_V for all DPP topologies, but it converges to an upper limit. This is because the conduction loss of an N:1 converter is dominated by the term $MN\sigma^2$ as C_V increases, increasing at the same rate as that of DPP topologies. The asymptotic upper limits of β for ac-coupled or SC-based DPP, dc-coupled DPP, and ladder DPP with DAB or buck-boost cells are $\frac{N-1}{4}$, $N-1$, and $\frac{(N+1)(N-1)^2}{6N}$, respectively.

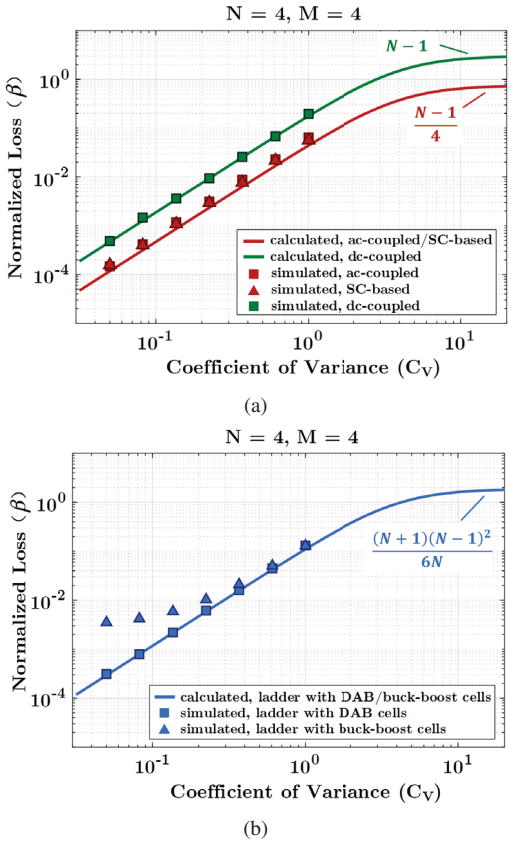

Fig. 11. Calculated and simulated normalized loss β as a function of the coefficient of variance C_V in: (a) fully-coupled DPP converters; (b) ladder DPP converters.

Figs. 9 – 11 and Table I provide quantitative design insights for DPP architectures. For example, the upper asymptotic limit of β in an ac-coupled DPP topology is $\frac{C_V^2}{4M}$ as N increases. Therefore, when $M = 4$, $N \geq 2$, and $C_V = 1$, the normalized loss of an ac-coupled DPP converter is always lower than $1/16$, indicating at least 16x loss reduction compared to an N:1 dc-dc converter. Similarly, a dc-coupled DPP converter can offer at least 4x reduction in loss compared to an N:1 dc-dc converter under the same conditions. If $M > C_V^2$, β of fully-coupled DPP converters will be always less than 1, indicating that a fully-coupled DPP solution is guaranteed to be more efficient than an N:1 dc-dc converter with an arbitrary number of voltage domains. For a ladder DPP converter, β will be larger than 1 if N goes beyond $\frac{6M}{C_V^2}$, indicating that a ladder DPP converter will lose advantages compared to an N:1 dc-dc converter if the number of voltage domains is very large. It should be pointed out, however, that ladder DPP circuits still have high value if load variance is limited. A C_V value of 0.1, for example, still supports a large value of N before β becomes too large. Figs. 9 – 11 and Table I also reveal that ac-coupled DPP stands out from other DPP architectures explored here, although SC-based DPP is equally good if capacitor charge sharing loss is low. The SC-based DPP can be considered as a fully-coupled DPP only if they are operating in fast switching limit (FSL) [12] with very large capacitors.

V. Conclusion

This paper revealed performance limits of differential power processing (DPP) systems. A stochastic loss model was developed to evaluate performance limits of general DPP topologies as dimensions (N, M), average load power (μ), and load power variance (σ) of a modular load array scale up. The performance limits of many DPP topologies were analyzed and compared, providing useful design guidelines for selecting a DPP topology for applications with probabilistic load profiles. The analytical framework was verified by Monte Carlo simulations in SPICE, and the results indicate that the ac-coupled DPP stands out from all other DPP architectures explored in this paper in terms of the lowest average power loss.

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