

A Low-power Reconfigurable Readout Circuit with Large DC Offset Reduction for Neural Signal Recording Applications

Nishat Tasneem and Ifana Mahbub
Department of Electrical Engineering
University of North Texas
Denton, Texas 76207-7102

Email: nishattarannumtasneem@my.unt.edu, ifana.mahbub@unt.edu

Abstract—This paper presents a fully reconfigurable readout circuit including a chopper-stabilized neural amplifier and a successive approximation register (SAR) analog-to-digital converter (ADC) for neural signal recording applications. Since the target neural signals - action potentials (APs) and local field potentials (LFPs) differ in the peak amplitude while occupying different frequency bandwidths, gain, and bandwidth reconfigurability would be advantageous in improving power and noise performance. The readout circuit is designed in 180 nm standard CMOS technology. It achieves the mid-band gain of 50.3 dB in the frequency band of 0.1 Hz - 250 Hz to detect the LFPs, and 63.4 dB in 267 Hz - 20.8 kHz for detecting the APs. The neural amplifier consumes a total power of 1.54 μ W and 1.94 μ W for LFP and AP configurations, respectively. The input-referred noises have been achieved as 0.97 μ V_{rms} (0.1 Hz - 250 Hz), and 0.44 μ V_{rms} (250 Hz - 5 kHz), leading to a noise efficiency factor (NEF) of 1.27 and 1.21, for the two configurations, respectively. It rejects the generated large DC offset up to 40 mV at the electrode-tissue interface, by implementing a DC servo loop (DSL). The offset voltage with the DSL becomes 0.23 mV, which is acceptable for the neural experiments. Enabling the impedance boosting loop, the DC input impedance is found to be within the range of 1.77 - 2.27 G Ω , introducing the reconfigurability in impedance for matching with the electrode impedance. The SAR-ADC having a varying sampling frequency ranging from 10 - 40 ksamples/s demonstrates to digitize the APs and the LFPs with the resolution from 8 - 10 bits. The entire AFE provides good compatibility to record the neural signal while lowering the large DC offset down to 0.23 mV.

I. INTRODUCTION

Remarkable advances in the next-generation portable and implantable medical devices have led to more effective and precise experiments for various neurophysiological activities. Multi-channel neural signal acquisition using invasive penetrating electrodes plays a significant role to perceive the functionalities of the brain [1]. A low-power analog front-end (AFE) featuring small form-factor and low input-referred noise is required to record the targeted neural signals. The AFE also requires the rejection of the large DC offsets due to the differential DC voltage mismatches at the electrode-tissue interface [2]. Typically, the neural signal recording includes the high-precision acquisition of the action potentials (APs) and the local field potentials (LFPs) for numerous neuroscience researches. The targeted neural signals not only have different

amplitudes but also occupy different frequency bands. The APs have the peak amplitude of about 50 - 500 μ V lying within the frequency band of 250 Hz to 5 kHz, whereas that of the LFPs can be up to several mVs lying in the frequency range of 0.1 Hz to 250 Hz [3]. Since the peak amplitude of the APs is less than that of the LFPs in the tenth or higher order of magnitude, the neural amplifier gain is required to be higher for recording the APs. Having the same amount of high gain for both the target signals would result in saturation of the amplifier as well as unnecessary higher power consumption for the LFPs. Additionally, the frequency band of interest for the two signals are different. Thus, the recording AFE should have the reconfigurability in the detection of the APs and the LFPs. Gain and bandwidth reconfigurability would also help to improve the input-referred noise performance in the two different frequency bandwidths.

Several techniques have been implemented to improve the low-frequency/flicker noise ($1/f$) performance in a neural amplifier. The goal is to reduce the noise efficiency factor (NEF), which quantifies the trade-off between the total power dissipation and the input-referred noise in the recording amplifiers [4]. Chopper stabilization technique is utilized in reducing the $1/f$ noise, upconverting the low-frequency neural signal out of the bandwidth, thus eliminating the low-frequency noise component [5]. Since one of the consequences after chopper modulation is the reduction of input impedance, it is required to enhance the impedance at the input of the amplifier [6]. In order to boost the input impedance, a positive impedance-boosting loop is introduced in the amplifier. Another important consideration in designing the chopper-stabilized neural amplifier is to minimize the electrode-DC-offset (EDO) to prevent saturation. Hence, another feedback loop is integrated along with the impedance-boosting loop to attenuate the EDO at the output, called the DC servo loop (DSL) [7]. The readout circuit also includes the SAR-ADC with a reconfigurable resolution of 8 - 10 bits. The sampling rate is also kept as scalable to achieve the reconfigurability in the AP and the LFP bands.

The contributions of the paper are as follows: design of a chopper-stabilized neural signal sensing amplifier eliminating the EDO and enhancing the input impedance performance,

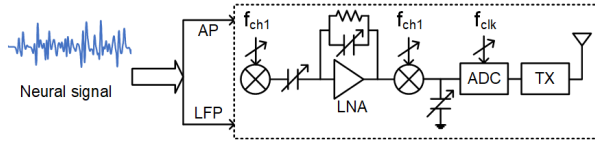


Fig. 1. A reconfigurable neural recording system.

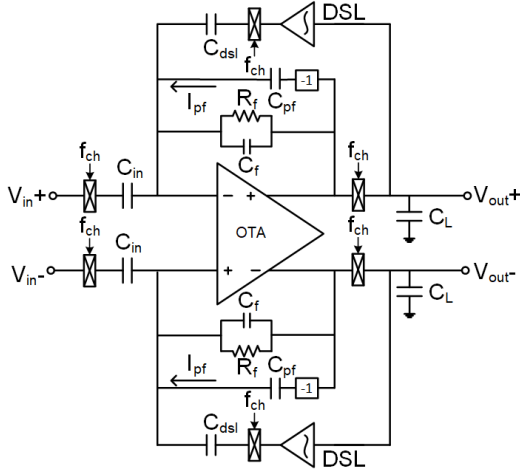


Fig. 2. Schematic of the amplifier with the DSL and IBL.

also achieving a good balance between the noise, power consumption, and linearity. The novelty of the paper includes the fully reconfigurable architecture of the readout circuit, making it possible to acquire the APs and LFPs with low-power and low-noise performance. The paper is organized as follows: section II describes the detailed architecture and design parameters, section III presents the simulation results of the readout circuit for neural signal recording, and a concluding remark is presented in section IV.

II. DESIGN AND ARCHITECTURE

The AFE for neural signal recording applications, mostly being portable and implantable, requires some specifications to ensure several criteria: performance, accuracy, linearity, dynamic range, battery power consumption, and so on. A typical neural signal recording system consists of a low-noise chopper amplifier (LNA) and an ADC followed by a transmitter, as shown in Fig. 1. As most of the neural signal recording system necessitates for multi-channel AFE, the power dissipation for the entire block needs to be minimized, while maintaining the noise floor level in the order of μV . Considering all the requirements, this paper presents a reconfigurable neural amplifier and an SAR-ADC. Fig. 2 presents the schematic of the chopper-stabilized operational transconductance amplifier (OTA) with capacitive-resistive feedback network, impedance-boosting loop (IBL), and the DSL. As the typical frequency bandwidth for the LFPs and APs varies, so does the chopping frequency (f_{ch}) for reducing the input-referred noise. In this work, f_{ch} is chosen to be 1 kHz and 10 kHz for the two target signals, respectively. The descriptions of the reconfigurable feedback loops are described in the sub-sections below.

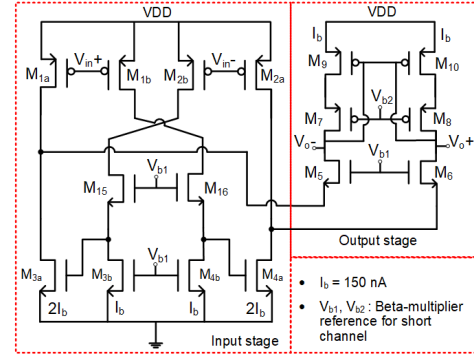


Fig. 3. Schematic of the OTA.

A. OTA

Folded cascode (FC) OTA is a widely used amplifier architecture due to its high gain and wide signal swing characteristics. This paper presents the modified FC by utilizing the current recycling FC (RFC) architecture [8], [9]. The full schematic of the OTA is shown in Fig. 3. It achieves improved performance in terms of gain-bandwidth (GBW) product by utilizing the idle transistors in the conventional FC. Two pairs of PMOS transistors ($M_{1a,b}$ and $M_{2a,b}$) are used as the input pairs in order to reduce the $1/f$ noise components. The input pairs are cross-coupled with the split tail current mirrors - $M_{3a,b}$ and $M_{4a,b}$ with the current ratio of 2 : 1. At the output stage, the source current from M_5 and M_6 are added to the M_{3a} and M_{4a} , respectively. In order to maintain the distribution of current through all the branches equal to I_b , the W/L ratio of M_5 and M_6 are kept to be equal to that of transistors M_{15} and M_{16} . The bias current through each branch is set to be 150 nA, which results in 900 nA as the total current. In order to reduce the $1/f$ noise more, wide-gate input PMOS transistors are used. The W/L ratio of the $M_{1a,b}$ and $M_{2a,b}$ is chosen to be 200/1 $\mu\text{m}/\mu\text{m}$. Beta-multiplier reference circuit for short channel devices are designed to bias the transistors $M_5 - M_6$, $M_{15} - M_{16}$ using V_{b1} voltage, and $M_7 - M_8$ through V_{b2} voltage. The gain of the amplifier, A_v can be calculated by using the following equations:

$$A_v = G_m R_o \quad (1)$$

$$G_m = 3g_{m,1a} \quad (2)$$

where R_o is the equivalent output resistance and G_m is the total transconductance of the amplifier, which is three times that of the input transistor. G_m is enhanced by widening the input pair transistors, thus increasing the gain of the amplifier.

B. Capacitive-resistive Network

The OTA is capacitively-coupled with the input capacitance C_{in} , which blocks all the DC components at the input of the amplifier as shown in Fig. 2. The mid-band gain of the amplifier depends on the ratio of C_{in} to feedback capacitance C_f . It is desirable to set C_{in} to a high value, ensuring a high closed-loop gain performance. As the neural signal's frequency can be as low as in the sub-Hz frequency band, the low-pass

corner of the amplifier requires to reach this band. In order to realize a high feedback resistance value, pseudo-resistor is used as R_f . Two NMOS transistors are diode-connected in series to get the resistor value as high as 100 $G\Omega$ or more. The gain reconfigurability comes from designing the C_{in} and C_f as varactors to vary from 220 pF - 670 pF and 450 fF - 620 fF by applying the control voltage from 0 - 1.8 V. The factor $R_f C_f$ is also used in designing the low-pass corner from around 0.1 Hz - 250 Hz. As the high-pass corner is determined by both the G_m and the load capacitor C_L , a varactor ranging from 1.3 pF - 3.7 pF is implemented as C_L .

C. DC Servo Loop (DSL)

In order to eliminate the effects of saturation due to the large DC offset voltage at the input electrodes, a DC servo loop is implemented. The EDO can be as high as 50 mV, which results in excess DC current, which can damage the tissue. This paper presents a low-bandwidth integrator based DSL to attenuate the EDO. As shown in Fig. 2, the DSL also includes the capacitance C_{dsl} with the integrator to create negative feedback. C_{dsl} is designed to be $C_{in}/50$ to lessen the EDO of up to 40 mV. The unity-gain bandwidth of the DSL integrator is designed in such a way to maintain the high-pass corner as low as 0.1 Hz (applicable to record the LFPs). C_{dsl} is also controlled to demonstrate a varying capacitance of 4.4 pF - 13.4 pF to introduce the reconfigurability in attenuating the EDO.

D. Impedance-boosting Loop (IBL)

The reduction of the DC input impedance due to the chopper stabilization is one of the significant drawbacks in the neural amplifier. The impedance of the electrodes is typically high, so the DC input impedance needs to be matched with that. In order to boost the input impedance, a positive feedback loop is implemented in the amplifier design. The IBL provides the necessary current at the input node by converting the output voltage to current. This current is then being injected back to the generated switched-capacitor resistor, which is supposed to be supplied by the input neural signal from the electrodes. Thus the IBL results in an increase in the input impedance. IBL includes the capacitance C_{pf} , which provides positive feedback current, I_{pf} . C_{pf} is designed in such a way to set I_{pf} equal to the negative feedback current through the $R_f - C_f$ network. Considering an impedance boosting gain of 100, C_{pf} is varied from 2.2 - 6.7 pF in order to set I_{pf} accordingly [6].

E. SAR-ADC

In order to digitize the APs and the LFPs following the amplifier, a successive approximation register analog-to-digital (SAR-ADC) is designed in this paper. Reconfigurability in terms of resolution and sampling frequency is implemented in the design [10], [11]. It consists of the 8 to 10-bit shift register, SAR logic block, DAC (digital-to-analog converter), and one dynamic comparator to introduce the reconfigurability in resolution. One of the most common architectures- charge-scaling DAC consisting of the binary-weighted capacitors is

implemented as the DAC. Since the APs can be as low as few μV , 10-bit ADC can be sufficient to digitize the APs. 8-bit of resolution is enough for the LFPs to faithfully digitize them. Varying sampling frequency from 10 - 40 ksamples/s is also introduced in the ADC design.

III. RESULTS

The proposed neural signal sensing readout circuit is designed in 180 nm standard CMOS technology. The total power consumption from the 1.8 V supply is calculated as 1.94 μW and 1.54 μW for recording the APs and LFPs, respectively.

As discussed in the previous section, C_{in} and C_f are designed to vary the mid-band gain of the amplifier. The gain ranges from 50.3 dB to 63.4 dB while setting up the parameters as: $C_{in} = 670$ pF, $C_f = 450$ fF and $C_{in} = 220$ pF, $C_f = 620$ fF, respectively. The target neural signals can be detected within two different bandwidths: 50.3 dB in 0.1 - 250 Hz for LFPs and 63.4 dB in 267 Hz - 20 kHz for APs. Fig. 4 shows the mid-band gain with the $R_f - C_f$ network for two different bandwidths (Fig. 4(a) for LFPs and Fig. 4(b) for APs). Chopper modulation technique is implemented to the amplifier to attenuate the $1/f$ noise components by up-converting the neural signal to a higher frequency. The input-referred noise is simulated over the AP and the LFP bands to see the effects of chopper stabilizing on the noise performance. Integrated within the 250 Hz - 5 kHz (AP band), the input-referred noise is simulated as 0.44 μV_{rms} , while that within the LFP band (0.1 Hz - 250 Hz) is found as 0.97 μV_{rms} , resulting in the NEF of 1.21 and 1.27, quantifying the balance between noise-power performance. Fig. 5(a) presents the input-referred noise of the chopper amplifier. One of the consequences of chopping is that the chopper stabilization significantly reduced the DC input impedance of the amplifier to 27.8 $M\Omega$. Introducing the positive feedback loop boosts the DC impedance to 1.77 $G\Omega$ and 2.27 $G\Omega$ for the two signals. As enabling the IBL results in increasing the chip area, the varying MIM capacitors are optimized to get a boosting factor of 63 and 81. With the low-bandwidth integrator, the DSL decreases the generated EDO at the electrode interface. Simulation results show that the proposed neural amplifier enabling the DSL can suppress as high as ~ 40 mV EDO. Implementation of DSL results in 0.23 mV DC, which could be considered as negligible for AP and LFP recording applications.

The reconfigurable SAR-ADC is also simulated along with the neural amplifier. A varying resolution of 8 - 10 bits is achieved to record the APs and LFPs. Since the peak amplitude of LFPs can reach up to few mVs, an ADC with a resolution of 8-bit would be sufficient enough to digitize them. APs need higher resolution with a higher sampling frequency. The sampling frequency is also varied within the range of 10 - 40 ksamples/s. The ADC with a total power consumption of 134 μW achieves the effective number of bits (ENOB) as 6.9 - 8.8. The noise density of the ADC is simulated and presented in Fig. 5(b). The low-power neural amplifier integrated with the ADC demonstrates the reconfigurability features to record the APs and LFPs separately with a large DC offset reduction.

TABLE I
COMPARISON AMONG OTHER WORKS

Specifications	[12]	[1]	[6]	[13]	[14]	This work*
Technology (nm)	65	40	65	65	180	180
Supply voltage (V)	0.8	1.2	1	1	2.7 - 3.6	1.8
Gain (dB)		AP : 69, LFP : 78	100	60.2, 70.4, 80.8	128	50.3 - 63.4
Power consumption (μ W)	0.8	2	1.8	1.86	0.108 - 0.144	1.54 - 1.94
NEF	1.81	AP : 4.9, LFP : 7	3.3	1.99	-	1.21, 1.27
Input-referred noise	44	AP : $7 \mu V_{rms}$ LFP : $2 \mu V_{rms}$	60	0.7	19	AP : $0.44 \mu V_{rms}$ LFP : $0.97 \mu V_{rms}$
	nV/ $\sqrt{Hz}$		nV/ $\sqrt{Hz}$	μV_{rms}	nV/ $\sqrt{Hz}$	

*Simulation results

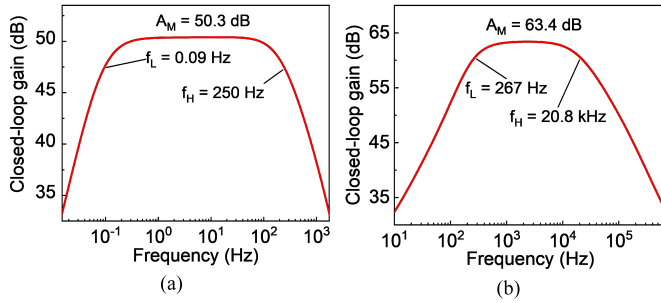


Fig. 4. Closed-loop gain of the neural amplifier in two different bandwidths.

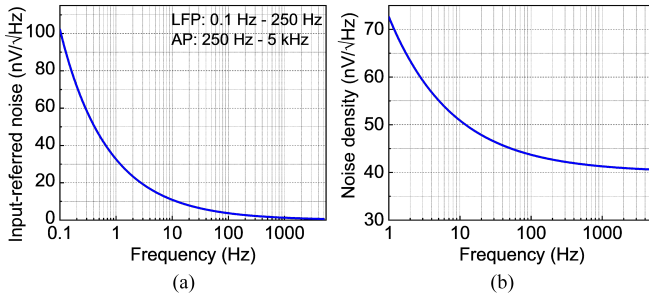


Fig. 5. (a) Input-referred noise of the amplifier, (b) noise density of the ADC.

Table I presents the comparison among other state-of-the-art neural amplifier performances, which clearly shows the improved performance of the proposed work, featuring a wide range of reconfigurability within power, noise, and gain for recording the neural signals. The trade-off between power and noise is also maintained better than other works, which is represented by the NEF. The amplifier also achieves a wide range of mid-band gain for APs and LFPs, which helps to optimize the amplifier saturation and power consumption.

IV. CONCLUSION

In this paper, the neural chopper amplifier along with an SAR-ADC demonstrates the reconfigurability to record the APs and the LFPs separately, with the goal of attenuating the large DC offset at the electrode and boosting the input impedance. A low-bandwidth DC servo feedback loop is implemented in order to eliminate the EDO. An impedance boosting positive feedback loop is employed to enhance the input impedance.

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