20MHz, Two Phase Negative Coupled Inductor Design for Integrated Voltage Regulator in Smartphone Applications

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***Abstract*—In order to provide a compact and efficient power solution for high-performance processors in smartphone application, three-dimensional integrated voltage regulator operating at ultra-high frequency(beyond 10MHz) becomes a promising solution. One of the most challenging parts is ultra-low profile magnetic design with small footprint, loss and large current handling capability. In this paper, a novel, two phase negative coupled inductor structure with TKOIN metal-flake composite magnetic material is proposed. The structure exploration and design process are illustrated with the help of finite element tool. The new inductor structure features very small inductor loss(<0.15W per phase) and footprint(<4mm^2 per phase), large inductance density and current handling ability(3A dc current per phase) operating at 20MHz switching frequency. Three different inductor samples are fabricated and experimentally tested to verify the design and evaluate thermal performance of inductors.**

Keywords – Ultra-high frequency, Low profile, Coupled inductor, Smartphone

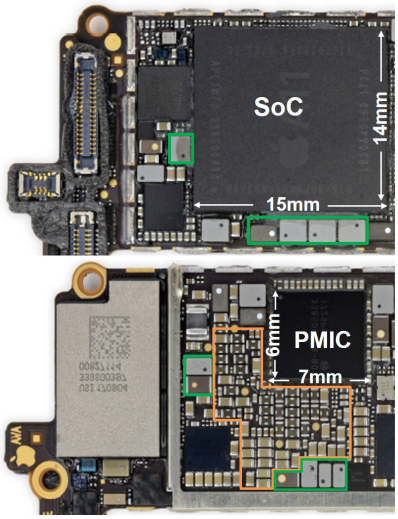

Fig. 1: Power Management Design in iPhone 8 Motherboard

I. Introduction

As the number of cores in System-on-chip (SoC) and power demand increase in mobile applications, power management is crucial to the whole system. Fig 1 shows the power management design of SoC in iPhone 8 motherboard. The processor is on the front side of motherboard and power management integrated circuit (PMIC) is on the back side of motherboard. The green box and orange box indicate output inductors and capacitors used in multiphase buck converters, where passive components occupy lots of spaces. On the other hand, dynamic voltage and frequency scaling (DVFS) can help reduce power consumption of processor dramatically [1]–[3]. However, traditional voltage regulators cannot support this function due to low frequency operation and long power delivery path. In order to reduce the size of passive components and fully utilize DVFS, integrated voltage regulator (IVR) becomes more and more popular by pushing frequency to tens of MHz [4]–[17]. One of the main challenges for IVR is very high frequency magnetic design and integration with small volume and loss. For the magnetic integration in IVR, the on-chip inductor based on wafer level integration and package-embedded magnetic integration are two mainstreams. The on-chip inductor achieves ultra-high inductance density and small inductor size with a multi-turn structure [4]–[10]. However, large DC resistance (DCR) limits its current handling ability to <1A load current per phase generally. In smartphone applications, the peak current demand for CPUs could be tens of ampere. Increasing the phase number to supply sufficient power increases cost and control complexity. On the other hand, package-embedded inductor with a larger current handling ability is more suitable for high output current applications [11]–[17]. Among them, a single-via 5 phase integrated inductor with lateral flux pattern for a three-dimensional (3D) IVR structure was proposed by Hou as shown in Fig 1 [17]. The inductor and PMIC are right beneath the processor, which can provide a very short power delivery path and save the space occupied by inductors. To achieve this, a 5-phase integrated inductor structure was proposed, where each via serves as winding for one phase inductor. This structure has very small DCR, footprint with ultra-low profile and can support total 15A load current. However, the unbalanced design between core loss and winding loss results in high core loss, which lowers the whole system efficiency. At the same time, the low inductance value of each phase causes huge current ripple. In order to reduce core loss and boost the inductance, a novel, 2 phase negative coupled inductor structure is proposed in this paper. The structure derivation process is illustrated in section

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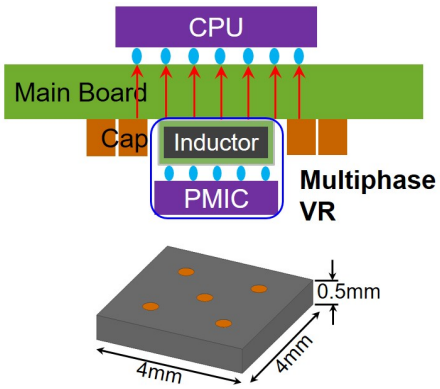

Fig. 2: three-dimensional IVR structure with single-via 5 phase integrated inductor

II. The design process of the new structure is presented in section III. The fabricated inductor prototypes and experimental results are provided in section IV. Finally, conclusion and future work are presented in section V.

II. Proposed Three-via Two Phase Negative Coupled Inductor Structure

As mentioned before, the large core loss of each phase results in high inductor loss in single-via 5 phase inductor. First, new single phase inductor structures are explored in this section to improve inductor performance by reducing core loss. Then two phase negative coupled inductor structure is proposed based on single phase inductor structure. To make a fair comparison between different inductor structures, the operating condition are kept the same below. Input voltage Vin=3.8V and output voltage Vo=1V is chosen as nominal design point in this paper. The switching frequency is set to be 20MHz and load current for each phase is 3.75A. Metal flake composite from TOKIN is chosen as magnetic material due to compatible for pcb integration, lower loss at larger flux density excitation and larger permeability with dc bias field compared with LTCC material [18]. Due to non-uniform flux distribution of this lateral flux structure, the Finite Element Analysis (FEA) tool is used to evaluate the inductance and core loss of different inductor structures [19], [20].

A. Single Phase Inductor Structure Exploration

For single phase inductor, Fig 3 shows the single-via inductor structure and its flux density distribution plot with 2x2mm footprint, 0.5mm thickness and 0.15mm radius for the via. It can be seen high ac flux density in the core causes large core loss for this structure. To reduce ac flux density in the core, several new structures are proposed as shown in Fig 4. To make a fair comparison, the footprint and thickness are kept the same for new structures. Fig.4(a) shows the new structure#1 with 3 vias in the core. The scale for ac flux distribution plot is the same as that in Fig 3. Black cross and dot represent current direction flowing into and out of the paper respectively. Solid line in ac flux distribution plot shows its ac flux flow direction.

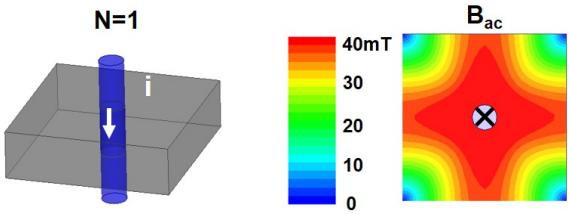

Fig. 3: Single via structure and ac flux distribution

With given voltage second, each via only withstand one third of total flux in structure #1. As a result, ac flux density in the core is reduced. Table I shows the loss and inductance comparison between single-via structure and new structure #1. Although winding loss increases due to more vias and surface winding, core loss of structure #1 reduces more resulting in smaller inductor loss compared to single-via inductor. The inductance of structure #1 is also boosted by 2 times. The

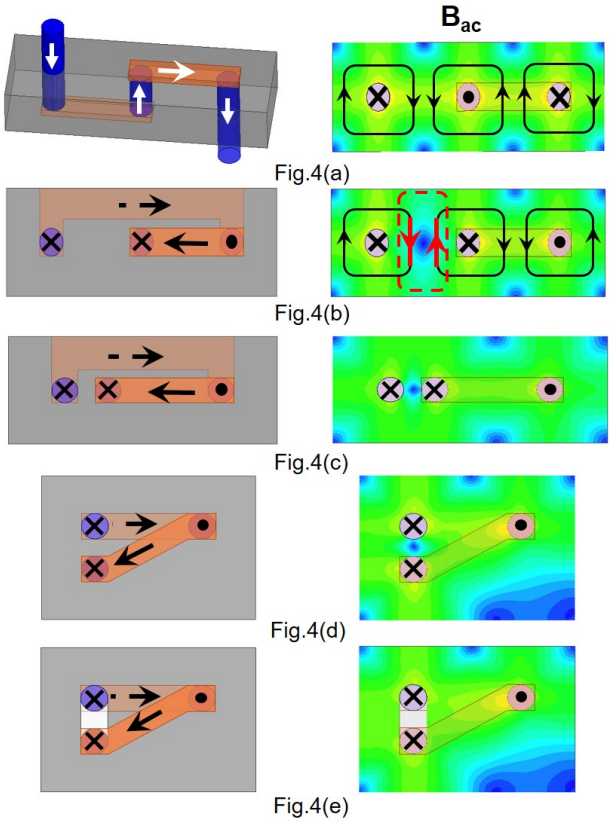

Fig. 4: Different single phase 3-via structures and their ac flux distribution

core loss of structure #1 can be further reduced by utilizing flux cancellation. Fig.4(b) shows structure #2 by exchanging the position of second via and third via in structure #1. In the region highlighted by red dashed line, the flux generated by the first and second via are cancelled with each other due to opposite direction, leading to small ac flux density in this

TABLE I: Loss Comparison Between Different single phase Inductor Structures

	Core loss(mW)	Winding loss(mW)	Total loss(mW)	L(nH)
single-via	280	1	281	13
#1	92	34	126	24
#2	78	52	130	26
#3	67	45	112	29
#4	67	37	104	26
#4 w slot	67	37	104	26

area. Then the core loss of structure #2 is even smaller as shown in Table 1. However, the inductor loss is larger than that of structure #1 because of larger winding loss with longer bottom surface winding. Then structure #3 is proposed by moving first and second via close to each other as shown in Fig. 4(c), where the distance between these two vias is 0.2mm considering manufacture capability. On the one hand, the area with small ac flux density in structure #2 is reduced in this way. The saved core area is utilized to increase the distance from via to the edge of the core, which equivalently increases the cross-section area, leading to smaller core loss in structure #3. On the other hand, the length of bottom surface winding is also reduced. As a result, structure #3 has smaller inductor loss compared with that of structure #4. To further reduce bottom surface winding length, the second via position is rotated in structure #4 as shown in Fig.4(d). The winding loss is further reduced with on sacrifice on core loss. However, the very small distance between two vias makes it difficult to drill holes in the magnetic core. To reduce manufacture burden, air slot is used rather than holes as shown in Fig.4(e). It can be seen air slot has no impact on inductor performance. Therefore, structure #4 with air slot is chosen for is chosen for coupled inductor design for the next step.

B. Proposed Two Phase Negative Coupled Inductor Structure

From Fig.4(e), it can be seen there is unutilized core area in the right corner of the core with very small ac flux density for single phase inductor. This area actually can be utilized by another phase as shown in Fig 5, where two phase inductors are integrated in one magnetic core. The opposite flux direction generated by two phases makes it a negative coupled inductor structure naturally. Due to flux cancellation, the dc flux in this structure is smaller than that of single phase inductor. Another benefit of this structure is non-linear inductance of negative coupled inductor. There are two inductances for coupled inductor, steady state inductance L_{ss} and transient inductance L_{tr}. The expressions of L_{ss} and L_{tr} are shown below:

$$L_{ss} = L_{self}\frac{(1-\alpha^2)}{(1+\frac{D}{1-D})\alpha} \quad (1)$$

$$L_{tr} = L_{self}(1+\alpha) \quad (2)$$

Where L_{self} is self inductance and α is coupling coefficient. Small steady state current ripple and fast transient response are achieved with large L_{ss} and small L_{tr}. For non-coupled inductor, the steady state inductance and transient inductance are the same as self inductance. Therefore, small current ripple at steady state and fast transient speed cannot be achieved at the same time. However, for negative coupled inductor, α is a negative value and larger α gives larger ratio between L_{ss} and L_{tr} [21], which is preferred from circuit operation point of view. To fully explore the performance of this novel negative coupled inductor structure, a detailed design process is discussed in section III.

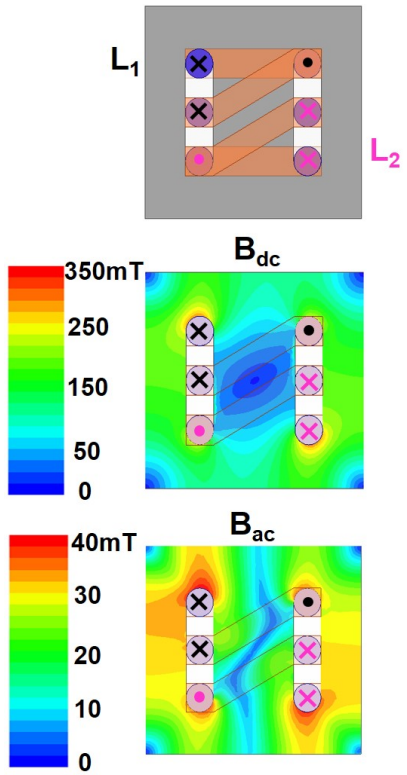

Fig. 5: Proposed 2 phase negative coupled inductor and its flux distribution

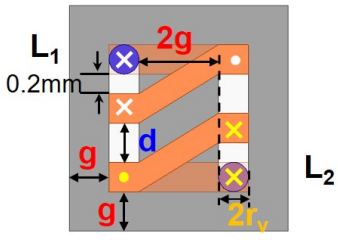

Fig. 6: Design parameters of proposed negative coupled inductor

III. Design Process of 2 Phase Negative Coupled Inductor

The design parameters of this 2 phase negative coupled inductor is shown in Fig 6, where r_v is via radius, d is the distance between two inductors controlling the coupling between two phases, h is core thickness and g value determines

the total footprint. Based on manufacture capability and current handling capability, r_v is set to be 0.15mm. Core thickness is set to be 0.5mm to achieve low profile target. The values of d and g are swept to evaluate their impact on inductance, footprint and loss. First, the impact of d value on coupling coefficient, inductance and loss per phase are analyzed as shown in Fig 7 and Fig 8. The d value is swept from 0.2mm to 0.6mm. The g value and thickness of the core are fixed as 0.4mm and 0.5mm for all cases. Larger d value results in smaller coefficient, L_{ss} and larger L_{tr}. From flux density distribution plot, it can be seen ac flux density crowding is more severe in the core with larger d value, leading to larger core loss. Therefore, smaller d value is preferred and chosen as 0.2mm considering manufacture capability of embedding magnetic core into PCB in the future.

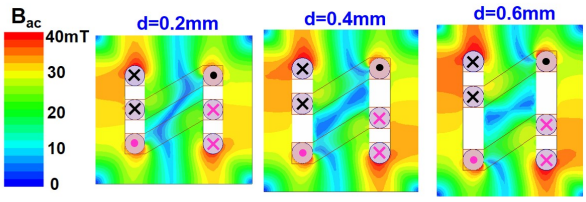

Fig. 7: The impact of d value on flux distribution

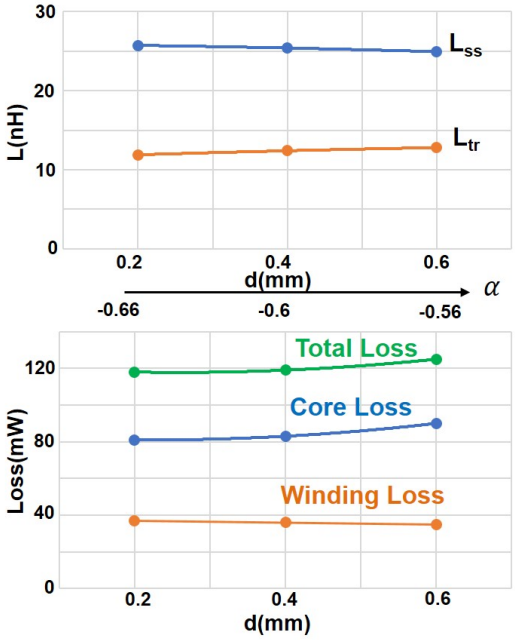

Fig. 8: The impact of d value on inductor performance

Then the impact of g value on inductance, loss and footprint for each phase is analyzed as shown in Fig 9. The d value is fixed as 0.2mm and g is swept from 0.3mm to 0.6mm corresponding to footprint from 1.7mm^2 per phase to 3.8mm^2 per phase. It can be seen larger inductance is achieved with larger g value. For the loss part, larger g value results in smaller core loss due to reduced flux density with increased cross section area. The winding loss increases with larger g value because of longer surface winding. Since core loss is the dominant part of inductor loss, increasing g value will reduce total loss of the inductor. Therefore, there is a trade-off between inductor loss and footprint. Three different inductor samples with different footprint named as sample A, sample B and sample C are fabricated by TOKIN as shown in Fig 10 from left to the right. The footprint for each phase of sample A, B and C are 1.7mm^2, 2.6mm^2 and 3.8mm^2 respectively. The core thickness, h=0.5mm are kept the same for all three samples. In section III, the inductance of these samples are measured first to verify the accuracy of inductor model. Then their thermal performance are tested. Finally, the performance of 2 phase coupled inductor are compared with that of single-via 5 phase inductor to demonstrate the improvement by using new inductor structures.

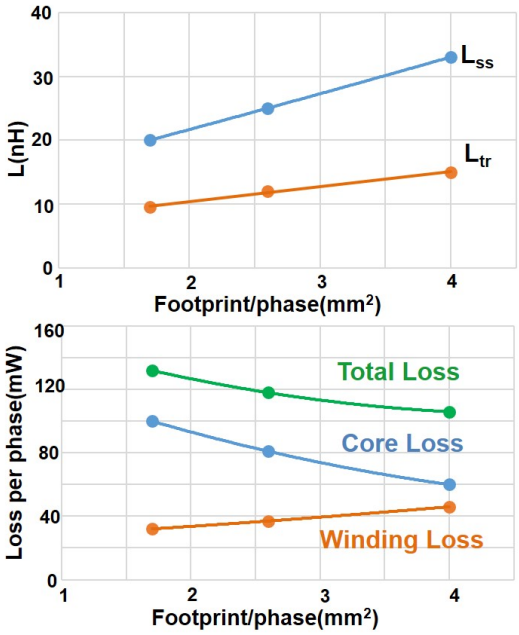

Fig. 9: The impact of g value on inductor performance

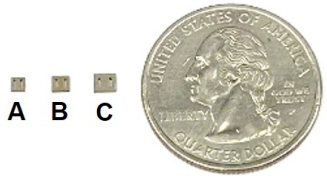

Fig. 10: Fabricated inductor samples

IV. Experiments and Comparison

Due to very short winding length and ultra-high frequency of inductor current ripple, the method proposed in [22] by using a rogowski coil to measure inductor current cannot be applied in this case. This paper proposes another method to measure the inductance under high frequency as shown in Fig 11. The ac

excitation of a 20MHz, sinusoidal waveform is provided by a function generator(Tektronix AFG31020) and power amplifier (150A100C from Amplifier Research) and connected on the pcb board by flowing through an isolation transformer. Two dc current sources(TDK Lambda UP60-14) are used to provide dc load current for two inductors, L_1 and L_2. The voltage v_1 of inductor L_1, voltage v_2 of inductor L_2, and ac current of inductor L_1, i are measured by using differential voltage probe(TDP1000) and current probe(TCP0030A). A large choke inductor is added in the dc current loop of L_2 to reduce its impact on v_2 measurement. Then self inductance L_{self} and mutual inductance M under dc load current can be calculated as below based on measured voltage and current

$$L_{self} = \frac{1}{2\pi f_s}\frac{V_1}{I} \tag{3}$$

$$M = -\frac{1}{2\pi f_s}\frac{V_2}{I} \tag{4}$$

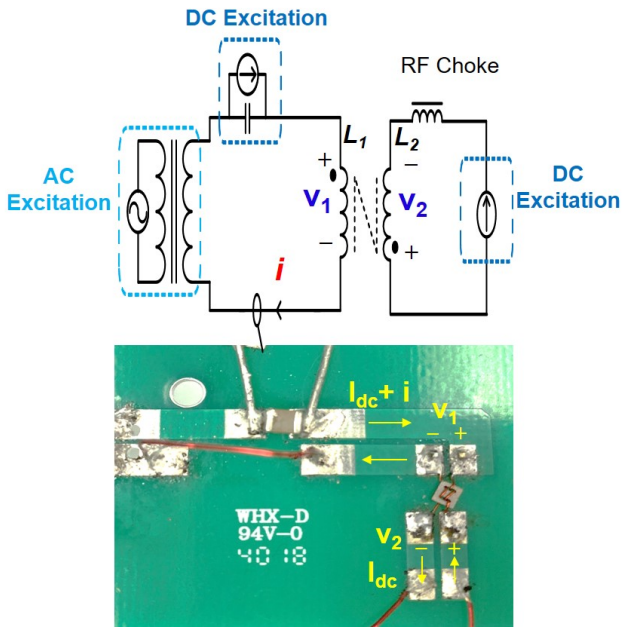

Fig. 11: Inductance measurement principle and circuit board

Where V_1, V_2 and I are the amplitudes of v_1, v_2 and i, f_s is testing frequency. Then L_{ss} and L_{tr} can be calculated based on equation (1) and (2). Fig 12 shows the comparison between measurement results represented by points and simulation results represented by solid lines at 20MHz. It can be seen the measurement results can match very well with simulation results for all three inductor samples.Then the thermal performance of these samples are evaluated. A two phase buck converter is built as shown in Fig 13. Low voltage GaN device, EPC2040 from EPC is used as switches to operate at 20MHz with gate driver PE29102 from pSemi. The thermal images of 3 different samples are shown in Fig 14 with 3.8V input voltage, 1V output voltage and 3A load current. The temperature rise of sample A, B and C at natural convection are 50 °C, 43 °C and 27 °C respectively. It can be seen that although these inductors operates at ultra-high switching frequency, it is still thermal manageable. It can be ascribed to the fact of: 1)large surface-area-to-volume ratio of this ultra-low profile inductor structure;2) very small inductor loss design. Among all three samples, sample A has highest temperature rise due to largest core loss and smallest footprint.

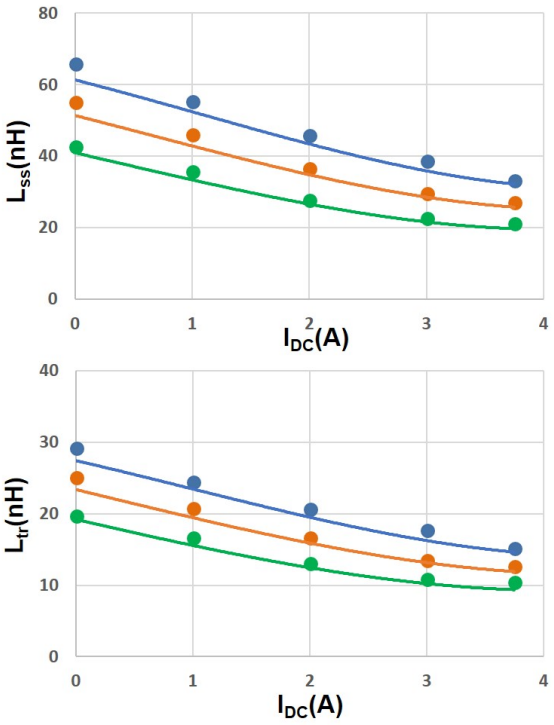

Fig. 12: Comparison between measurement and simulation result of inductance. The green, orange and blue color represent results of sample A, B and C respectively.

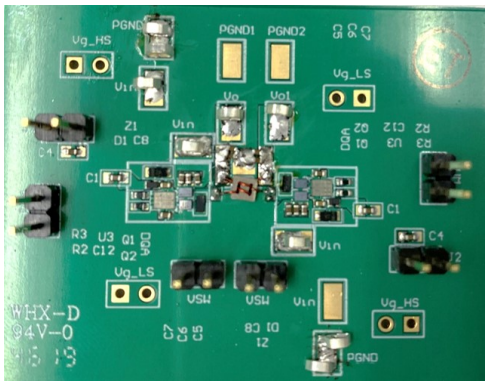

Fig. 13: 2 phase buck converter board with testing inductor samples

Therefore, thermal performance needs to be considered as an important aspect besides inductance, inductor loss and size.

Finally, the inductor performance comparison between these three new inductor designs(sample A, B and C) with single via 5 phase inductor in [17] is shown in table II. All values in table II are per phase values. The units for loss, footprint and inductance are mW, mm^2 and nH. It can be seen the new structure has more than 50% loss and footprint reduction. With similar footprint, the steady-state inductance of sample C is almost boosted by 3 times compared with the inductor structure in [17].

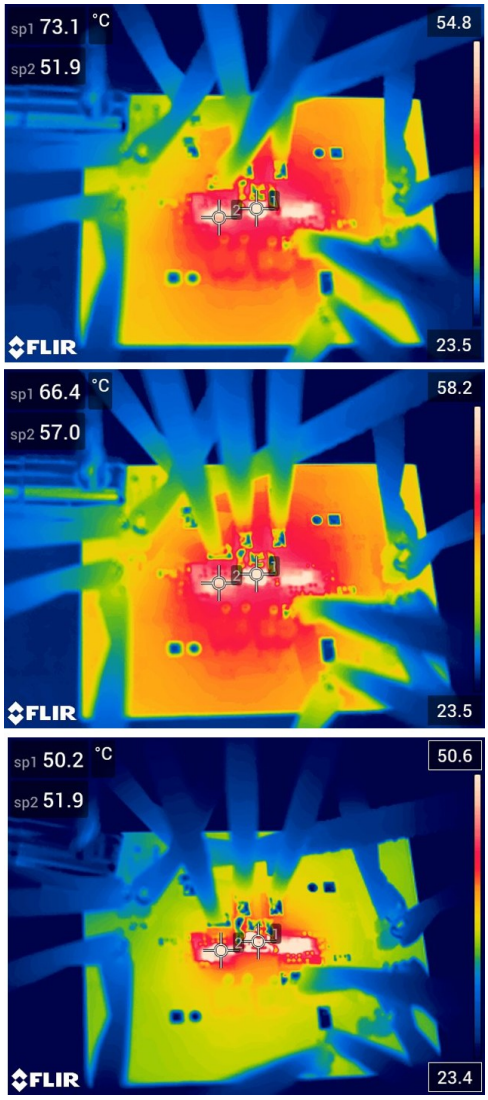

Fig. 14: Thermal images of inductor samples A,B and C with natural convection from top to the bottom. Spot 1 indicates inductors under test ; spot 2 indicates GaN device EPC2040.

V. Conclusions

In this paper, a novel, two phase negative coupled inductor structure is proposed for integrated voltage regulator in smartphone applications. In this paper, a novel, two phase negative coupled inductor structure with TKOIN metal-flake composite magnetic material is proposed. The structure exploration and design process are carefully analyzed with the help of finite element tool. The new inductor structure has a significant loss and footprint reduction compared to the work in literature. Three different inductor samples are fabricated and experimentally tested at 20MHz with a two phase buck converter built with GaN devices. The measurement result verify the design and thermal test shows that new inductor structure is thermal manageable. The future work will be multi-phase(more than 2 phase) inductor design and PCB integration.

TABLE II: Inductor performance comparison

	Core loss	Winding loss	Total loss	footprint	L_{ss}	L_{tr}
[17]	280	1	281	3.2	13	13
A	100	32	132	1.7	20	9.5
B	81	37	118	2.6	25	12
C	60	46	106	3.8	33	15

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Disclaimer

Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the National Science Foundation.

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