# Dual-Loop Frequency Synchronization and Load Regulation using a Discrete Time Model for a 7-Level Switched Capacitor WPT Rectifier

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Abstract—In wireless power transfer (WPT) applications, the multi-level switched capacitor topology achieves significant advantages in terms of efficiency, system loading, THD, and output regulation. The topology requires dual-loop control in order to harness these benefits. First, a small signal discrete time model for the 7-level rectifier WPT system is developed. Then, a control loop is designed that enables the rectifier to regulate DC load voltage by varying its modulation scheme. Next, the WPT carrier frequency is sensed and a phase-locked loop is used in combination with the small signal power stage model to design a closed-loop controller that synchronizes frequency and regulates control phase through adjustments of the switching period. Finally, cross-coupling interactions between the two control loops are modeled, and stable dual-loop operation is shown.

## I. INTRODUCTION

Active rectifiers in wireless power transfer (WPT) systems are capable of increasing rectifier efficiency, reducing coil harmonic content, regulating load voltage, and providing real-time system tuning [1–4]. However, any receiver-side WPT active rectifier requires some form of sensing and regulation in order to isolate and match the carrier frequency. Any error between transmitter and rectifier switching frequency will cause phase drift, causing beat frequency oscillations and negatively impacting the WPT system [4, 5]. Synchronous rectifiers are also often controlled to regulate the output via closed-loop output voltage sensing [4, 6, 7]. Realizing both output regulation and frequency synchronization from a single power stage requires stable dual-loop control design.

One synchronization approach is to sense the voltage across the switching devices. With the assumption that the active rectifier will always switch at zero input phase, the devices are actuated with a change in voltage polarity [8,9]. This technique relies on fast sensing to reduce conduction loss by forcing the switches to act as near-ideal diodes, limiting reverse current from commutation delays [8,9]. This diode emulation technique fails to leverage the switching rectifier's ability to control phase, a capability that could be used to actively respond to load or tuning changes.

Some techniques sense other circuit parameters like secondary current [10, 11] or secondary capacitor voltage [12]. A lower power implementation for smart watch applications

actually senses the WPT magnetic field and uses it to generate a clock. This clock serves as a reference for synchronously switching the secondary side [13]. Again, control freedom is sacrificed for each approach that emulates ideal diode switching [10–13].

Another strategy is to simplify or disregard the plant model [14,15]. If the power stage model is disregarded, a low bandwidth phase-lock loop (PLL) can be used to control the switching frequency [14]. This technique assumes that the relevant dynamics of the power stage are attenuated by the lower bandwidth control loop and will not significantly influence the synchronization. Here, two trade-offs arise: the designed control bandwidths must be forced low, and the final loop dynamics are not predicted due to the absence of a precise plant model. Experimental settling times from 110 ms to 140 ms are demonstrated for a system using a digital PLL to synchronize frequency, but no model comparison is provided for these results [15].

Active rectifiers are also capable of regulating the output load by varying their switching times [3, 6, 7, 16]. The phase [3] or duty cycle [6, 7] of the rectifier are used to regulate the output through variations in the loading impedance seen by the inverter.

It is possible to combine frequency synchronization and output regulation without communication between the primary and secondary sides [13, 17]. In [17], three signals are sensed: input voltage, input current, and output voltage. Because all control parameters are interdependent, frequency synchronization is verified when the output voltage error term goes to zero [17]. These works again lack discussion of synchronization transient times and small-signal predictions of loop-stability [17].

Previous work characterizes the 7-level switched capacitor topology as a good candidate for wireless power [2] and investigates secondary-side sensing and discrete time plant modeling, both of which serve to accomplish frequency synchronization [4,5]. This paper combines the bodies of work. The state space model of the 7-level rectifier, in Section II, is used to develop discrete time small signal models of the system in Section III. Closed-loop controllers for both loops

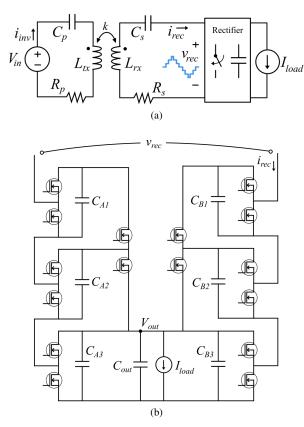


Fig. 1. (a) Wireless power circuit and (b) 7-level rectifier topology.

are analyzed in Section IV. The analysis is verified on a prototype 20 W, 150 kHz system in Section V. Simultaneous, dual-loop operation is demonstrated in Section VI. Section VII concludes the work.

## II. STEADY-STATE STATE SPACE MODEL

The wireless power transfer system in this work is comprised of an inverter, tuned tank, and a 7-level switched capacitor rectifier. Fig. 1a shows an overview of the WPT network. The inverter stage is modeled as a voltage source,  $V_{in}$ , that flips polarity according to the inverter switching actions. Components  $R_p$ ,  $C_p$ , and  $L_{tx}$  makeup the transmitterside of the WPT tank, while  $R_s$ ,  $C_s$ ,  $L_{rx}$  comprise the receiver-side portion of the tank.

The 7-level switched capacitor rectifier [18] is shown in Fig. 1b. Each of the flying capacitors  $(C_{A1}...\ C_{B3})$  and the output capacitance  $(C_{out})$  have small ripple around a DC value equal to the output voltage, 5 V in this work. The circuit operates by periodically switching the flying capacitors in parallel with  $C_{out}$  orin series in the path of  $i_{rec}$ , generating a 7-level staircase waveform,  $v_{rec}(t)$ .

Within any switching interval, the circuit is modeled by state space equations of the form

$$\dot{x}(t) = Ax(t) + Bu(t)$$
. [19]

The state vector x(t) is made up of the inductor currents and capacitor voltages in Fig. 1.

$$\begin{aligned} x(t) = & [v_{CA1} \ v_{CA2} \ v_{CA3} \ v_{CB1} \ v_{CB2} \dots \\ & v_{CB3} \ v_{Cout} \ v_{Cp} \ v_{Cs} \ i_{Ltx} \ i_{Lrx}]^T. \end{aligned}$$

where each state variable's time dependency '(t)' is dropped for conciseness. The input vector contains the DC source voltage  $V_{in}$  and DC load current  $I_{load}$ . Because the input vector consists of only ideal DC sources, it is not time varying,  $u(t) = U = [V_{in} \ I_{load}]^T$ .

Matrices  $A_i$  and  $B_i$  model the circuit during the  $i^{th}$  switching interval. For the 7-level switched capacitor rectifier, as modulated in this work, there are 16 switching intervals per period,  $i \in \{1, 2, 3...16\}$ . Because the model contains 11 states and 2 inputs,  $A_i \in \mathbb{R}^{11 \times 11}$ ,  $B_i \in \mathbb{R}^{11 \times 2}$ . PLECS [20,21] is used in conjunction with MATLAB to produce each of the state space matrices  $A_i$  and  $B_i$ , numerically.

When A is invertible, the state space description in (1) has the closed-form solution

$$x(t) = e^{A_i t} x_0 + A^{-1} (e^{A_i t} - I) B_i U$$
 (2)

where t is any time within interval i and  $x_0$  is the state vector at the beginning of the interval. Let  $t_i$  be the duration of interval i. This means that  $x(t_i)$  is the state vector at both the end of interval i and the beginning of interval i+1. The model propagates through the full period by initializing the state vector of each interval with the final state vector values from the previous interval.

Steady state occurs when the state vector begins and ends at the same values after one period. A closed form expression for the steady state value of x(t) is given by

$$X_{ss} = X_{ss1} = \left(I - \prod_{i=1}^{16} e^{A_i t_i}\right)^{-1}$$

$$\sum_{i=1}^{16} \left(\prod_{k=i+1}^{16} e^{A_k t_k}\right) A_i^{-1} \left(e^{A_i t_i} - I\right) B_i U, \quad [20]$$

where  $X_{ss}$  is the beginning of the period, and  $X_{ss1}$  is the beginning of interval 1. More generally,  $X_{ssi}$  represents the steady state values of x(t) at the beginning of interval i.

The state space model of the 7-level switched capacitor rectifier WPT circuit is verified in Fig. 2, where the experimental waveforms are shown in good agreement with the predicted waveforms. This steady-state model is the foundation of the small signal modeling in the remainder of this work.

## III. DISCRETE TIME SMALL-SIGNAL MODEL

## A. Output Transfer Functions

The state space model of the rectifier in Fig. 1 is employed to develop small-signal models of transient dynamics and design feedback control. Using discrete time modeling, the small signal dynamics of the converter, sampled synchronously with the switching period, are given by [19]

$$\hat{x}[n+1] = N\hat{x}[n] + F_q \hat{t}_q[n].$$
 (4)

The natural response of the system, N, is

$$N = \prod_{i=16}^{1} e^{A_i t_i},\tag{5}$$

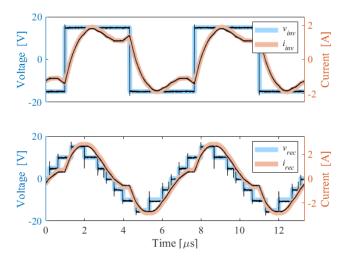


Fig. 2. Verification of state space modeled waveforms (color) with experimental overlaid in black.

where the total change in states over one full period is the cumulative result of all 16 intervals through which the states must propagate.

The forced response matrix,  $F_q$ , models the system response to perturbations in the modulation pattern. For a perturbation to any individual switching action,  $\hat{t}_i$ , the linearized impact on  $\hat{x}[n+1]$  is derived by finding the instantaneous perturbation in states  $\Delta x_{ssi}$  generated from from  $\hat{t}_i$ ,

$$\Delta x_{ssi} = (A_i X_{ssi} + B_i U) \hat{t}_i - (A_{i-1} X_{ssi} + B_{i-1} U) \hat{t}_i,$$
(6)

then propagating the state perturbation through the remainder of the period to find the perturbation in the states at the end of the period resulting from  $\hat{t}_i$ 

$$\Delta x_{di} = \left(\prod_{k=16}^{i} e^{A_k t_k}\right) \cdot \Delta x_{ssi}.$$
 (7)

The models (6)-(7) for each of the 16 subinterval perturbations are combined to generate  $F_q$ . In order to prevent the rectifier from producing significant DC or harmonic components, the modulation pattern is constrained to a quarter-period symmetric staircase waveform. Fig. 3 shows the resulting possible perturbations on a half-period of the rectifier  $v_{rec}$  waveform. A phase perturbation  $\hat{t}_p$  shifts all switching instances uniformly, while a modulation perturbation  $\hat{t}_{mn}$  to level  $n \in \{1,2,3\}$  decreases the duration of that level while remaining centered in the half-period.

There is a different forced response for each type of modulation perturbation that acts on the system,  $F_q \in \{F_p \ F_{m1} \ F_{m2} \ F_{m3}\}$  and  $t_q \in \{t_p \ t_{m1} \ t_{m2} \ t_{m3}\}$ . Each component column vector in  $F_q$  is derived by summing the associated time perturbations. For example, perturbations in phase or in modulation level one yield

$$F_p = \sum_{k=1}^{16} \frac{\Delta x_{di}}{\hat{t}_i},$$
 (8)

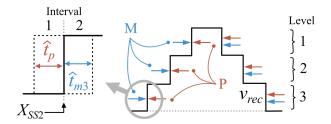


Fig. 3. Modulation (M) and phase (P) type control actions around steady state  $v_{rec}$  resulting in time perturbations  $\hat{t}_{mn}$  and  $\hat{t}_p$ , respectively.

$$F_{m1} = \sum_{k \in 8, 16} \frac{\Delta x_{di}}{\hat{t}_i} - \sum_{k \in 2, 10} \frac{\Delta x_{di}}{\hat{t}_i}.$$
 (9)

The transfer functions from each modulation perturbation to the states at the end of the period are then

$$G_{xq} = (zI - N)^{-1} F_q. (10)$$

 $G_{xq}$  is a vector of length 11, each element of which is a transfer function from a control action q to one of the states in  $\hat{x}[n+1]$ . Isolating the output voltage state,  $v_{Cout}$ , characterizes how the output is affected by a control perturbation:

$$G_{vq} = C_{iso7} \cdot (zI - N)^{-1} F_q.$$
 (11)

 $C_{iso7}$  is a vector that isolates the  $7^{th}$  index  $(v_{Cout})$  by zeroing all others. Transfer functions  $G_{vq}$  are the plant models to be used when designing the output regulation loop. To accomplish frequency synchronization, the plant model must be expanded to include sensed zero-crossing information.

# B. Phase Transfer Functions

Frequency and phase regulation are accomplished by sensing power stage waveforms. A zero-crossing detector (ZCD) is placed across the secondary-side capacitor to measure the zero-crossing events of  $v_{Cs}$ , and the ensuing ZCD square wave is a function of the WPT carrier frequency,  $f_{wpt}$ . The sensed square wave is fed into the controller as a frequency and phase reference. The small signal model is designed with this sensing strategy in mind, and the resulting transfer functions are derived to quantify the change in time of the zero-crossing resulting from changes in modulation pattern.

In steady-state, the zero crossing of  $v_{cs}$  occurs at time  $t_z$ . The state vector at this instant is  $X_{ssz}$ . During a transient, the small-signal state vector at this instant is

$$\hat{x}_z[n] = H\hat{x}[n] + J_q\hat{t}_q[n],$$
 (12)

where  $\hat{x}[n]$  are modeled by (4). Note that, although (12) is sampled once per switching period, like (4), the sampling point of  $\hat{x}_z[n]$  is the zero-crossing instant, rather than the beginning of the switching period. Thus, H and  $J_q$  only include perturbations and propagation from the beginning of the period to the zero-crossing event, rather than over the complete period.

Matrix H is given by

$$H = e^{A_{i_z} t_z} \cdot \prod_{i=i_z-1}^{1} e^{A_i t_i}, \tag{13}$$

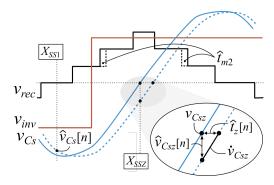


Fig. 4. Steady state waveforms (solid) with a perturbation on level 2  $(\hat{t}_{m2})$  and the resulting change in  $v_{Csz}$ . The linear projection using the steady state slope,  $\dot{v}_{Csz}$ , gives the change in zero-crossing,  $\hat{t}_z$ .

where  $i_z$  is the index of the interval within which the zero-crossing event occurs and  $t_z$  is the time of the zero-crossing referenced to the beginning of the  $i_z$ <sup>th</sup> interval. The change in x due to a single perturbation is given by

$$\Delta x_{dzi} = e^{A_z t_z} \prod_{k=i_z-1}^{i} \left( e^{A_k t_k} \right) \cdot \Delta x_{ssi}. \tag{14}$$

Likewise, matrix  $J_{m2}$ , for example, is given by

$$J_{m2} = -\sum_{k \in 3} \Delta x_{dzi},\tag{15}$$

when  $\hat{t}_3$  is the only perturbation within control action q=m2 that occurs before the zero crossing interval,  $i_z$ .

The transfer functions from control changes to the state variables at the zero-crossing event are given by

$$G_{xzq} = H(zI - N)^{-1}F_q - J_q. (16)$$

The state of interest is  $v_{Cs}$ , so the isolation vector is applied to give the relevant transfer function:

$$G_{vcszq} = C_{iso9} \cdot G_{xzp}. (17)$$

Transfer function  $G_{vcszq}$  describes how voltage  $v_{Cs}$  changes at the steady state zero-crossing as a result of control action q. Fig. 4 shows this change as  $\hat{v}_{Csz}$  for a change in modulation of the  $2^{nd}$  rectifier level (q = m2).

For frequency synchronization, the goal is to define the relationship from a control action to the affected zero-crossing event, and in Fig. 4, the zero-crossing point is changed by  $\hat{t}_z[n]$ . The slope of the steady state secondary capacitor voltage at the zero-crossing event,  $\dot{v}_{Csz} = A_{iz}X_{ssz} + B_{iz}U$ , is used as a linear projection to approximate  $\hat{t}_z$  as a function of  $\hat{v}_{Csz}$ . The final transfer function from control action q to the change in zero-crossing time  $\hat{t}_z$  is

$$G_{zq} \equiv \frac{\hat{t}_z}{\hat{t}_q} = G_{vcszq}/\dot{v}_{Csz}$$

$$= C_{iso9} \cdot \left(H(zI - N)^{-1}F_q - J_q\right)/\dot{v}_{Csz}.$$
(18)

Equations (12)-(17) culminate in (18) which gives a novel *time-to-time* transfer function. Here,  $G_{zq}$  is used to address the

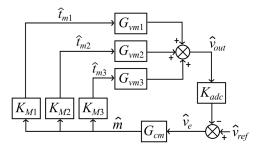


Fig. 5. The control loop for output voltage regulation isolated from the rest of the system.

synchronization problem by characterizing how the switching actions of the plant affect the sensed ZCD signal.

With four types of control actuation and two circuit characteristics being sensed, there are a total of eight transfer functions for the plant. These characterize how modulations of phase and each of the three  $v_{rec}$  levels affect both  $v_{Cout}$  and the zero-crossing of  $v_{Csz}$ . Table I summarizes the plant transfer functions that are used in designing the control loops in Section IV.

# IV. ISOLATED CONTROL LOOPS

The output regulation and frequency synchronization control loops are first examined separately. Phase modulation is used to synchronize phase and frequency, and the three modulation levels are used to regulate the output voltage. In reality, either type of actuation will have an affect on the other control loop through the transfer functions in Table I. Here, these affects are ignored and the loops are isolated as a starting point for control design.

# A. Output Voltage Regulation

The 7-level rectifier is able to modulate any of its three levels during the half-period. Because the three levels can be individually actuated, each is individually considered before they are each added together to represent the total change in output voltage,  $\hat{v}_{out}$ . Fig. 5 shows the isolated output regulation loop. The small signal gain of the 11 bit, 3.3 V analog-to-digital converter includes the gain of a 2:1 resistor divider,  $K_{adc} = (1/2) \cdot 2048/3.3$ .

The reference  $(v_{ref})$ , compensator  $(G_{cm})$ , and modulators  $(K_{M1}, K_{M2}, \text{ and } K_{M3})$  are all implemented digitally. The input to the modulators is an unsigned 11 bit variable (range: 1 to 2048), and the modulators output the PWMs that control each rectifier level. The modulation scheme that maps the 11 bit input to the on-time of each level is seen in Fig. 6 where M1, M2, and M3 are the half-period on-times of each respective level. The distributions of M1, M2, and M3 across the 11 bit input are assigned strategically so that the total gain across the sum of the three modulations is constant across all control points. The small signal gains of the modulator levels are calculated using the approximated slopes shown by the dotted lines. Note that the modulator gains  $(K_{M1}, K_{M2}, \text{ and } K_{M3})$  each change as the steady state operating point lies

### Sensed Circuit Characteristic

			Output Voltage, $\hat{v}_{Cout}$	$V_{Cs}$ Zero-Crossing Time, $\hat{t}_z$
	Phase,	$\hat{t}_p$	$G_{vp} = C_{iso7}(zI - N)^{-1}F_p$	$G_{zp} = C_{iso9} \left( H(zI - N)^{-1} F_p - J_p \right) / \dot{v}_{Csz}$
Control	Level 1,	$\hat{t}_{m1}$	$G_{vm1} = C_{iso7}(zI - N)^{-1}F_{m1}$	$G_{zm1} = C_{iso9} (H(zI - N)^{-1} F_{m1} - J_{m1}) / \dot{v}_{Csz}$
Actuation	Level 2,	$\hat{t}_{m2}$	$G_{vm2} = C_{iso7}(zI - N)^{-1}F_{m2}$	$G_{zm2} = C_{iso9} (H(zI - N)^{-1} F_{m2} - J_{m2}) / \dot{v}_{Csz}$
	Level 3,	$\hat{t}_{m3}$	$G_{vm3} = C_{iso7}(zI - N)^{-1}F_{m3}$	$G_{zm3} = C_{iso9} (H(zI - N)^{-1} F_{m3} - J_{m3}) / \dot{v}_{Csz}$

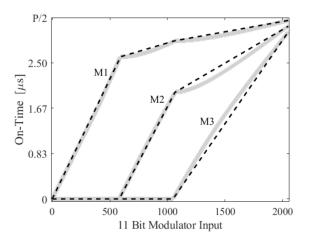


Fig. 6. Modulation scheme of the 7-level switched capacitor rectifier.

within one of the three regions determined by introducing each modulation level.

The compensator is designed in the z domain using only powers of 2 so that it can be implemented with minimal resources and time delay in the digital controller. The discrete compensator is

$$G_{cm} = \left(\frac{z^{-1}}{1 - (1 - 2^{-5})z^{-1}}\right) \left(\frac{-2^{-15}z^{-1}}{1 - z^{-1}} + \frac{2^{-9}z^{-1}}{1 - (1 - 2^{-7})z^{-1}}\right),$$
(19)

where the design assumes a given clock speed (20 MHz, here) such that the resulting difference equation has the desired frequency characteristics. The loop gain of the system is

$$T_{out} = K_{adc}G_{cm}$$

$$(K_{M1}G_{vm1} + K_{M2}G_{vm2} + K_{M3}G_{vm3}).$$
(20)

Fig. 7 shows a bode plot of the uncompensated loop gain, the compensator transfer function, and the final loop gain after compensation. The loop gain has a crossover frequency of  $f_{c-out}=2.99$  kHz and a phase margin of  $\phi_{m-out}=64.4^\circ$ . The discrete time model is accurate well past a crossover

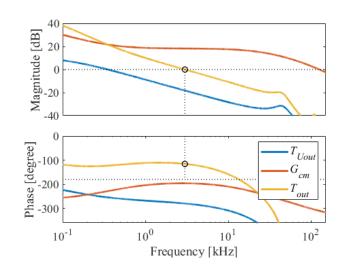


Fig. 7. Plot of the uncompensated loop gain  $(T_{Uout})$ , compensator  $(G_{cm})$ , and loop gain  $(T_{out})$ .

frequency of 2.99 kHz, but Fig. 7 shows the plant a right-half-plane zero around 10 kHz, limiting the achieve able bandwidth from this compensator structure.

# B. Phase and Frequency Synchronization

The frequency synchronization control scheme is shown in Fig. 8, where the phase-frequency detector (PFD), compensator (comp), and digitally controlled oscillator (DCO) make up the PLL. The zero-crossing detector reports the carrier frequency,  $f_{wpt}$ . The PFD compares this signal to the output of the PLL  $(f_{pwm})$  and generates a 3-level signal containing information about the two signals' phase difference. This phase difference is compared to a reference, an error is generated, and the compensator converts the error signal into a reference for the DCO. The output of the DCO is sent to both the power circuit PWM signals and the input of the PLL for phase comparison. The PFD, summation, compensation, and DCO blocks are all implemented digitally inside the controller.

The small-signal model of the system in Fig. 8 is shown in Fig. 9. The DCO changes its oscillation frequency by adding or subtracting clocks to change its period length,  $f_{pwm} = f_{clk}/N_{clks}$ , where  $f_{clk}$  is the clock frequency and  $N_{clks}$  is the

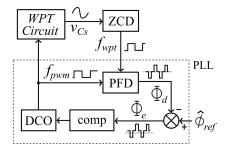


Fig. 8. Block diagram of the control circuitry responsible for synchronizing the rectifier switching frequency,  $f_{pwm}$ , to the WPT carrier frequency,  $f_{wpt}$ .

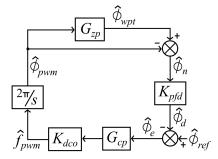


Fig. 9. Small signal representation of the frequency synchronization control loop.

number of clock periods at the steady state operating point. Therefore,  $K_{dco} = -f_{clk}/N_{clks}^2$ .

The functionality of the PFD results in multiple blocks in the diagram. First,  $K_{pfd}=N_{clks}/2\pi$  converts from units of radians to units of clock edges. Next, the  $2\pi/s$  gain converts the frequency of the  $\hat{f}_{pmw}$  square wave in Fig. 8 to phase  $\hat{\phi}_{pwm}$ .

The way the discrete time model is derived means that the zero-crossing detector is included within  $G_{zp}$ . Because  $\hat{t}_z/\hat{t}_p = \hat{\phi}_z/\hat{\phi}_p$ ,  $G_{zp}$  is unaltered when using phase, rather than time, to describe the system.

The total loop gain of the small signal model in Fig. 9 is

$$T_{freq} = K_{pfd}G_{cp}K_{dco}\frac{2\pi}{s}(G_{zp} - 1), \qquad (21)$$

where compensator  $G_{cp}$  is designed for the desired crossover and phase margin. The compensator is designed in the same manner as  $G_{cm}$ , relying on a known digital clock frequency and powers of 2 for implementation.  $G_{cp}$  is

$$G_{cp} = \left(\frac{2^{-21}}{1 - z^{-1}}\right) \left(\frac{2^{-11}}{1 - (1 - 2^{-8})z^{-1}}\right). \tag{22}$$

This gives a loop crossover frequency of  $f_{c-freq} = 7.08$  kHz and a phase margin of  $\phi_{m-freq} = 58.6^{\circ}$ . The compensator and final loop gain are shown in Fig. 10.

# V. EXPERIMENTAL VALIDATION

# A. Hardware Setup

An experimental wireless power system is constructed to test the design. The complete circuit design includes the

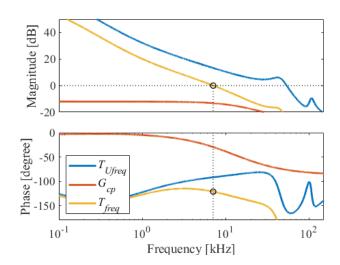


Fig. 10. Frequency synchronization uncompensated loop gain  $(T_{Ufreq})$ , compensator  $(G_{cp})$ , and final loop gain  $(T_{freq})$ .

#### TABLE II CIRCUIT PARAMETERS

Parameter	Value			
$L_{tx}$	$10.78~\mu\mathrm{H}$	_	$L_{rx}$	12.11 $\mu { m H}$
$C_p$	221 nF		$C_s$	95 nF
$R_p$	155 m $\Omega$		$R_s$	390 m $\Omega$
Coupling, $k$	0.50		$C_{A1}$ - $C_{B3}$	$15.66~\mu F$
Device	BSZ0910NDXTMA1		$C_{out}$	$27.41~\mu F$
Gate Driver	MP1907AGQ-P			

TABLE III STEADY STATE OPERATING POINT

$V_{in}$	$V_{out}$	$\phi_{ref}$	M1	M2	M3	$P_{out}$	$\eta$
10 V	2 V	$-67.7^{\circ}$	$2.99 \ \mu s$	$2.25~\mu s$	$1.33~\mu s$	4.54 W	84.12 %

inverter, tuned wireless power tank, 7-level MSC rectifier, and two Altera De0-Nano FPGA controllers (FPGA: Cyclone® IV EP4CE22F17C6N). Fig. 11 shows the circuit setup, and Table II outlines the main component characteristics.

An impedance analyzer is used to measure the flying capacitor value of  $15.66~\mu F$  at 150~kHz with a DC bias of 5 V. Similarly, the LCR parameters of both the primary and secondary sides of the WPT tank are measured at 150~kHz as well. The coupling value of k=0.5 is calculated based on tank measurements of either side while the opposite side is unloaded and a measurement of the primary side while the secondary side is shorted.

The steady state power waveforms are validated by comparison to the state space model in Fig. 2. The small signal experiments are carried out at the operating point given in Table III.

# B. Isolated Output Regulation

In order to test the design in (20), the inverter and rectifier are both driven synchronously by FPGA 1 so that no control is needed for frequency synchronization, isolating the output

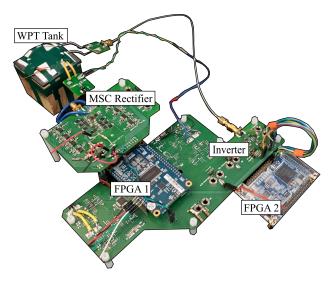


Fig. 11. Experimental prototype.

regulation control loop. The compensator is built in MATLAB Simulink and then exported to a VHDL file and uploaded to the control FPGA. Due to the digital implementation, creating a step-change in the voltage reference is a simple clock-edge command that triggers  $v_{ref}=616$  to change to  $v_{ref}=596$ . This 20 integer difference in  $v_{ref}$  is equivalent to a -0.0645 V change in the steady state operating point.

Fig. 12 shows the experimental result of the isolated output loop compared to the small signal prediction. The test demonstrates good agreement with the model, showing that the methods used are accurate.

# C. Isolated Frequency Synchronization

To isolate the frequency synchronization loop the modulation index is fixed, and both FPGA controllers are used. FPGA 2 drives the inverter, and FPGA 1 drives the rectifier, with no communication between the two. The zero-crossing detector in [5] is used to sense  $v_{Cs}$ .

For comparison to the model, the system is set for a step-change in  $\phi_{ref}$  from -188 to -198, where these numbers denote the number of clock edges and correspond to -188 = -67.7° and -198 = -71.3°, respectively. Experimental waveforms are extracted from the oscilloscope and imported into MATLAB. Waveform data is interpolated to increase the sampling resolution, the phase difference is calculated along the length of the experimental data, and the result is reported in Fig. 13 with the small signal prediction overlaid.

A simulation is included in Fig. 13 to illustrate that limit-cycling in the experimental data is expected due to the limited resolution of the DCO and PFD. Fig. 13 proves that the model predicts the dominant dynamics of the system.

#### VI. DUAL-LOOP OPERATION

In a real wireless power transfer system both the frequency synchronization and output regulation control loops need to operate simultaneously. The two isolated that have been experimentally verified in isolation considering only the effects

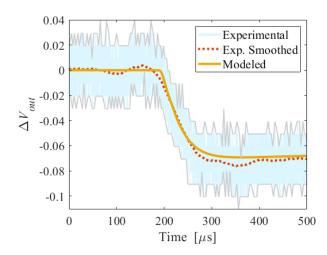


Fig. 12. Experimental vs. modeled response to a step change in  $v_{ref}$  for the design in Fig. 7.

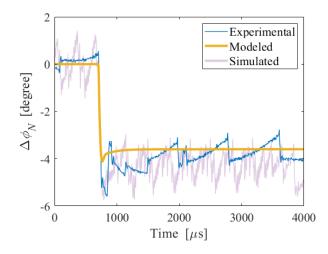


Fig. 13. Experimental vs. modeled vs. simulated response to a step change in  $\phi_{ref}$  for the design in Fig. 10.

of four of the eight plant transfer functions in Table I. The other four transfer functions describe how the two loops are coupled together. Modulation of any of the levels influences the phase of the system via  $G_{zm1,2,3}$ . Likewise, a change in phase affects the output voltage at the rectifier load via  $G_{pv}$ . The two isolated control loops are employed simultaneously to examine the feasibility of dual-loop control.

Fig. 14 shows a load step from 2.2 A to 1.8 A. The system regulates the output and remains frequency synchronized during the load step. Fig. 14 illustrates the viability of running both loops in a single system. Future work will consider further detail of designing high-bandwidth, stable dual-loop operation.

# VII. CONCLUSIONS

The benefits of 7-level rectifier WPT systems can only be fully leveraged when both frequency synchronization and load regulation are achieved in closed-loop. Discrete time state

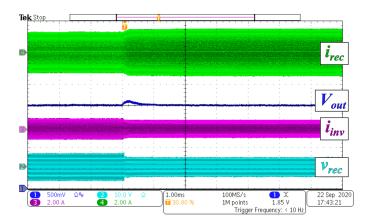


Fig. 14. Steady state dual loop operation with a load step from 2.2 A to 1.8 A.

space models are developed to accurately predict both small-signal and large-signal converter operation. A novel linear projection method is adopted to develop transfer functions from the control actions to the zero-crossing time of the secondary capacitor voltage. The eight transfer functions encompass the small signal plant model.

The isolated output regulation and frequency synchronization control loops are individually modeled, designed with kilohertz bandwidths, and verified with step responses. The cross-coupling plant transfer functions are then considered, and the viability of dual-loop control is demonstrated experimentally. The discrete time design approach is shown to be a valid technique with which to address real-world control implementation for active rectifiers in WPT systems.

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