Active Rectifier Design and Synchronization Control for 6.78 MHz Wireless Power Transfer

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***Abstract*— In wireless power transfer systems, active rectifiers demonstrate improved efficiency and regulation capability. To enable impedance or output regulation, ensure stable operation, and maximize the efficiency, switching actions of the rectifier have to be synchronized with the magnetic field generated from the transmitter coil. This work presents an implementation of a phase-locked-loop synchronization controller using commercial components, including a low-cost microcontroller. A discrete-time small-signal model is used to derive the transfer function of the inherent feedback and design a compensator stabilizing the synchronization loop. Large-signal state-space modeling is used to design a high-efficiency, soft-switching, 6.78MHz power stage. A low-profile, 40W, GaN-based rectifier prototype is designed and built to experimentally verify the ability to synchronize and achieve high efficiency due to soft-switching.**

Keywords—wireless power transfer, state-space discrete-time modeling, active rectifier, frequency synchronization

I. INTRODUCTION

Active rectifiers have been studied for application as wireless power transfer (WPT) receivers due to their superior efficiency, controllability, and ability to compensate for detuning of the WPT link due to parasitic reactive loading [1]. The latter is particularly important in loosely-coupled, multi-receiver WPT where variations in coupling due to the spatial location of the receivers, or the presence of conductive elements in the field may alter the transmitter load reactance, degrading efficiency [2]. Active rectifiers with impedance-regulation can compensate for varying operating conditions and retune the network to maximize end-to-end WPT efficiency [3]. In order to accomplish this, the rectifier must first synchronize switching actions to the WPT field, then dynamically vary its phase to produce a reactive load. Despite the challenges, loosely coupled WPT applications offer greater spatial freedom of charging location, which is desirable for consumer electronics applications.

Class-E rectifiers are used widely for low-harmonic rectification in WPT systems operating at 6.78 MHz and above [4]. However, these converters have limited controllability without loss of soft-switching or require large filtering elements that are not suitable for low-profile applications, including consumer electronics. A low-THD, 6.78 MHz zero-voltage switching (ZVS) Class-D rectifier with impedance control is presented in [5]. This topology, shown in Fig. 1, uses a resonant tank to produce low-harmonic soft-switching waveforms which maintain ZVS across a designed range of phases. The low-THD waveforms aid in ensuring EMI-compliance without requiring additional filtering between the receiver coil and the power stage.

Previous attempts to synchronize the rectifier resulted in unstable operation at low power [5]. At lower frequencies, synchronization has been demonstrated using additional signaling hardware [6], magnetic field sensing [7], or phase-locked loops (PLL) [8]. Recent work in [8] showcases a discrete-time modeling framework that predicts the full dynamics of a PLL-based synchronization controller but is demonstrated only on low-frequency 150 kHz systems with tightly-coupled coils. The model in [8] neglects the rectifier deadtime by assuming the rectifier input voltage is a square wave. In high-frequency applications, it is critical to maintain ZVS to prevent excessive switching loss, and ZVS transitions may occupy a non-negligible portion of the 6.78MHz switching period.

In this paper, the modeling approach of the synchronization loop dynamics in [8] is improved by incorporating the resonant interval and the state-dependent switching actions using generalized discrete-time state-space techniques [9]. In addition, the parasitic elements of various power transistors and passive components are included in the converter model to facilitate the component selection process and find the optimal operating condition yielding the highest efficiency. A compact PLL synchronization control network using low-profile commercial components is designed and demonstrated. A 6.78MHz GaN-based rectifier prototype delivering an output power of 40W is built to validate the proposed analysis.

The outline of this paper is as follows. Section II describes the circuit topology, models steady-state operation, and

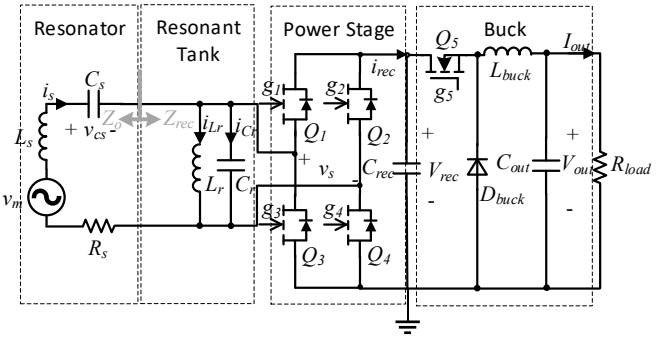

Fig. 1. Circuit schematic of the proposed rectifier.

presents an approach to hardware design for high efficiency. Section III models the synchronization loop dynamics and presents a compensator design for stable synchronization. Experiments are carried out to validate the proposed analysis in Section IV. Section V concludes and provides potential future improvements to this work.

II. Power Stage Model and Design

A. Circuit Topology

Fig. 1 shows the schematic of the full-bridge active rectifier in a series-series resonant WPT system. The circuit is comprised of a resonator, auxiliary resonant tank, active rectifier, and buck converter. The receiver coil L_s, capacitor C_s and equivalent series resistor R_s are connected in series forming a resonant network that has a resonant frequency $f_o = 1/(2\pi\sqrt{L_sC_s})$, which is near the operating frequency f_s. An auxiliary resonant tank consisting of L_r and C_r in parallel is added at the rectifier input to assist the ZVS achievement and keep the THD of the secondary voltage $v_s(t)$ low [10]. C_r is the equivalent parasitic capacitance of switches and any additional capacitance. $Z_{rec} = R_{rec} + jX_{rec}$ is the equivalent load impedance seen by the resonator. $Z_s = R_s + jX_s$ denotes the open-circuit impedance of the resonator.

In order to maximize coil-to-coil efficiency, the total reactance must be nulled ($X_{rec} = -X_s$) and R_{rec} must be set to the optimal value [11]. As mentioned, the active rectifier can alter $Z_{rec}$by controlling its switching timing to adjust the input phase ϕ_{v_s,i_s}. However, having ϕ_{v_s,i_s} as the only control parameter is not sufficient to separately change both reactive and resistive parts of the equivalent load impedance. A dc/dc buck converter is cascaded at the rectifier output to provide an additional control parameter, rectified voltage V_{rec}, while maintaining the desired output voltage V_{out} at the load. In mobile electronics applications, this additional stage could be replaced by the battery charger.

The transmitter is designed to keep the sinusoidal current amplitude constant [12], which induces a constant ac voltage $v_m(t)$ on the secondary side, serving as the input source of the receiver. Since the induced voltage frequency f_m is identical to the transmitter switching frequency f_s with a phase offset, f_m is also considered as the reference frequency for the synchronization control.

B. State-space Discrete-time Model of Power Stage

Operating waveforms of the rectifier are modeled using a time-varying state-space description. To find steady-state operation, the discrete-time technique is employed, requiring the input $v_m(t)$ to be constant during each switching interval. Therefore, $v_m(t)$ is approximated as a square waveform, as shown in Fig. 2. The error induced by this approximation is minimal as long as a high-Q resonance between L_s and C_s at 6.78MHz is achieved.

There are six intervals per period. Regarding the first half of the waveform, intervals I and II are transition times where the drain-to-source capacitances of each transistor are charged by the resonant tank inductor current i_{Lr} before the switches are turned on to achieve full ZVS. Interval III is the power-delivery duration where two switches are on, forming a path to deliver current to the load.

The state-space representation of the rectifier circuit during the i^{th} interval is

$$\dot{\mathbf{x}}(t) = \mathbf{A}_i\mathbf{x}(t) + \mathbf{B}_i\mathbf{u}(t), \tag{1}$$

where $\mathbf{x}(t)$ is the state vector consisting of five states $[v_{cs}(t)\ i_{Lr}(t)\ v_{rec}(t)\ v_s(t)\ i_s(t)]^T$ and $\mathbf{u}(t) = [v_m(t)\ I_{rec}]^T$ is the input vector. PLECS [13] is used for extracting state-space matrices, $\mathbf{A}_i$ and $\mathbf{B}_i$, of the linear equivalent circuit during each interval.

For invertible matrix $\mathbf{A}_i$, by leveraging anti-symmetric rectifier waveforms, and the sampling frequency of $f_s/2$, the steady-state state vector $\mathbf{X}_0$ at the beginning of the period and the continuous state vector expression within each interval $\mathbf{x}(t)$ are obtained as follows [8]

$$\mathbf{X}_0 = \mathbf{I}_{\text{HC}}\left(\mathbf{I} - \prod_{i=3}^{1} e^{\mathbf{A}_i t_i}\right)^{-1} \sum_{i=1}^{3}\left(\prod_{j=3}^{i+1} e^{\mathbf{A}_j t_j}\right)\mathbf{A}_i^{-1}(e^{\mathbf{A}_i t_i} - \mathbf{I})\mathbf{B}_i\mathbf{u}_i. \tag{2}$$

$$\mathbf{x}(t) = e^{\mathbf{A}_i t}\mathbf{x}_{i-1} + \mathbf{A}_i^{-1}(e^{\mathbf{A}_i t} - \mathbf{I})\mathbf{B}_i\mathbf{u}_i, \tag{3}$$

where $\mathbf{A}_i$, $\mathbf{B}_i$, and $\mathbf{u}_i$ are the system matrix, input matrix, and input vector, respectively, during interval i. Whereas $\mathbf{x}_{i-1}$ is the state vector at the end of interval $i-1$. $\mathbf{I}_{\text{HC}} = \text{diag}(-1,-1,1,-1,-1)$ is the square diagonal matrix accounting for the opposite polarity of ac waveforms in the second half of T_s. From (2) and (3), complete steady-state waveforms of the rectifier are constructed for any given operating conditions.

C. Steady-State Efficiency Modeling

Because the rectifier is designed to achieve full ZVS, the hard-switching loss is eliminated. The power loss then consists of the resonant tank inductor conduction loss $P_{Lr,cond}$, core loss $P_{Lr,core}$, and transistor conduction loss P_{cond}.

In this topology, the resonant tank inductor current $i_{Lr}(t)$ has a high-frequency ac waveform with a large RMS value, causing a significant loss. The resonant tank inductor L_r is

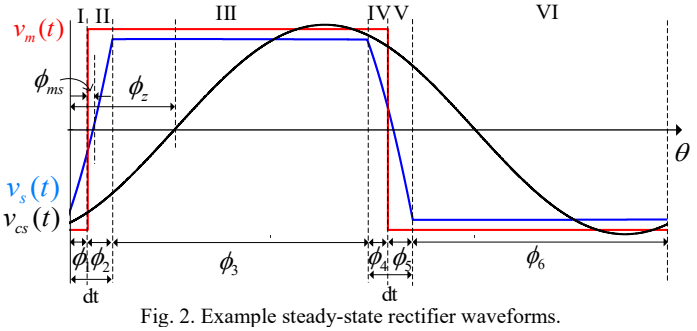

Fig. 2. Example steady-state rectifier waveforms.

fabricated in the lab by wrapping the magnetic wire around a low-profile high-frequency toroid core [14]. The core loss on the inductor is calculated using the empirical data provided by the manufacturer,

$$P_{L_r,core} = \left(\frac{f_s}{\frac{a}{B_{pk}^3} + \frac{b}{B_{pk}^{2.3}} + \frac{c}{B_{pk}^{1.65}}} + dB_{pk}^2 f_s^2 \right) V_e, \tag{4}$$

where *a, b, c, d* are coefficients of the core material provided by the manufacturer. The peak ac magnetic flux density B_{pk} is

$$B_{pk} = \frac{E_{rms} 10^8}{4.44 A_e N_{turn} f_s}, \tag{5}$$

where $A_e$is the cross-sectional area of the core, V_e is the core volume, N_{turn} is the number of coil turns, and E_{rms} is the RMS value of the sinusoidal inductor voltage.

As the coil resistance varies with the frequency, the inductor ac resistance R_{ac} needs to be derived as a function of f_s in order to compute the inductor conduction loss at 6.78 MHz. It is important to note that, at high frequencies, R_{ac} is drastically increased due to the skin and proximity effects. Based on Dowell's approximation approach for finding R_{ac} [15], which has been validated in many studies [16], [17], the inductor ac resistance is obtained

$$R_{ac} = R_{dc}\alpha \left[\frac{e^{2\alpha} - e^{-2\alpha} + 2\sin(2\alpha)}{e^{2\alpha} + e^{-2\alpha} - 2\cos(2\alpha)} + \frac{2(m^2-1)}{3} \frac{e^{\alpha} - e^{\alpha} - 2\sin(\alpha)}{e^{\alpha} + e^{\alpha} + 2\sin(\alpha)} \right], \tag{6}$$

where the factor α is

$$\alpha = \left(\frac{\pi}{4}\right)^{\frac{3}{4}} \frac{d^{\frac{3}{2}}}{\delta\sqrt{p}}, \tag{7}$$

and $R_{dc} = \rho l/A$ is the inductor dc resistance, δ is the conductor skin depth at 6.78 MHz, *m* is the number of centrical layers of the winding, *d* is the wire diameter, and p is the pitch between adjacent winding turns. Because no dc component is present in the inductor current, R_{ac} is incorporated directly in the state-space model to find the inductor conduction loss.

Because this work does not consider coil design, the resistive loss of the coil is subtracted from the power supplied by v_m to obtain the input power to the rectifier circuit,

$$P_{in} = f_s \int_0^{T_s} (v_m(t) i_s(t) - i_s(t)^2 R_s) dt, \tag{8}$$

Then, the output power and converter efficiency are

$$P_{out} = f_s \int_0^{T_s} (v_{rec}(t) i_{rec}(t)) dt, \tag{9}$$

$$\eta = \frac{P_{out}}{P_{in} + P_{core}}. \tag{10}$$

D. Optimal Efficiency and Power Component Selection

The process of finding the rectifier steady-state optimal operating condition and selecting components are shown in Fig. 3 and described as follows. A group of low R_{on} GaN FETs with rated blocking voltage ranging from $1.2V_{rec}$ to $4V_{rec}$ are pre-selected.

Since the transistor drain-to-source capacitance C_{ds} is nonlinear and dependent on the drain-to-source voltage v_{ds}, the charge-equivalent linearized value at a given V_{rec} value is used,

$$C_{ds,eq} = \frac{1}{V_{rec}} \int_0^{V_{rec}} C_{ds}(v_{ds}) dv_{ds}. \tag{11}$$

For each GaN device being evaluated, the amplitude of $v_m(t)$ stays constant and L_r value is swept by iterating N_{turn}on the selected core. At each L_r value, inductor ac resistance R_{ac} is calculated using (6)-(7). Then R_{ac} , $C_{ds,eq}$ and R_{on} are incorporated in the state-space model to calculate the rectifier power loss in steady-state. For each hardware candidate, t_1 and t_2 are simultaneously iterated until full ZVS and the desired output power are achieved. The rectifier efficiency is then computed by using (8)-(10) and compared with that at other operating points to find the maximum efficiency yielded from an individual FET.

Fig. 4 shows the rectifier efficiency and input phase resulting from a single GaN FET with varying L_r . The efficiency increases at higher L_r due to reduced current i_{Lr}, resulting in lower core and conduction loss. However, reducing i_{Lr} results in less available current to assist in obtaining ZVS, leading to a reduced range of phases over which the converter can maintain ZVS. To prevent the design from requiring excessive reactive loading of the transmitter to obtain ZVS, the rectifier input phase is limited to $\pm 15°$ in this application. The red circle in Fig. 4 indicates the optimal operating point for the given GaN device.

Finally, the GaN FET and the corresponding L_r value resulting in the highest efficiency are selected for building the converter. Selected components and parameter values are listed in Table I in Section IV.

III. Synchronization Control Design

The principle of this PLL-based synchronization control is to sense a periodic signal related to the input $v_m(t)$ and generate an output signal that is phase-locked to the input signal, resulting in equal frequencies. The PLL output signal is then used to drive the switching actions of the rectifier. Fig. 5

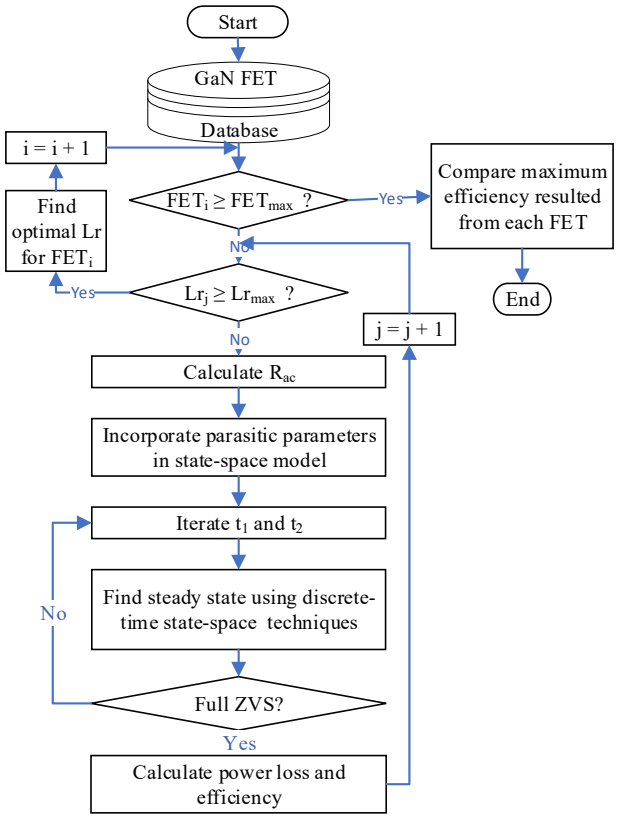

Fig. 3. Rectifier efficiency optimization process.

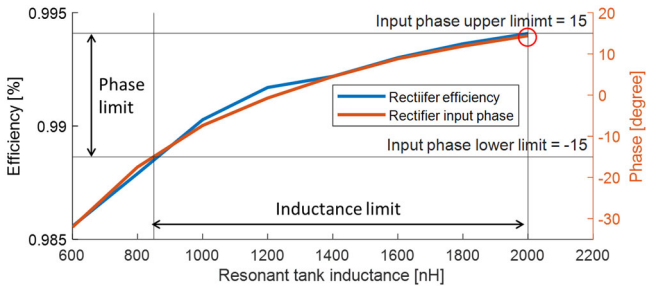

Fig. 4. Rectifier efficiency with varying L_r.

shows the structure of the on-board PLL-based synchronization control consisting of a phase-frequency detector (PFD), a charge pump (CP), a compensating loop filter $G_c(z)$, a microcontroller (MC), and a digitally controlled oscillator (DCO).

Improved from work in [5], which senses the noise-susceptible secondary current $i_s(t)$, the receiver-side tuning capacitor voltage $v_{cs}(t)$ being sensed in this work is relatively large and out of phase with the rectifier switching actions when the rectifier load is nearly resistive. As a result, the PLL has a high immunity to switching noise, even at low power, ensuring the proper functionality in wide loading conditions. This advantage is also demonstrated in [18], [8].

The phase information of $v_{cs}(t)$ is extracted by detecting its zero-crossing point using a zero-crossing detector (ZCD) to generate a reference signal $v_{ZCD,ref}(t)$. This signal is then fed to the PFD, along with the PLL output signal $v_{DCO,fb}(t)$, to

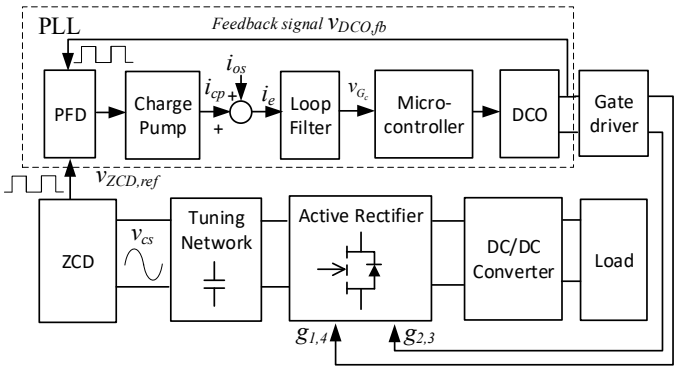

Fig. 5. Synchoronization control structure.

measure their phase difference ϕ_{PFD}. The PFD controls the charge pump to output current pulses $i_{cp}(t)$ whose average value is proportional to ϕ_{PFD}. The phase between $v_{ZCD,ref}(t)$ and $v_{DCO,fb}(t)$ can be locked to each other but separated by a phase offset ϕ_{os} by either injecting or withdrawing amount of current i_{os} at the CP output. The resultant current pulse i_e, which is proportional to the phase error ϕ_e, is fed to the analog compensator/loop filter $G_c(z)$ to convert to a voltage level v_{G_c} corresponding to ϕ_e. The compensator $G_c(z)$ is designed to stabilize the loop and achieve a target bandwidth. A low-power microcontroller (MC) samples the voltage level v_{Gc} using the integrated analog to digital converter (ADC) module and generates communication signals controlling the output signal frequency of the digitally controlled oscillator (DCO). The DCO outputs two complementary signals used as PWM signals driving the switching actions of the rectifier. The deadtime dt between gate signals is set using a resistor-programmed gate driver. As mentioned above, one of the DCO outputs is also used as a feedback signal to the PFD, completing the closed-loop synchronization control.

To examine the stability of the synchronization loop, an analytical approach is developed in [8] to model the response of the sensed signal phase to the dynamics of the rectifier switching actions. An extended model is presented in this section, where the deadtime between rectifier switching states is taken into account. Also, an extra auxiliary parameter, i.e. t_2, is included in the model, to model the reverse conduction of GaN FETs clamping v_s to v_{rec} at the end of the resonant interval.

A. Power Stage Model

The small-signal state vector at sampling points derived using the discrete-time technique [9] has the form

$$\hat{\mathbf{x}}[n+1] = \mathbf{F}\hat{\mathbf{x}}[n] + \mathbf{\Gamma}\hat{\phi}_1[n] + \mathbf{\Lambda}\hat{\phi}_2[n], \qquad (12)$$

where $\hat{\mathbf{x}}[n+1]$ is the state deviation responding to perturbations in the previous state $\hat{\mathbf{x}}[n]$, control parameter $\hat{\phi}_1[n]$, and auxiliary parameter $\hat{\phi}_2[n]$. Since the input vector $\mathbf{u}(t)$ remains unchanged during each interval, inputs are not perturbed and not included in (12). Coefficient matrices $\mathbf{F}$, $\mathbf{\Gamma}$, and $\mathbf{\Lambda}$ are

$$\mathbf{F} = (e^{\mathbf{A}_3 t_3} e^{\mathbf{A}_2 t_2} e^{\mathbf{A}_1 t_1} \mathbf{X}_0)\mathbf{I}_{HC}, \tag{13}$$

$$\mathbf{\Gamma} = e^{\mathbf{A}_3 t_3} e^{\mathbf{A}_2 t_2} ((\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}_1 + \mathbf{B}_1\mathbf{u}_1 - \mathbf{B}_2\mathbf{u}_2)\frac{T_s}{2\pi}, \tag{14}$$

$$\mathbf{\Lambda} = e^{\mathbf{A}_3 t_3} ((\mathbf{A}_2 - \mathbf{A}_3)\mathbf{X}_2 + \mathbf{B}_2\mathbf{u}_2 - \mathbf{B}_3\mathbf{u}_3)\frac{T_s}{2\pi}. \tag{15}$$

To model the reverse conduction, the response of $v_s(t)$ at the end of the deadtime to perturbations is also analyzed. Because only the linear equivalent circuit is modeled during the deadtime in interval II, the FET drain-to-source voltage can take on spurious negative values if t_2 is not constrained to the correct value based on the large-signal transition to reverse conduction. To model this behavior, a constraint equation, $\sigma = 0$, is included in the model, where σ is generally a vector of constraint equations. In this case, only one constraint is included: the value of $v_s(t)$ at the end of t_2 is equal to V_{rec}, assuming the voltage drop on FETs is neglectable,

$$\begin{aligned}\sigma(t_1, t_2) = \ & \mathbf{C}_{v_s}(e^{\mathbf{A}_2 t_2} e^{\mathbf{A}_1 t_1}\mathbf{X}_0 \\ & + e^{\mathbf{A}_2 t_2}\mathbf{A}^{-1}(e^{\mathbf{A}_1 t_1} - \mathbf{I})\mathbf{B}_1\mathbf{u}_1 \\ & + \mathbf{A}^{-2}(e^{\mathbf{A}_2 t_2} - \mathbf{I})\mathbf{B}_2\mathbf{u}_2) - V_{rec} = 0\,,\end{aligned} \tag{16}$$

where $\mathbf{C}_{v_s} = [0\ 0\ 0\ 1\ 0]$ is used to select the desired state, v_s, from the state vector. When this constraint holds, during every period, $v_s(t)$ at the end of t_2 stays fixed at V_{rec} due to the reverse conduction of the FETs. The the small signal model of (16) is then

$$\hat{\sigma}[n+1] = \mathbf{C}_{v_s}\left(\mathbf{F}'\hat{\mathbf{x}}[n] + \mathbf{\Gamma}'\hat{\phi}_1[n] + \mathbf{\Lambda}'\hat{\phi}_2[n]\right) = 0, \tag{17}$$

where

$$\mathbf{F}' = \frac{\partial\sigma}{\partial x} = \mathbf{C}_{v_s} e^{\mathbf{A}_2 t_2} e^{\mathbf{A}_1 t_1}, \tag{18}$$

$$\mathbf{\Gamma}' = \frac{\partial\sigma}{\partial\phi_1} = \mathbf{C}_{v_s} e^{\mathbf{A}_2 t_2} ((\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X}_1 + \mathbf{B}_1\mathbf{u}_1 - \mathbf{B}_2\mathbf{u}_2)\frac{T_s}{2\pi}, \tag{19}$$

$$\mathbf{\Lambda}' = \frac{\partial\sigma}{\partial\phi_2} = \mathbf{C}_{v_s}((\mathbf{A_2} - \mathbf{A_3})\mathbf{X_2} + \mathbf{B_2}\mathbf{u_2} - \mathbf{B_3}\mathbf{u_3})\ \frac{T_s}{2\pi}. \tag{20}$$

Using the generalized state-space modeling technique [9], the linearized constraint equation (17) and small-signal model (12) are combined to obtain the equivalent small-signal form of the state vector

$$\hat{\mathbf{x}}[n+1] = \mathbf{F_{eq}}\hat{\mathbf{x}}[n] + \mathbf{\Gamma_{eq}}\hat{\phi}_1[n], \tag{21}$$

where

$$\mathbf{F}_{eq} = \mathbf{F} - \mathbf{\Lambda}(\mathbf{\Lambda}')^{-1}\mathbf{F}', \tag{22}$$

$$\mathbf{\Gamma}_{\mathrm{eq}} = \mathbf{\Gamma} - \mathbf{\Lambda}(\mathbf{\Lambda}')^{-1}\mathbf{\Gamma}'. \tag{23}$$

Then, the $\hat{\phi}_1[n]$ to $\hat{\mathbf{x}}[n+1]$ transfer function is

$$G_{x\phi_1}(z) = \left((z\mathbf{I} - \mathbf{F}_{eq})^{-1}\mathbf{\Gamma}_{eq}\right). \tag{24}$$

which incorporates the impact of the transistor reverse conduction and dead time during switching transitions.

B. Inherent Zero-Crossing Feedback Model

When the control parameter ϕ_1 is perturbed, small-signal states are propagated through the entire switching period, causing a deviation in the zero-crossing point t_z of $v_{cs}(t)$. Thus, to model the synchronization loop dynamic behavior, the transfer function from the control perturbation $\hat{\phi}_1[n]$ to the sensed zero-crossing phase deviation $\hat{\phi}_z$[n+1] is derived by following the modeling framework in [8].

$$G_{\phi_z,\phi_1}(z) = \mathbf{C}_{v_{cs}}\left(\mathbf{H}G_{x\phi_1}(z) + \mathbf{J}\right)\frac{2\pi}{T_s(-\dot{v}_{cs,z})}. \tag{25}$$

where

$$\mathbf{H} = e^{\mathbf{A}_3(t_z - t_2 - t_1)} e^{\mathbf{A}_2 t_2} e^{\mathbf{A}_1 t_1}\mathbf{I}_{HC}, \tag{26}$$

$$\begin{aligned}\mathbf{J} = & -e^{\mathbf{A}_3(t_z - t_2 - t_1)} e^{\mathbf{A}_2(t_2)}((\mathbf{A_1} - \mathbf{A_2})\mathbf{X_1} + \mathbf{B_1}\mathbf{u_1} \\ & - \mathbf{B}_2\mathbf{u}_2)\frac{T_s}{2\pi}.\end{aligned} \tag{27}$$

$\dot{v}_{cs,z}$ is the linearized slope of $v_{cs}(t)$ at the zero-crossing point t_z

$$\dot{v}_{cs,z} = \mathbf{C}_{v_{cs}}(\mathbf{A}_3\mathbf{X}_z + \mathbf{B}_3\mathbf{u}_3), \tag{28}$$

where $\mathbf{X}_z$ is the steady-state state vector at t_z and $\mathbf{C}_{v_{cs}} = [1\ 0\ 0\ 0\ 0]^T$.

C. Synchronization Loop Dynamics and Compensator Design

Fig. 7 shows a block diagram of the complete small-signal model of the synchronization loop, including the dynamics of the power stage. The loop gain of the synchronization loop is

$$\begin{aligned}&T_{sync}(z) \\ &= \left(-1 - G_{\phi_z,\phi_1}(z)\right)K_{PFD}G_c(s)K_{ADC}K_{DCO}\left(\frac{-2\pi}{s}\right)\left(\frac{1}{N}\right),\end{aligned} \tag{29}$$

where $\left(-1 - G_{\phi_z,\phi_1}(\mathrm{z})\right)$ presents the effective change in the input phase difference ϕ_{PFD} at the PFD resulting from $\hat{\phi}_1$.

The PFD gain is calculated by averaging the maximum CP output current over one period

$$K_{PFD} = i_{cp,\max}/2\pi. \tag{30}$$

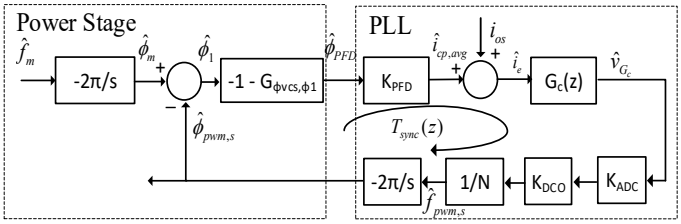

Fig. 7. Block diagram of the synchronization loop including the converter dynamics.

The gain of the ADC integrated into the microcontroller is the ratio between the digital output range and the input voltage level range

$$K_{ADC} = ADC_{out,\text{range}}/ADC_{in,\text{range}}. \tag{31}$$

The DCO gain depends on the operating frequency f_s and is linearized at steady state

$$K_{DCO} = \frac{f_{DCO}[n+1] - f_{DCO}[n]}{DCO_{in}[n+1] - DCO_{in}[n]}, \tag{32}$$

where $DCO_{in}[n]$ is the digital input value of the DCO setting the output frequency $f_{DCO}[n]$ to the steady-state operating frequency f_s, which is nearly 6.78 MHz in this application.

The $1/N$ gain in Fig. 7 models the frequency divider integrated into the PFD chip, which is used to reduce the feedback signal frequency. The fraction $-2\pi/s$ is the frequency-to-phase conversion gain in radians. The negative sign indicates the inverse correlation between $\hat{f}$ and $\hat{\phi}$. For the reference, negative $\hat{\phi}$ value implies the deviation to the left and vice versa.

Fig. 6 shows the bode plot of the uncompensated loop gain $T_{sync,un}$ that has a high phase margin of 90° and low bandwidth of 630 Hz. A compensator is required to increase the bandwidth for a faster response, while maintaining acceptable phase margin. Also, the compensated bandwidth must be at least a decade below the ADC rate and f_s to sufficiently attenuate the impact of nonlinear sampling behaviors and switching noise on the control. Therefore, the control bandwidth is targeted at 10 kHz. A Bode plot of the compensated loop gain T_{sync} is also shown in Fig. 6.

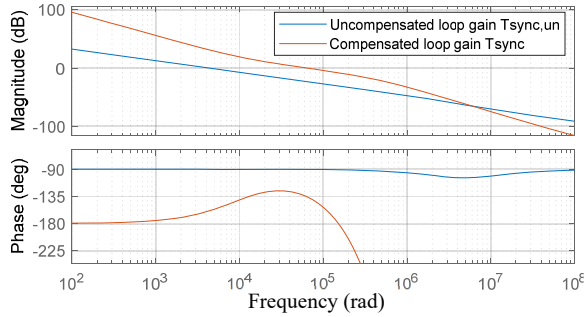

Fig. 6. Bode plots of $T_{sync,un}(z)$ and $T_{sync}(z)$.

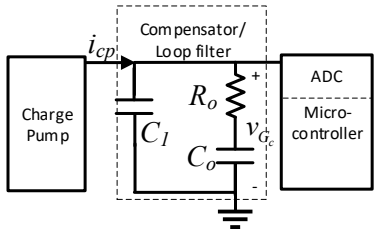

Fig. 8. Compensator circuit schematic.

Error! Reference source not found. shows the circuit of the compensator, which is a combination of an integral and a lead compensator. The integrator is used to convert the error signal i_e into v_{Gc} which is the reference to adjust the output frequency to bring the error down to zero. However, the pole in the integrator reduces the phase margin by 90°, causing the instability. Thus, the lead compensator is added to increase the phase margin to 45° The general transfer function of the compensator is obtained from the circuit

$$G_c(s) = \frac{\hat{v}_{G_c}}{\hat{\imath}_{cp}} = G_{c0}\frac{1 + \frac{s}{2\pi f_z}}{s\left(1 + \frac{s}{2\pi f_p}\right)}, \tag{33}$$

which has one zero and two poles. The compensator phase θ_{com} at the crossover frequency f_c is the difference between the desired phase margin $\theta_{desired}$ and the uncompensated phase margin $\theta_{T_{sync,un}}$

$$\theta_{com} = \theta_{desired} - \theta_{T_{sync,un}} - \theta_{delay} + \frac{\pi}{2}, \tag{34}$$

where $\pi/2$ and $-\theta_{delay}$ are added to compensate for the phase margin reduction due to the pole at dc and delay in PLL components. To realize θ_{com}, the pole and zero frequencies are chosen as follows [19]

$$f_z, f_p = f_c\sqrt{\frac{1 \mp \sin(\theta_{com})}{1 \pm \sin(\theta_{com})}}, \tag{35}$$

Then the compensator dc gain is

$$G_{c0} = \frac{s\left(1 + \frac{s}{2\pi f_p}\right)}{T_{sync,un}(j\omega_c)\left(1 + \frac{s}{2\pi f_z}\right)}, \tag{36}$$

where $T_{sync,un}(j\omega_c)$ is the uncompensated loop gain at the desired crossover frequency. With the full compensator transfer function being derived, compensator component values are calculated.

IV. Experimental Verification

Fig. 9 and Fig. 10 show the experimental setup of the closed-loop WPT system and the prototype, 6.78 MHz, 40W WPT receiver built to validate the proposed power stage and control

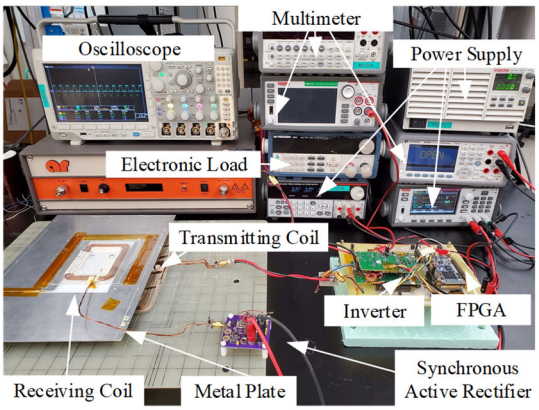

Fig. 9. Closed-loop experimental setup.

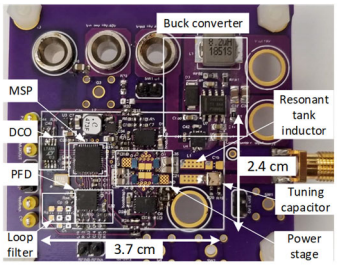

Fig. 10. Synchronous rectifier prototype.

design. Prototype component values and part numbers are listed in Table I.

TABLE I.
PROTOTYPE CIRCUIT PARAMETERS AND COMPONENTS

Parameter	Value	Component	Part
L_s	3.78 µH	GaN FET	EPC2007C
C_s	150 pF	Gate driver	LMG1210
L_r	2 µH	PFD	ADF4002
f_s	6.78 MHz	Microcontroller	MSP430F5172
P_o	40 W	DCO	LTC6903
$v_{m,pk}$	50.9 V	Buck converter	LMR14030
V_{rec}	40 V	Inductor core	T44-17
V_o	19 V		
C_1	0.16 µF		
R_0	16.24		
C_0	6.12 µF		

The transmitter consisting of a half-bridge inverter controlled by a DSP operates at 6.78 MHz and achieves ZVS at full load, as designed in [20]. In order to validate the loss model of the power stage, the experimental rectifier efficiency is compared to the analytical value in open-loop operation. Fig. 12 shows rectifier operating waveforms in open-loop, which have a good agreement with analytical waveforms, confirming the accurate steady-state model. However, it is difficult to accurately measure the input ac power of the rectifier from $v_s(t)$ and $i_s(t)$ waveforms at high frequencies because of non-ideal factors, including probes delays, probe error measurement, and harmonic contents. An improved approach to validate the power stage loss model is to measure the end-to-end efficiency of the entire open-loop WPT system. The input and output dc powers are accurately measured using precise

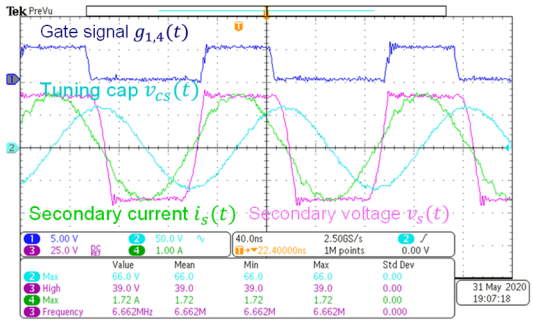

Fig. 12. Experiemtal waveforms of the rectifier in open-loop operation delivering 40W.

multimeters in Kelvin connections. The system efficiency is compared to that of a diode rectifier at a similar operating condition.

Fig. 11 illustrates the calculated and measured power loss breakdown of these two systems. Although there is a discrepancy between the model and measurement caused by parasitic elements, the power loss reduction is well predicted in the model. Using the designed active rectifier significantly reduces the total loss by nearly 1.75 W, which is 4.36% of the output power.

The transfer function $G_{\phi_z,\phi_1}(z)$ is validated by the experimental step response of ϕ_z to $\hat{\phi}_1$ in the open-loop setup. Waveforms are captured using the MDO3104 oscilloscope then imported to MATLAB to extract phase values. As shown in Fig. 10, the experimental result matches with the step response extracted from the analytical model (25), Simulink model, LTspice model. It is also more accurate compared with the

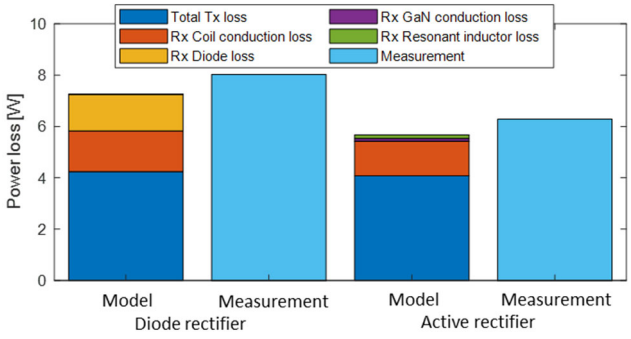

Fig. 11. Power loss breakdown of WPT systems consisting of a synchronous active rectifiifer and a diode rectifier.

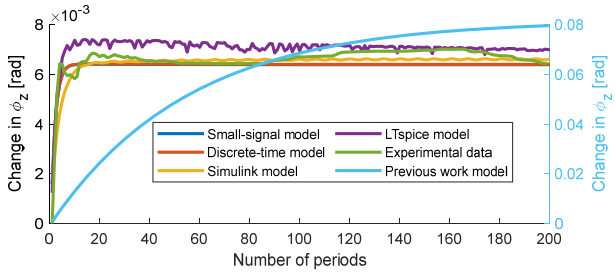

Fig. 10. Step response of G_{ϕ_z,ϕ_1} comparison between experimental results with different models and previous work model [11].

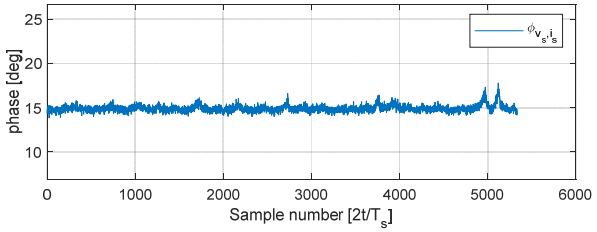

Fig. 13. Experimental rectifier input phase showing the synchronization.

model in the previous work [8], which does not account for the transition time and reverse conduction of GaN FETs.

In closed-loop, because there is no communication channel between the transmitter and receiver, the synchronization between them is accomplished by using the proposed control network on the secondary side. The PFD, CP, MC, and DCO listed in Table I are commercial ICs. The PFD and CP are combined in one chip, which also has an integrated ZCD used to detect the reference signal phase. The MSP430F5172 microcontroller samples the voltage level from the compensator using a 10-bit ADC module at the sampling rate of 220 kHz. The DCO employs the serial peripheral interface (SPI) protocol to communicate with the microcontroller and outputs complementary signals with frequencies ranging from 1 kHz to 68 MHz. The DCO delay is nearly 2.7 µs.

Finally, the rectifier input phase, i.e., the phase difference between $i_s(t)$ and $v_s(t)$, is plotted in Fig. 13 to demonstrate stable synchronization control. The signals $i_s(t)$ and $v_s(t)$ are locked in phase with a phase offset of 15°, as predicted by the model. The subtle jitter in the phase difference, resulting in an RMS error of 0.5°, is caused by quantization error from the ADC and DCO. Due to the robustness of the sensed signal $v_{cs}(t)$, the rectifier is able to synchronize from a low power of 0.05 W to the full power of 40 W.

V. Conclusion

In WPT systems, active rectifiers are synchronized with the magnetic field by sensing a local signal and generating synchronous driving signals controlling the rectifier switching actions. However, this controlling approach creates inherent feedback as the power stage dynamics alters the current and voltage waveforms, including the sensed signal. The previous study in [8] addresses this issue by proposing a modeling framework analyzing the dynamics of this feedback. Improving from that model, this work successfully accounts for the transient time and reverse conduction of GaN devices in the ZVS operation. A compact and low-cost synchronization control network based on PLL techniques is developed and built on the prototype board. An analog compensator is designed to stabilize the control loop. Furthermore, utilizing the power loss model, an optimization process for designing the power stage is proposed. Experimental results show a highly-efficient active rectifier and stable synchronization.

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