ADVANCED INTELLIGENT SYSTEMS
Open Access
www.advintellsyst.com

Efficient Defect Identification via Oxide Memristive Crossbar Array Based Morphological Image Processing

*Hee Sung Lee, Yongmin Baek, Qiubao Lin, Joseph Minsu Chen, Minseong Park, Doeon Lee, Sihwan Kim, and Kyusang Lee**

Defect identification has been a significant task in various fields to prevent the potential problems caused by imperfection. There is great attention for developing technology to accurately extract defect information from the image using a computing system without human error. However, image analysis using conventional computing technology based on Von Neumann structure is facing bottlenecks to efficiently process the huge volume of input data at low power and high speed. Herein efficient defect identification is demonstrated via a morphological image process with minimal power consumption using an oxide transistor and a memristor-based crossbar array that can be applied to neuromorphic computing. Using a hardware and software codesigned neuromorphic system combined with a dynamic Gaussian blur kernel operation, an enhanced defect detection performance is successfully demonstrated with about 10^4 times more power-efficient computation compared to the conventional complementary metal-oxide semiconductor (CMOS)-based digital implementation. It is believed the back end of line (BEOL)-compatible all-oxide-based memristive crossbar array provides the unique potential toward universal artificial intelligence of things (AIoT) applications where conventional hardware can hardly be used.

1. Introduction

Automated defect inspection technology has been widely investigated in a variety of fields, including the semiconductor and integrated circuit industry,[1–3] engineering and science,[4,5] and medical applications,[6,7] to overcome the drawbacks of manual detection methods, which are imprecise and time-consuming. Various image processing approaches of defect identification such as filtering, structuring, and statistical methods have been recently developed to recognize the defective information from input images.[8–10] However, most defects are of irregular shape and size, while the inspection area is large, and thus the complexity of the input data for defect inspection is usually high. Therefore, high computational power along with large power consumption and long processing times is generally required to operate defect identification algorithms using the von Neumann architecture based computing system due to a memory wall problem between the microprocessor and storage memory.[11] To ameliorate these issues, here we have used a nonvolatile memory based neuromorphic computing system that imitates the human brain's operation combined with a software algorithm for the defect identification process.[12,13]

Among them, memristor-based crossbar array based neuromorphic computing has received great attention due to its scalability and computing-in-memory features.[13–18] Cross-point structured memristors, nevertheless, have suffered from cell-to-cell interferences due to the sneak path currents through neighboring memristor pixels that lead to unnecessary power dissipation and inaccurate operations.[19] To precisely modulate the resistance of each memristor, the memristor-based array is usually integrated with a selector device (switching component) such as silicon (Si)-metal-oxide field-effect transistor (MOSFET), which is known as 1-transistor and 1-resistor (1T1R) structure.[20–23] The 1T1R architecture allows us to precisely program individual memristors using the

Dr. H. S. Lee, Y. Baek, J. Minsu Chen, M. Park, D. Lee, Dr. S. Kim, Prof. K. Lee
Department of Electrical and Computer Engineering
University of Virginia
Charlottesville, VA 22904, USA
E-mail: kl6ut@virginia.edu

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aisy.202000202.

DOI: 10.1002/aisy.202000202

Prof. Q. Lin
School of Science
Jimei University
185 Yinjiang Road, Xiamen, Fujian 36102, China

Prof. K. Lee
Department of Material Science and Engineering
University of Virginia
Charlottesville, VA 22904, USA

selectable input electric field controlled by the transistor gate without the cell-to-cell interferences. However, applications of Si-MOSFET-based 1T1R crossbar array systems are limited for the heterogeneously integrated artificial intelligence of things (AIoT) system due to the back end of line (BEOL) process incompatibility.[24,25] Although there are various alternative BEOL-compatible thin-film transistors (TFTs) such as oxide/organic TFTs that can fulfill large-area and flexible fabrication, they have yet to be demonstrated in neuromorphic system applications due to the insufficient electrical performance and poor reliability to operate the huge volume of artificial synapses in a neural network.[26] Here, to provide reliable and sufficient current-driving performance, we have used an indium (In)-rich indium zinc oxide (IZO)-based TFT[27–30] exhibiting high μ_{FE} of 50 cm^2 $(Vs)^{-1}$ as a selector that is BEOL process compatible in the memristive crossbar array. Then, hafnium oxide (HfO_2)[31,32] based memristors are integrated with IZO TFTs as a 1T1R pixel for the memristive crossbar array. The HfO_2 used as the active switching medium of the memristor also functions as a passivation layer of the IZO active channel; thus, the reliability of TFTs has been significantly improved without increasing the structural complexity of the 1T1R system. Moreover, the low leakage current (I_{OFF}) of the IZO TFT (two orders of magnitude lower than Si-TFT) in the 1T1R system can allow the potential availability for low-power computing applications requiring low leakage power consumption in unselected lines under heavy training operation.

Using the fabricated memristive crossbar array combined with a morphological image process algorithm,[33,34] we demonstrated a defect identification with about 10^4 times more power-efficient computation compared to an identical conventional central processing unit (CPU)-based process. Particularly, we complemented a unique hardware-based dynamic Gaussian blur kernel[35,36] operation with the defect identification process algorithm that allows us to vary the sigma value of a 2D Gaussian curve to precisely generate defect information. By combining neuromorphic hardware and software algorithms, we have demonstrated a power-efficient and accurate defect identification performance using morphological image processing. Successful identification performance has been confirmed by detecting the presence of defects from the various image sets, including fabric, brain tumor, graphene, and cupric oxide (CuO) thin film. Furthermore, our system is BEOL process compatible; thus, it provides the potential to be adapted in various applications that require limited fabrication conditions, including low temperature, large scale, and flexibility, which the conventional hardware cannot fulfill, toward universal AIoT applications.

2. Results and Discussion

2.1. Defect Detection Process

Morphological image processing is an image analysis technique that allows the detection of defects by identifying key shape characteristics while removing irrelevant background information. Through the image process, the unintentionally existing defect information can be extracted from the noisy background by thresholding the pixel intensity of the preprocessed image according to the size and shape based on the morphology.[33,34] However, the conventional morphological image operation has limitations in the perspective of accuracy because it usually only uses a single filter for the background segmentation process. **Figure 1**a schematically illustrates a flowchart of the conventional morphological image process (left) and our process (right). In the preprocessing stage, the input image was adjusted by applying denoising operations and by converting the full-color image into binary data. To achieve further accurate defect information, we used an averaging operation in addition to the conventional process by applying 3×3 dynamic Gaussian blur kernels as filters. We applied nine types of Gaussian blur kernels with a sigma value ranging from 0.7 to 1.1 using the programable memristive crossbar array. Weight values of each pixel in a Gaussian blur kernel was discretized into integers between 1 and 64 to match the available programing resolution of fabricated memristors that is discussed in a later section, as shown in Figure 1b. By performing the matrix convolution of a converted image with each kernel, nine denoised images were acquired. Then, to distinguish the defects from the background, the binarization process was subsequently performed by applying a threshold on the grayscale images through Otsu's algorithm.[37]

Following the preprocess stage described previously, we used the morphological image operations for defect identification. Detection of the defect areas can be achieved through a morphological image process via matrix multiplication of pixel information of the target image and a structuring element.[34] The structuring element is a diamond-shaped disk matrix consisting of 0s and 1s (shown in Figure 1a) that allows us to remove any details or regions smaller than the size of it through matrix multiplication. The results of this process confirm the existence of defects regardless of the shape and size of the defective area by varying the structuring matrix and the type of morphological operation. Specifically, we have used the morphological operations of dilation, erosion, opening, and closing, which are commonly used in defect detection (see Experimental Section and Supporting Information Note 2). The combination of these mathematical operations with the application of structuring elements can be used to identify defects from the images. The erosion and dilation operations are processed using kernel convolutions[38] via Boolean operations of XOR and. Here, we have used memristors to implement binary state kernels as the structuring elements to perform the erosion and dilation operations. Two types of diamond-shaped disks (shown in Figure 1a) were used as structuring elements. Figure 1c shows a comparison of the estimated power consumption of performing inference mode kernel operations with analog and digital implementations using the fabricated 1T1R system and a hypothetical digital circuit, respectively. Figure S1, Supporting Information, shows the approximated power consumption of the morphological image process using kernel operations with structuring elements for the analog and digital implementations. The kernel operation can be computed based on the multiply-accumulate (MAC) operation with a matrix convolution process. The digital implementation has been modeled as a system executing a sequential programming code using CPU and dynamic random-access memory. Then, we calculated the total CPU cycles required for MAC operation for each kernel by multiplying the basic unit cycle. For the analog implementation, we assumed the 1T1R

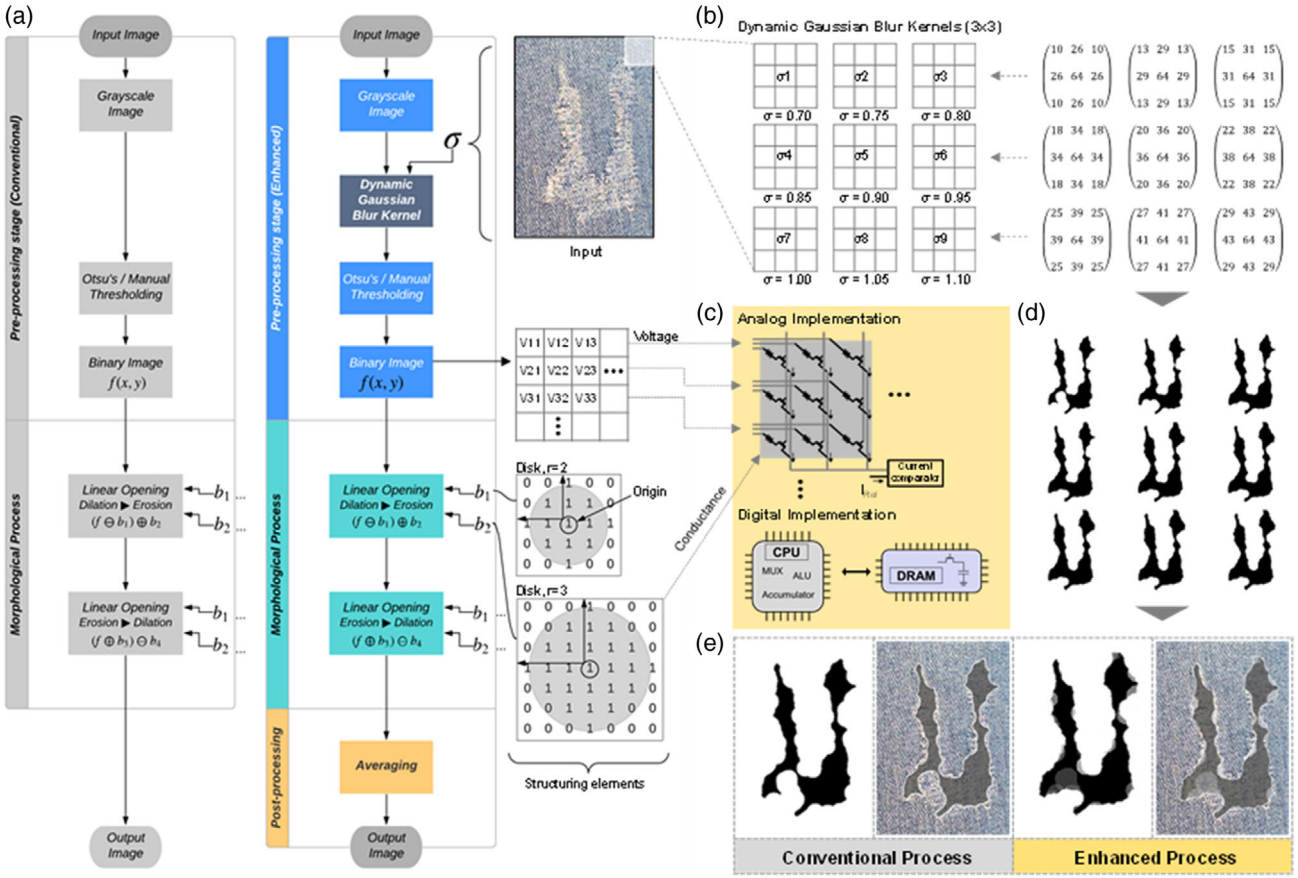

Figure 1. Scheme of the defect identification process. a) Schematic flowcharts of the conventional morphological image process (left) and our process (right). Our process consists of a preprocessing stage where the input image is processed by using a dynamic Gaussian blur kernel, a defect detection stage using morphological operations, and a postprocessing stage where the results are processed via an averaging schema that provides a gradient image of the defects. b) Dynamic Gaussian blur kernels with various sigma values, discretized into integers between 1 and 64. c) Schematic diagrams of analog (above) and digital (below) implementation performed using a fabricated 1T1R system and a hypothetical digital circuit, respectively. d) The nine outputs generated from the processes with nine types of Gaussian blur kernels. e) Comparison of detected defects processed by the conventional process (left) and our process (right).

memristive crossbar array based system operates at 1 MHz, output memristor current of 1 μA at low V_G, and input V_{read} of 0.2 V. The structuring element, realized by binary states of the memristor corresponding to the input voltage, was applied to each pixel of the image to process vector–matrix convolution for the MAC operation. Particularly, the digital-to-analog conversion (DAC) and multibit analog-to-digital conversion (ADC) units are not required for both cases because the kernel operations only have digital inputs and binarized outputs. As a result, the approximated inference mode power consumption shows that our memristive crossbar array based analog system enables about 10^4 times more power-efficient computing than conventional digital-circuit-based computing, regardless of the disk size, due to its computing-in memory architecture.[39] (See in Figure S1, Supporting Information, for details.)

In the postprocessing stage, an averaging schema was used to improve identification accuracy. The element-wise-averaging method[40] was used to combine the distributed intensity of extracted binary images using the following equation: $I_{average} = 1/n \sum_{i=1}^{n} I_i$, where I_i is ith image matrix, and n is the number of detected distributions. Figure 1b shows the process example of the fabric defect detected by the previously described method using the fabricated memristive crossbar array combined with software operation. We have applied the kernel operation using nine types of dynamic Gaussian blur kernels with varied sigma values ranging from 0.7 to 1.1 to the input image. (The sigma values higher than 1.1 have shown no significant difference in the output for the application of defect detection with the given size of our kernel.) The individual pixel weight value of kernels was discretized by 6 bits of information through the 1T1R memristor array. To program the kernel to the targeted sigma value, each pixel of the memristive crossbar array was set by a calibrated input voltage. Each output processed through programmed kernels with varied sigma values shows defect information. The segmentation process removes uninformative variations, and then the output is combined to provide an averaged value. The nine outputs processed by the blur kernels using the fabricated memristor array are shown in Figure 1d. Figure 1e shows the comparison of identified defects processed by conventional means and our method, respectively. The result

processed by conventional operation using a fixed sigma value of 0.7 was insufficient to provide accurate defect information due to the difficulty in extracting the defective area from the background. In contrast, the defect information more effectively reconstructed the defect information using multiple sigma values by updating the weight value of each memristor in the array. The extracted grayscale output image in Figure 1e exhibits the defect information.

2.2. Structural and Electrical Properties of the 1T1R Pixel

To precisely modulate the resistance of individual memristors in the array for the kernel operation in the defect detection process, we fabricated a 1T1R memristive crossbar array. The 1T1R pixel in the crossbar array consists of a series connection of an IZO TFT and a HfO_2 memristor. The optical microscope image of the 5×5 1T1R pixel array integrated on a sapphire substrate is shown in **Figure 2**a. All pixels are interconnected as a matrix in the array to operate parallel convolution computing. To enhance the driving current through the oxide TFT, we applied an interdigitated design[41] of the source (S)/drain (D) electrodes with the channel width/length (W/L) ratio of 50/5 (see zoomed scanning electron microscope (SEM) image of Figure 2a). The pixels in the same row share the gate electrodes of TFTs, while the parallel column lines connect the top electrode (TE) and bottom electrode (BE) of each memristor, respectively. Figure 2b schematically illustrates the device structure of the fabricated 1T1R single pixel. The IZO oxide TFT was designed as an inverted staggered structure[42] with an Al_2O_3 gate insulator and a bottom-gate electrode. A 5 nm thick HfO_2 layer was deposited simultaneously using the atomic layer deposition (ALD) process on top of both the IZO TFT back-channel and the 25 nm Pt/3 nm Ti BE as a passivation layer and as an active medium of the memristor, respectively. As shown in the inset of Figure 2b, the HfO_2 layer covered on the IZO back-channel can effectively prevent the oxygen-related atomic diffusion that can cause degradation issues in oxide semiconductors. In this structure, the Pt/Ti is used as a common electrode which forms the drain contact of the IZO TFT and the BE of the HfO_2 memristor in series. The current compliance of the memristor is controlled by the applied gate voltage of the connected IZO TFT to precisely tune the weight values of the memristor.

Figure 2c shows the transfer characteristics (drain current (I_D) versus gate voltage (V_G) measured at drain voltages (V_D) of 0.1 and 1 V) of the single IZO TFT. To enhance the carrier mobility, we deposited the In-rich IZO (In_2O_3–10 wt% ZnO) as the active channel layer of the n-type oxide TFT by using a DC magnetron sputter at room temperature. As shown in the inset of Figure 2c, the IZO TFT exhibited high μ_{FE} of 50 $cm^2 (Vs)^{-1}$ at V_D of 0.1 V, which is approximately five times higher than that of commonly used oxide TFTs based on an indium gallium zinc oxide (IGZO)[43] and zinc oxide (ZnO)[23] TFTs. The 1T1R system based on such oxide semiconductors can hardly operate the memristor due to its insufficient driving current.[23,43] The IZO TFT shows high enough I_D of 0.1 to 10 mA at V_D of 1 V depending on V_G ranging from −5 to 10 V, which is sufficiently high to program the resistance of the HfO_2 memristor. Furthermore, the IZO TFT shows a low subthreshold gate swing, an enhancement mode threshold voltage (V_{th}), and a low off-current (I_{OFF}) of 0.15 V dec^{-1}, 0.8 V, and $\approx 10^{-13}$ A, respectively. (details are shown in Supporting Information Note 1) In particular, transformation of the TFT property from the depletion mode to enhancement mode was achieved by applying O_2 plasma treatment on the back channel of the IZO active layer to effectively compensate for the free electrons that are unintentionally generated from the In-rich composition of IZOs (see Experimental Section and Figure S2, Supporting Information).

The current–voltage characteristics of a HfO_2 memristor fabricated on top of the Pt/Ti drain electrode of the TFT is shown in Figure 2d. Before measurement, an electroforming process was performed to obtain reliable bipolar resistive switching behavior of memristors by applying a 5 V DC bias to the TE of Ta as shown in the dotted line of Figure 2d. The electroforming in oxide-based memristors is driven by induced conducting paths via migration of oxygen atoms.[44,45] The fabricated memristor exhibited a typical resistive switching I–V behavior, where the device is switched from a high-resistance state (HRS) to a low-resistance state (LRS) by applying a positive bias over the SET voltage (V_{SET}). The programmed LRS is retained during the voltage sweep back in a negative direction and switched to the HRS by applying the RESET voltage (V_{RESET}).

Moreover, the HfO_2 oxide layer coated on top of the TFT channel significantly improves the reliability of the oxide TFT. The external bias stress and ambient air conditions usually cause the conductance instabilities of oxide TFTs.[46,47] Under the bias stress conditions with constant V_G and V_D to turn on the transistor, an oxide TFT's performance is generally degraded by the gate electric field induced chemical reaction between ambient air and the back-channel surface of an oxide semiconductor. Especially, the degradation becomes more serious in a high-mobility oxide channel such as IZO.[47] Therefore, an effective passivation layer for the stable operation of an oxide TFT is essential to protect the chemical reaction and to precisely control the conductance state of a 1T1R system. In the 1T1R system, the 5 nm thick HfO_2 acts as the passivation layer to protect the back-channel surface of the IZO TFT as well as the active layer of the memristor. To confirm the effectiveness of HfO_2 passivation, the DC bias stress induced I_D degradation characteristic of the fabricated IZO TFT with and without the HfO_2 protecting layer was measured under ambient air conditions at the positive bias stress conditions (V_G and V_D were set to 10 and 1 V, respectively, at room temperature, and the stress duration was 10^4 s), as shown in Figure 2e. As the stress time increased, the I_D level of the IZO TFT without the HfO_2 passivation layer continuously degraded over two orders of magnitude, whereas the degradation behavior was dramatically improved by using the HfO_2 passivation layer to cover the back-channel surface of the oxide TFT. The measured results clearly indicate that the HfO_2 layer could enhance the stability of oxide TFTs.

The I–V characteristic of the 1T1R system, consisting of the HfO_2 memristor and IZO TFT in series, was measured under the application of 10 V gate bias, as shown in Figure 2f. The electroforming process was performed by doing a DC bias sweep from −3 to 3 V of the TE of the memristor (V_{mem}) before the measurement, as shown in inset curve of Figure 2f. The current flow to the memristor (I_{mem}) in the 1T1R pixel at the forward-biased regime is controlled by the driving current of the IZO

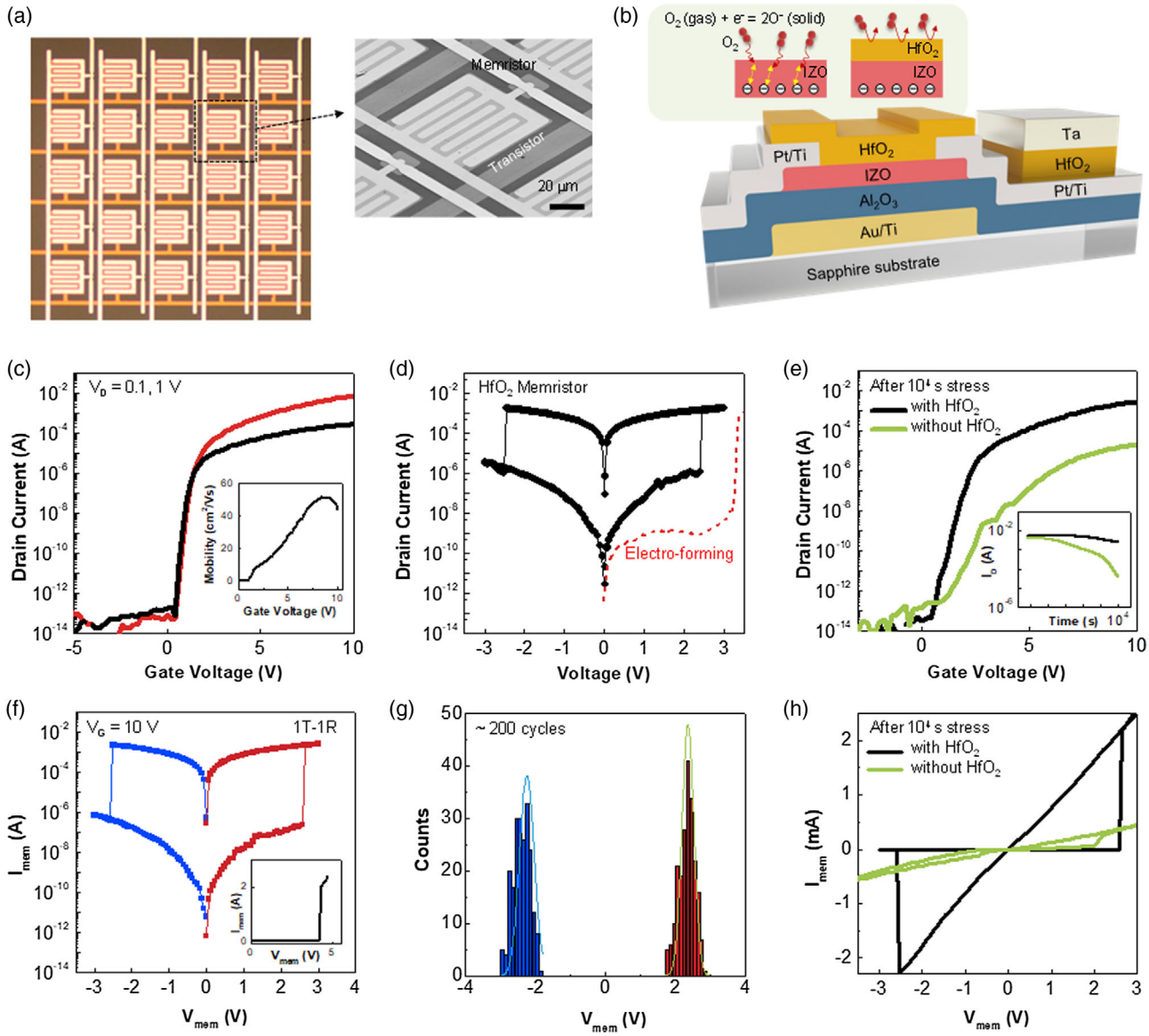

Figure 2. Structure and electrical properties of 1T1R pixel. a) Optical microscope image of the 1T1R array (left) and SEM image of the zoomed single 1T1R pixel (right). b) 3D schematic illustration of the 1T1R pixel consisting of an In-rich IZO TFT and a HfO_2 memristor. c) Transfer characteristics of the IZO TFT obtained at V_D of 0.1 and 1 V. The inset plot shows the field-effect mobility measured at V_D of 0.1 V. d) The *I–V* characteristics of a HfO_2 memristor fabricated on top of the Pt/Ti electrode of the TFT. The dotted line shows the electroforming operation. e) The DC bias stress induced transfer characteristics of IZO TFTs, with and without the HfO_2 protecting layer. The devices were stressed under the following conditions: V_G and V_D were set to 10 and 1 V, respectively, at room temperature, and the stress duration was 10^4 s. The inset shows I_D degradation properties of the TFTs. f) The *I–V* characteristic of 1T1R pixel obtained at V_G of 10 V. The inset shows the electroforming operation. g) The histogram of the SET and RESET voltage obtained from the *I–V* curves based on the 200 repetitive switching cycles. The statistical study of the SET and RESET voltage on the 1T1R pixel exhibited a general Gaussian distribution with a standard deviation sigma of both 0.2 at 2.35 and −2.25 V. h) *I–V* measurement of the 1T1R consisting of the bias-stressed IZO TFTs with and without HfO_2.

TFT tuned via V_G. The measured I_{mem} of the 1T1R system shows the *I–V* loop with two branches corresponding to the HRS and the LRS of the memristor, indicating that the fabricated IZO TFTs provide sufficient current to set the conductance of the connected memristor. To examine the repeatability of the 1T1R system, multiple cycling measurements were implemented. The *I–V* characteristics of the 1T1R pixel showed uniform SET and RESET operations during repeated DC voltage sweep cycles from −3 to 3 V of V_{mem} with a fixed V_G of 10 V (see Figure S3a, Supporting Information). Figure 2g shows the histogram of the SET and RESET voltage obtained from the *I–V* curves of the 200 repetitive switching cycles. The statistical study of the SET and RESET voltage on the 1T1R pixel exhibited a general Gaussian distribution with a standard deviation sigma of 0.2 at 2.35 and −2.25 V, respectively, indicating a uniform operation. As shown in Figure S3b, Supporting

Information, we also used endurance-cycling performance test with AC voltage pulses (500 ns width with fixed V_G of 2 V for SET, −2 V for RESET, and a read voltage of 0.2 V) for 10^3 cycles. The variation of HRS and LRS was consistent without remarkable degradation during the switching cycles. In addition, we demonstrated the *I–V* measurement of the 1T1R consisting of the bias-stressed IZO TFT without the HfO_2 layer to examine the effect of the HfO_2 passivation layer, as shown in Figure 2h. The electrical behavior of the 1T1R with the HfO_2-passivated TFTs was well preserved, showing the typical switching curve after 10^4 s bias stress time. However, in case of the 1T1R system with unpassivated TFTs, the memristor could not be completely reset after electroforming due to the degraded field effect mobility of the active layer.

2.3. Gate-Induced Current Modulation toward Kernel Operation

We have experimentally demonstrated precise control over the resistance state of the individual memristor in the 1T1R crossbar array by using the gate-induced current modulation of the integrated TFTs. **Figure 3**a shows I_D–V_G curves of the 1T1R pixel at a reading voltage of 0.2 V along with the resistance states set by V_G of the IZO TFT. Before the demonstration, the resistances of the memristor were programmed by set and reset processes with the IZO TFT using target V_G of 10 and 2 V. The I_D curve indicates distinct programmable current states of the HRS at V_G of 10 V and LRSs at V_G of 10 and 2 V, respectively. As the I_{OFF} of the fabricated IZO TFT is lower than 10^{-12} A, the oxide-based 1T1R system is capable of providing a wide operation window of programable weight values. The low leakage power consumption of oxide TFTs also makes it suitable for a wide range of low-power applications. The demonstrated all-oxide-based 1T1R system allows a hundred times more power-efficient computing compared to a Si-TFT-based system for the applications due to the low I_{OFF} and the high energy efficiency, which is even more effective when the size of the crossbar is large along with the heavy training operation (see Figure S4, Supporting Information). To confirm the feasibility of the current modulation of the oxide-based 1T1R system, we demonstrated continuous electrical tuning of the current states as shown in Figure 3b. By driving the IZO TFT with V_G ranging from the subthreshold to the high-electric-field regime (2–10 V), we were able to precisely select and modulate the 64 current levels (6 bits) through the memristor. Therefore, the on–off current ratio window of $\approx 10^3$ was achieved via the gate-induced modulation. The discretized current levels exhibited linearity over the applied V_G regime, as shown in Figure 3c. The linearly modulated behavior confirms that the resistance state of the memristor can be accurately tuned by an IZO TFT for dynamic kernel operation used in this work for the defect identification.

Furthermore, analog switching behavior was demonstrated by applying electrical pulses, similar to the weight update of biological synapses through potentiation and depression.[48,49] Figure 3d–f shows the incremental weight update characteristics of a fabricated 1T1R pixel measured by applying potentiation (rising) and depression (falling) pulses. We have applied both constant and incremental external bias pulse schemes to demonstrate the incrementally updated resistance properties of a 1T1R pixel. As shown in Figure 3d, the constant pulse scheme is a pulse sequence with a fixed set voltage in amplitude and frequency, while the incremental pulse scheme uses progressively increasing set voltage amplitudes at a fixed frequency.[48] The current value was monitored with a 0.2 V read pulse after each set or reset pulse. As shown in Figure 3e, when the constant pulse with 2 V amplitude and 500 ns width was applied, the current levels abruptly changed during both potentiation and depression processes. By contrast, the current levels changed almost linearly during weight updates when applying incremental bias pulses with 150 consecutive positive and negative pulses changed from 1.8 to 2 V and from −1.9 to −2.1 V, respectively, indicative of an ideal analog switching behavior as shown in Figure 3f. Furthermore, the gate-induced current modulation technique enables us to precisely tune the weight value window of the 1T1R device through the compliance current controlled by applying V_G of TFTs ranging from 2 to 10 V. The linear weight value update behaviors indicate that our 1T1R system based on oxide TFTs is a promising candidate for an electronic synapse for future analog computing applications that require a BEOL-compatible process.

For the demonstration of dynamic Gaussian blur kernel, we fabricated a 3×3 1T1R memristive crossbar array. Figure 3g shows the fabricated 3×3 1T1R array connected in series with IZO TFTs and HfO_2 memristors (Figure S5, Supporting Information, shows the *I–V* curves of all pixels in the array). To implement the dynamic Gaussian blur kernel operation, each pixel of the array was programmed by applying a targeted input V_G. Figure 3h shows one of the Gaussian blur kernels with a sigma value of 1.1 under reset and set conditions. The bottom graph of Figure 3h exhibits the measured current values of the 3×3 array based on the 64 linearly discretized states. As shown in the graph, the target current states could be precisely selected by set V_G with narrow distribution that allows accurate kernel operation. Figure 3i shows the in situ monitoring of the 1T1R array programming process, while measurement was performed with fixed read V_D and V_G of 0.2 and 5 V, respectively. Unit memristors in each pixel were programmed to the distinct resistive states for the target kernel operation using the biasing history described in Figure 3h. The read current, which is the accumulated current value obtained from each unit pixel's TE line, was increased stepwise and followed the used time domain bias scheme. This operation can be effectively expressed as the convolution process based on Ohm's law for vector–matrix multiplication and Kirchhoff's current law for summation.[50] This characteristic confirms the feasibility of the all-oxide-based memristive crossbar array for analog computing.

2.4. Demonstrations of the Defect Identification Process

We demonstrated the image filtering process via dynamic Gaussian blur kernel operation for the defect identification using the fabricated memristive crossbar array. To demonstrate the nine types of 3×3 Gaussian blur kernels varied by the sigma value, we simulated and measured the kernel maps based on the 6 bits programmed current states ranging from 10^{-7} to 10^{-4} A, as shown in **Figure 4**a. The nine types of Gaussian

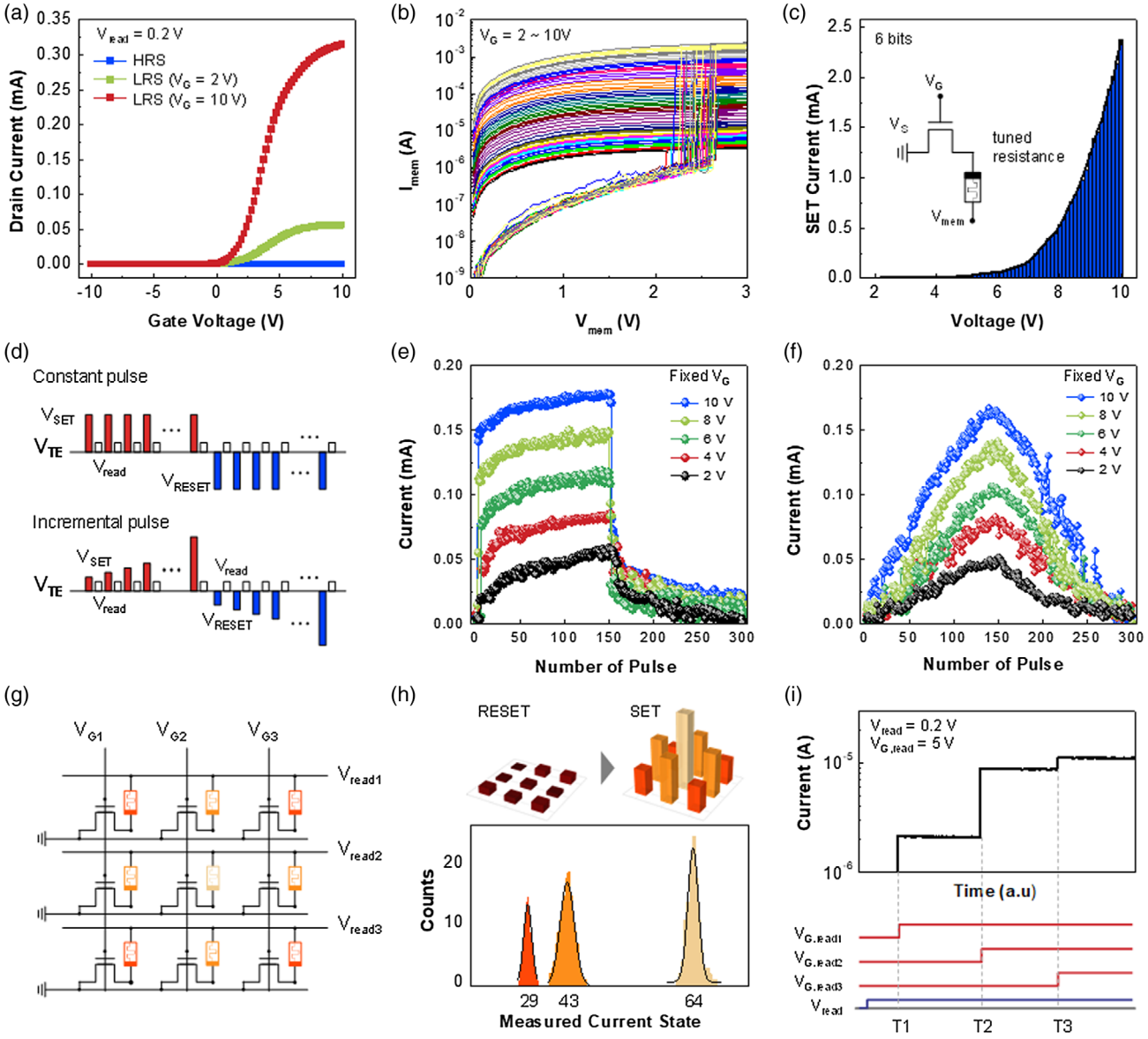

Figure 3. Gate-induced current modulation properties for the kernel operations. a) *I–V* characteristics of the 1T1R pixel at high- and low-resistance states obtained by applying a fixed reading voltage of 0.2 V and V_G of 2 and 10 V. b) *I–V* characteristics of the 1T1R pixel measured during the continuous electrical tuning of the memristor using gate-induced modulation. c) The plot of discretized 64 current (6 bits) states tuned by V_G. The inset diagram shows the 1T1R pixel circuit with designated resistance tuned by the IZO TFT. d) The constant and incremental external bias pulse schemes to demonstrate the linearly updated weight value of the memristor. The incremental weight update properties of our 1T1R pixel performed by e) constant and f) incremental pule scheme at V_G ranging from 2 to 10 V. g) Circuit diagram of our 3 × 3 1T1R array which connected in series with IZO TFTs and HfO_2 memristors. The color variation describes separately proposed resistances of memristor. h) The Gaussian blur kernel with a sigma value of 1.1 demonstrated by the memristive crossbar array. It is demonstrated by measured current values of the 3 × 3 array based on the calibrated 64 linearly discretized states. i) In situ monitoring of programed states of 1T1R array, while measurement was performed at the fixed read V_D and V_G of 0.2 and 5 V, respectively.

kernels mapped by the experimental readout current matrix accurately matched with the targeted sigma values of the simulated kernels (Figure S6, Supporting Information, shows all the experimental readout currents of kernels). Precisely tuned weight values of the blur kernel based on a memristor array confirmed the resistance modulation performance of the fabricated oxide-based 1T1R system for accurate kernel operation. We also demonstrated a 5 × 5 diamond-shaped disk consisting of binary components using the on and off operation of the 1T1R array for the linear opening and closing process, as shown in Figure 4b, showing a precise operation similar to the simulated matrix.

Figure 4c shows the processed output results, extracted from each processing step of the used defect identification process using the memristive crossbar array. The input image of a fabric was filtered by a Gaussian blur kernel to distinguish the defective pattern from the background. The tunable kernels with multiple

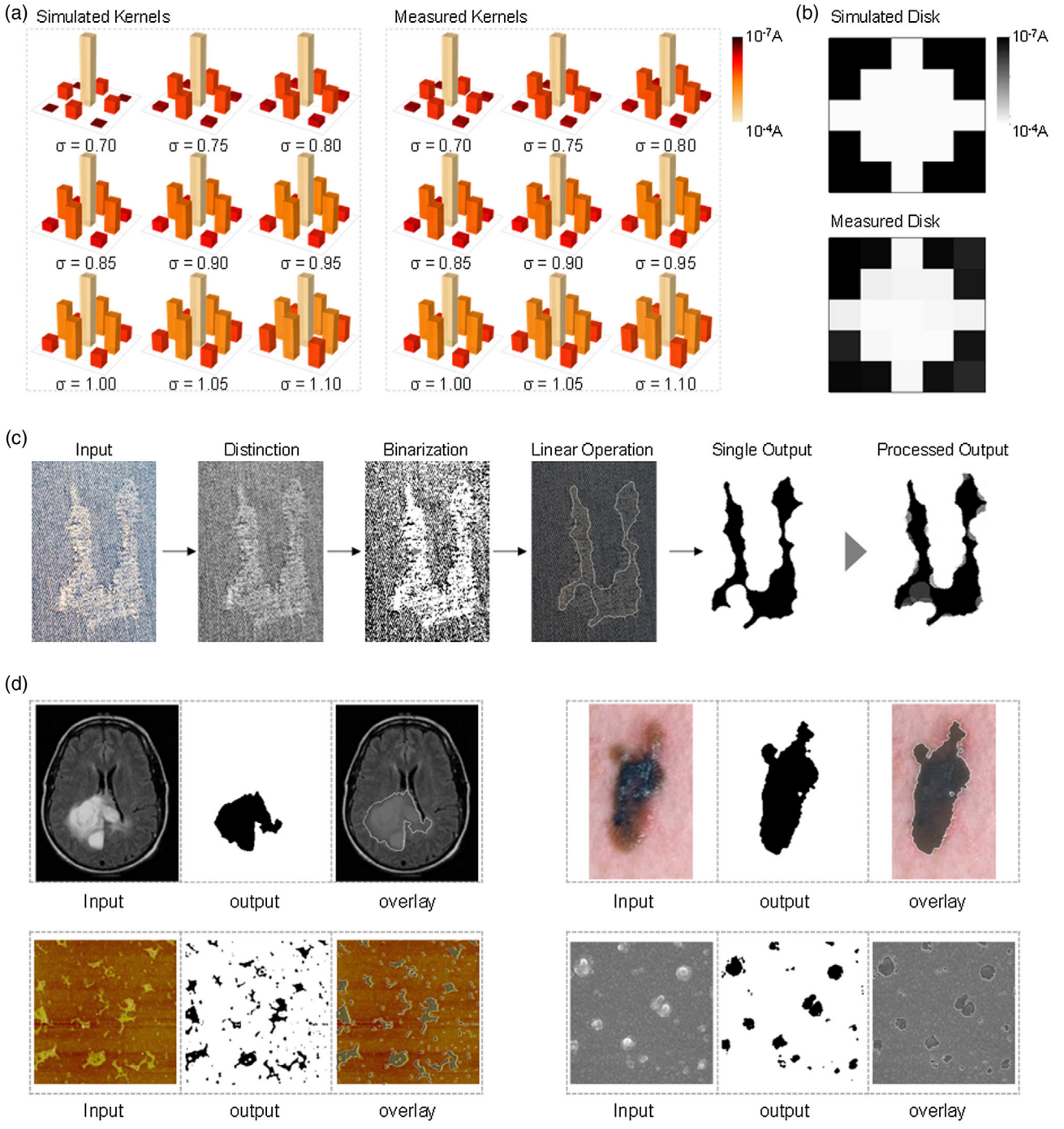

Figure 4. Demonstrations of the defect detection. a) Simulated and measured current map of the nine types of 3 × 3 Gaussian blur kernels programed by applying targeted V_G in 1T1R array. b) Simulated and measured current map of the 5 × 5 diamond-shaped disk for the MAC operation of the morphological image process. c) Processed output images extracted from each processing step of input, distinction, binarization, linear operation, and averaging, respectively. d) Additionally demonstrated results of brain tumor, skin cancer (called melanoma), CVD-grown graphene, and CuO thin film extracted by applying the defect detection process using the fabricated memristive crossbar array. The input, output, and overlapped images of each example are presented.

sigma values (here, ranging from 0.7 to 1.1) allow us to effectively distinguish the defect information from the background pattern. Then, the image was binarized by applying the thresholding process. The defect area was identified by implementing the morphological image process of dilation and erosion. This process was repeated using nine types of Gaussian blur kernels to yield nine outputs. Following, an element-wise-averaging method was applied to

reconstruct a single complete defect image from these nine outputs.

Our technique can be universally applied to various fields where defect identification is critical. To confirm the generality of the process, we have applied an identical computing process using a memristive crossbar array to medical and microscopic images as well. Figure 4d shows the processed images of brain tumor,[7] skin cancer (called melanoma),[51] chemical vapor deposition (CVD)-grown graphene,[52] and a CuO thin film[53] using the fabricated oxide-based 1T1R memristive crossbar system (Figure S7, Supporting Information, shows the nine different single output images generated from each demonstration). The processed output images from the various inputs display the identified defect information. These demonstrations indicate that a morphological process using memristive crossbar arrays can be effectively used for various applications, including those in industry, science, and medical areas.

3. Conclusion

In summary, we have demonstrated efficient defect identification using a morphological image process with low power consumption via a memristive crossbar array. The memristive crossbar array consists of 1T1R pixels fabricated with an In-rich IZO TFT and a HfO_2 memristor. The 1T1R system allows us to modulate the resistance of individual memristors in the array without cell-to-cell interference. The HfO_2 layer is used as the passivation layer for the oxide TFT channel to improve the reliability of IZO TFTs while it serves as an active switching medium of the memristor. Using the fabricated memristive crossbar array system, we have demonstrated defect identification via an analog computation process with lower power consumption compared to digital computation. To generate precise defect information, we have used additional pre- and postimage processing steps using unique hardware-based dynamic Gaussian blur kernels that allow us to extract accurate defect shapes with the gradient pixel information. Based on the approaches, we have successfully demonstrated the defect identification process using images excerpted from various fields including a fabric, brain cancer, CVD-grown graphene, and CuO thin film. We believe that the BEOL-compatible all-oxide-based memristive crossbar array provides a unique opportunity for neuromorphic hardware toward universal AIoT applications, including defect identification, where conventional hardware cannot be easily used.

4. Experimental Section

Fabrication of 1T1R Pixel Array: The 1T1R array was composed of IZO transistors and a HfO_2 memristor. The cross-section structure of the IZO transistor and Ti/Pt/HfO_2/Ta fabricated on a sapphire substrate is shown in Figure 2b. Although a sapphire substrate was used for an academic research purpose in this work, the device can be achieved on various substrates, including silicon and glass, without issues due to the high process compatibility of oxide-based semiconductors. For the fabrication of the IZO transistor, the Ti/Au back gate electrode (5/100 nm) was deposited by an e-beam evaporator. Then, a 100 nm thick Al_2O_3 film as a gate insulator was deposited on the patterned gate metal by ALD. Subsequentially, a 10 nm thick IZO thin film as a channel layer was formed by using DC-magnetron sputtering of In-rich IZO target (In_2O_3–10 wt% ZnO; the atomic percentage values of the indium, zinc, and oxygen were 29.01%, 13.74%, and 57.25%, respectively) with a deposition rate of 0.2 nm s^{-1}, where the gas volume ratio of $[O_2]/[Ar + O_2]$ was fixed to 0.2, followed by an annealing process at 250 °C for 1 h in an oven, and the channel layer was defined via photolithography and wet etching process by using a buffered oxide etchant (BOE). After the channel patterning, O_2 plasma treatment for the IZO film was performed at 200 W for 30 s to compensate for the exceeded oxygen vacancy. The 5/25 nm thick Ti/Pt was deposited as source and drain contacts of the transistor and BEs of the memristor by e-beam evaporation. Following the metallization, the 5 nm HfO_2 thin layer was formed by ALD, working as a passivation layer of transistor channel and switching medium for the memristor. The switching area was isolated from the passivation area via photolithography and wet etching process using BOE. Then, a 50 nm Ta metal as a TE of the memristor was formed via DC-magnetron sputtering and lift-off, forming a cross-junction.

Electrical Measurement: The DC electrical performance of the IZO transistor, HfO_2 memristor, and 1T1R array was characterized by using a Keysight B1500A Semiconductor Analyzer. The analog behaviors of the memristor and 1T1R array were measured using the Keysight B1500A, a pulse generator (Keysight 33600A), a transimpedance amplifier (Edmund 59-179), and an oscilloscope (Keysight DSOX3024T). The analog behavior of the 1T1R pixel was characterized using a pulsed signal with two types of bias schemes. The constant pulse modulation was performed at a fixed drain voltage of the transistor at ±2 V. On the other hand, the incremental pulse modulation was performed with linearly increasing drain voltage (with 150 consecutive positive and negative pulses changed from 1.8 to 2 V and from −1.9 to −2.1 V, respectively) for set and reset processes, respectively. All pulse modulation measurements were processed under a gate bias ranging from 2 to 10 V and at a fixed read voltage of 0.2 V.

Defect Detection Algorithm: This algorithm was used to detect defects used in this work.

Algorithm. Defect identification process using dynamic Gaussian blur kernels, morphological image process, and averaging schema.
Initialize image and convert to grayscale.
Initiate array of sigma values.
  Calculate the discretized Gaussian blur kernels using 64 states using the sigma values.
Initialize structuring elements SE_1 and SE_2 for the morphological process

$$(SE)_Z := \{x | x = i + z, \forall i \in SE\}$$

$$(\widehat{SE})_z := \{x | x = -i, \forall i \in SE\}$$

$$\text{Erosion} := A \ominus SE = \{z | (SE)_z \cap A^c = \varnothing\}$$

$$\text{Dilation} := A \oplus SE = \{z | [(\widehat{SE})_z \cap A] \subseteq A\}$$

For each kernel
  Initialize threshold level, t_h, using Otsu's method or manually.
  Convert grayscale image into a binary image using thresholding.
    binarized = image $> t_h$
  opened = mathematical morphological opening on binarized image with SE_1

$$A \bullet SE_1 = (A \ominus SE_1) \oplus SE_1$$

  closed = mathematical morphological closing on opened image with SE_2

$$A \circ SE_2 = (A \oplus SE_2) \ominus SE_2$$

  end
Calculate average via the element-wise method.
Set $I_{\text{average}} = \sum_{i=1}^{n} I_i$.
Divide I_{average} by the number of morphological output images.
end

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

H.S.L., Y.B., and Q.L. contributed equally to this work. This work was supported by the Virginia Micro-Electronics Consortium (VMEC) (Grant No. 406010-1) and the National Science Foundation (NSF) Career Award (Award No. 1825256).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

artificial intelligence, defect identification, image processing, memristors, oxide thin-film transistors

Received: August 27, 2020
Revised: September 23, 2020
Published online:

[1] C. Y. Chang, C. H. Li, J. W. Chang, M. Der Jeng, *Expert Syst. Appl.* **2009**, *36*, 950.
[2] C. J. Huang, C. C. Wang, C. F. Wu, *IEEE Des. Test Comput.* **2002**, *19*, 44.
[3] Y. H. Liu, S. H. Lin, Y. L. Hsueh, M. J. Lee, *Expert Syst. Appl.* **2009**, *36*, 1978.
[4] S. H. Indera Putera, Z. Ibrahim, in *ICETC 2010–2010 2nd Int. Conf. Education Technology and Computer*, IEEE, Vol. *5*, **2010**, p. 359.
[5] P. Vogt, K. H. Riitters, C. Estreguil, J. Kozak, T. G. Wade, J. D. Wickham, *Landsc. Ecol.* **2007**, *22*, 171.
[6] S. Saritha, N. Amutha Prabha, *Int. J. Imaging Syst. Technol.* **2016**, *26*, 295.
[7] S. Cha, *Am. J. Neuroradiol.* **2006**, *27*, 475.
[8] M. H. Karimi, D. Asemani, *ISA Trans.* **2014**, *53*, 834.
[9] S. Chabrier, B. Emile, H. Laurent, C. Rosenberger, P. Marché, *Proc. Int. Conf. Pattern Recognit.* **2004**, *1*, 576.
[10] N. Bouaynaya, D. Schonfeld, *J. Vis. Commun. Image Process.* **2006**, *6077*, 60771Y.
[11] J. Von Neumann, M. D. Godfrey, *IEEE Ann. Hist. Comput.* **1993**, *15*, 27.
[12] G. W. Burr, R. M. Shelby, A. Sebastian, S. Kim, S. Kim, S. Sidler, K. Virwani, M. Ishii, P. Narayanan, A. Fumarola, L. L. Sanches, I. Boybat, M. Le Gallo, K. Moon, J. Woo, H. Hwang, Y. Leblebici, *Adv. Phys. X* **2017**, *2*, 89.
[13] Q. Xia, J. J. Yang, *Nat. Mater.* **2019**, *18*, 309.
[14] C. Li, M. Hu, Y. Li, H. Jiang, N. Ge, E. Montgomery, J. Zhang, W. Song, N. Dávila, C. E. Graves, Z. Li, J. P. Strachan, P. Lin, Z. Wang, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, Q. Xia, *Nat. Electron.* **2018**, *1*, 52.
[15] J. J. Yang, D. B. Strukov, D. R. Stewart, *Nat. Nanotechnol.* **2013**, *8*, 13.
[16] M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, J. J. Yang, Q. Xia, J. P. Strachan, *Adv. Mater.* **2018**, *30*, 1705914.
[17] M. Prezioso, F. Merrikh-Bayat, B. D. Hoskins, G. C. Adam, K. K. Likharev, D. B. Strukov, *Nature* **2015**, *521*, 61.
[18] Z. Wang, C. Li, W. Song, M. Rao, D. Belkin, Y. Li, P. Yan, H. Jiang, P. Lin, M. Hu, J. P. Strachan, N. Ge, M. Barnell, Q. Wu, A. G. Barto, Q. Qiu, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Electron.* **2019**, *2*, 115.
[19] M. A. Zidan, H. A. H. Fahmy, M. M. Hussain, K. N. Salama, *Microelectron. J.* **2013**, *44*, 176.
[20] C. Li, D. Belkin, Y. Li, P. Yan, M. Hu, N. Ge, H. Jiang, E. Montgomery, P. Lin, Z. Wang, W. Song, J. P. Strachan, M. Barnell, Q. Wu, R. S. Williams, J. J. Yang, Q. Xia, *Nat. Commun.* **2018**, *9*, 7.
[21] P. Yao, H. Wu, B. Gao, S. B. Eryilmaz, X. Huang, W. Zhang, Q. Zhang, N. Deng, L. Shi, H. S. P. Wong, H. Qian, *Nat. Commun.* **2017**, *8*, 15199.
[22] M. Zangeneh, A. Joshi, *IEEE Trans. Very Large Scale Integr. Syst.* **2014**, *22*, 1815.
[23] N. Ghenzi, M. Rozenberg, L. Pietrobon, R. Llopis, R. Gay, M. Beltrán, M. Knez, L. Hueso, P. Stoliar, *Appl. Phys. Lett.* **2018**, *113*, 072108.
[24] L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos, G. Tröster, *Appl. Phys. Rev.* **2016**, *3*, 021303.
[25] S. Kim, H. Y. Jeong, S. K. Kim, S. Y. Choi, K. J. Lee, *Nano Lett.* **2011**, *11*, 5438.
[26] K. Myny, *Nat. Electron.* **2018**, *1*, 30.
[27] D. C. Paine, B. Yaglioglu, Z. Beiley, S. Lee, *Thin Solid Films* **2008**, *516*, 5894.
[28] B. Yaglioglu, H. Y. Yeom, R. Beresford, D. C. Paine, *Appl. Phys. Lett.* **2006**, *89*, 062103.
[29] Y. Song, R. Xu, J. He, S. Siontas, A. Zaslavsky, D. C. Paine, *IEEE Electron Device Lett.* **2014**, *35*, 1251.
[30] J. C. Park, H. N. Lee, S. Im, *ACS Appl. Mater. Interfaces* **2013**, *5*, 6990.
[31] S. Pi, C. Li, H. Jiang, W. Xia, H. Xin, J. J. Yang, Q. Xia, *Nat. Nanotechnol.* **2019**, *14*, 35.
[32] H. Jiang, L. Han, P. Lin, Z. Wang, M. H. Jang, Q. Wu, M. Barnell, J. J. Yang, H. L. Xin, Q. Xia, *Sci. Rep.* **2016**, *6*, 28525.
[33] H. Elbehiery, A. Hefnawy, M. Elewa, in *Proc. – WEC'05 3rd World Enformatika Conf.*, Istanbul, Turkey, Vol. *5*, **2005**, p. 158.
[34] K. L. Mak, P. Peng, K. F. C. Yiu, *Image Vis. Comput.* **2009**, *27*, 1585.
[35] R. A. Haddad, A. N. Akansu, *IEEE Trans. Signal Process.* **1991**, *39*, 723.
[36] R. Maini, H. Aggarwal, *Int. J. Image Process.* **2009**, *3*, 1.
[37] J. M. Haggerty, X. N. Wang, A. Dickinson, C. J. O'Malley, E. B. Martin, *BMC Med. Imaging* **2014**, *14*, 7.
[38] L. Gao, P. Y. Chen, S. Yu, *IEEE Electron Device Lett.* **2016**, *37*, 870.
[39] C. Merkel, R. Hasan, N. Soures, D. Kudithipudi, T. Taha, S. Agarwal, M. Marinella, *Computer* **2016**, *49*, 56.
[40] C. Summers, M. J. Dinneen, in *Proc. – 2019 IEEE Winter Conf. Applications of Computer Vision, WACV 2019*, IEEE **2019**, p. 1262.
[41] P. Y. Liao, T. C. Chang, Y. J. Chen, W. C. Su, B. W. Chen, L. H. Chen, T. Y. Hsieh, C. Y. Yang, K. C. Chang, S. D. Zhang, Y. Y. Huang, H. M. Chang, S. C. Chiang, *Appl. Phys. Lett.* **2017**, *110*, 263505.
[42] W. C. Su, T. C. Chang, P. Y. Liao, Y. J. Chen, B. W. Chen, T. Y. Hsieh, C. I. Yang, Y. Y. Huang, H. M. Chang, S. C. Chiang, K. C. Chang, T. M. Tsai, *Appl. Phys. Lett.* **2017**, *110*, 103502.
[43] C. C. Chang, P. T. Liu, C. Y. Chien, Y. S. Fan, *Appl. Phys. Lett.* **2018**, *112*, 172101.
[44] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G. L. Li, H. L. Xin, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Mater.* **2017**, *16*, 101.
[45] B. Mohammad, M. A. Jaoude, V. Kumar, D. M. Al Homouz, H. A. Nahla, M. Al-Qutayri, N. Christoforou, *Nanotechnol. Rev.* **2016**, *5*, 311.
[46] J. F. Conley, *IEEE Trans. Device Mater. Reliab.* **2010**, *10*, 460.
[47] J. K. Jeong, *Semicond. Sci. Technol.* **2011**, *26*, 034008.
[48] H. Liu, M. Wei, Y. Chen, *Nanotechnol. Rev.* **2018**, *7*, 443.
[49] S. Yu, *Proc. IEEE* **2018**, *106*, 260.

[50] G. Indiveri, B. Linares-Barranco, R. Legenstein, G. Deligeorgis, T. Prodromakis, *Nanotechnology* **2013**, *24*, 384010.
[51] H. M. Shaw, D. S. Rigel, R. J. Friedman, W. H. Mccarthy, A. W. Kopf, *JAMA* **2020**, *292*, 2771.
[52] S. S. Jo, Massachusetts Institute of Technology (MIT), February **2018**.
[53] A. Rydosz, W. Maziarz, A. Brudnik, A. Czapla, K. Zakrzewska, in *2018 XV Int. Scientific Conf. Optoelectronic and Electronic Sensors 2018*, IEEE **2016**.