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Letter

Three-terminal magnetic tunnel junction synapse circuits showing spike-timing-dependent plasticity

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Abstract

There have been recent efforts towards the development of biologically-inspired neuromorphic devices and architecture. Here, we show a synapse circuit that is designed to perform spike-timing-dependent plasticity which works with the leaky, integrate, and fire neuron in a neuromorphic computing architecture. The circuit consists of a three-terminal magnetic tunnel junction with a mobile domain wall between two low-pass filters and has been modeled in SPICE. The results show that the current flowing through the synapse is highly correlated to the timing delay between the pre-synaptic and post-synaptic neurons. Using micromagnetic simulations, we show that introducing notches along the length of the domain wall track pins the domain wall at each successive notch to properly respond to the timing between the input and output current pulses of the circuit, producing a multi-state resistance representing synaptic weights. We show in SPICE that a notch-free ideal magnetic device also shows spike-timing dependent plasticity in response to the circuit current. This work is key progress towards making more bio-realistic artificial synapses with multiple weights, which can be trained online with a promise of CMOS compatibility and energy efficiency.

Keywords: synapse, neuromorphic, magnetic tunnel junction, plasticity, domain wall

(Some figures may appear in colour only in the online journal)

1. Introduction

Dedicated architecture for artificial intelligence (AI) applications can overcome the limitations of the von Neumann architecture in accomplishing data-intensive tasks. Transistors are traditionally used as binary logic devices, whereas applications like perception, prediction, and decision making are inherently non-binary tasks. The von Neumann architecture also faces a memory access bottleneck, as separation between the memory unit and the computing unit necessitates the frequent transfer of data between these two units, which results in significant delay and energy consumption [1, 2]. Due to these reasons, there has been a paradigm shift towards biologically-inspired neuromorphic computing which requires developing devices and circuits that approximate physical components of the nervous system, e.g. the neuron and synapse, and embody

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dynamical operations such as learning and real-time adaptation (plasticity) [3].

Neurons are cells within the nervous system that receive signals from other neurons through their dendrites, perform non-linear processing on the signals in their soma, and transmit the output to the next set of neurons through their axon [4]. A synapse is a structure in the nervous system that allows a neuron to pass an electrical signal (electrical current) or a chemical signal (neurotransmitters) to another neuron or to a target effector cell [5]. Synaptic plasticity is believed to be a major contributor to memory and learning. In response to increases or decreases in specific patterns of a synapse's activity, the synapse strengthens or weakens over time. While plasticity is an ongoing topic of research in neuroscience, well-established hallmarks of plasticity operations include changes in the quantity of neurotransmitters, changes in the strength and number of receptors on the post-synaptic neuron, and changes in how rapidly the post-synaptic neuron responds to stimulation from the pre-synaptic neuron.

Spike-timing-dependent plasticity (STDP) has been identified as a key operation for learning and memory in the brain, as well as the basis for development and refinement of neural circuits during brain development. It is a biological process in which the strength of the synapse (synaptic weight) is correlated with the time differences between pre-synaptic neural signals and post-synaptic neural signals [6, 7]. This is commonly refered to as 'cells that fire together, wire together', [8] in which the synaptic connection between the neurons gets reinforced in the form of long-term potentiation (LTP) or weakened in the form of long-term depression (LTD).

Numerous types of emerging non-volatile memory devices are being studied as artifical neurons for low-power computing elements and synapses as adaptive memory elements [9]. So far, most research in this area has focused on technologies such as resistive random access memory (RRAM) [10, 11], phase change memory [9, 12], and conductive-bridge RAM (CBRAM) [13]. For example, complex plasticity effects have been physically demonstrated in CBRAM devices [14, 15] and used for nanodevice-powered learning architectures [16, 17]. Recently, there has been significant interest in fully implementing plasticity operations in magnetic random access memory (MRAM) systems based on magnetic tunnel junction (MTJ) devices. Magnetic devices have many properties similar to the neurons and synapses of the brain, such as low-energy [18] and stochastic switching [19], nonvolatility, and co-localized memory and logic [20]. Additionally, magnetic devices have been proposed to act as both synapses and neurons [21–24], providing a potential platform for monolithic neuromorphic circuits. MRAM cycle-to-cycle endurance is the highest among emerging resistive memories with over 10^{15} cycles [25]; it is a particularly attractive device for building synapses, because the devices can handle the high activity factor necessary for online learning.

The three-terminal magnetic tunnel junction (3T-MTJ), shown in figure 1(a), is an MTJ device where the ferromagnetic free layer is separated from the ferromagnetic pinned layer by a tunneling oxide barrier and there are three terminals: two terminals on either side of the free layer (*IN* and *CLK*) and one terminal connecting to the top pinned layer (*OUT*). The free layer can be set up to have two oppositely magnetized regions separated by a domain wall (DW), as shown. In the synapse implementation, the pinned layer is kept long enough in $\hat{x}$ such that the the free layer magnetization can be manipulated via the DW to orient either fully parallel, antiparallel, or inbetween, relative to the magnetization of the pinned layer, which will result in multiple conductances through the center tunnel junction that can represent synaptic weights. The extra third terminal is to provide separate read/write control channels and separate control of the DW, compared to the two-terminal MTJs (2T-MTJs) in MRAM where the same channel is used as both read and write [26, 27]. Since MTJ breakdown most often happens at the tunnel barrier, separating the read and write can extend the device endurance even further for synapse applications, because during training minimal current flows through the tunnel barrier. The DW of the free layer can be displaced by spin transfer torque (STT) exerted on it by spin polarized current flowing through the free layer [28] or

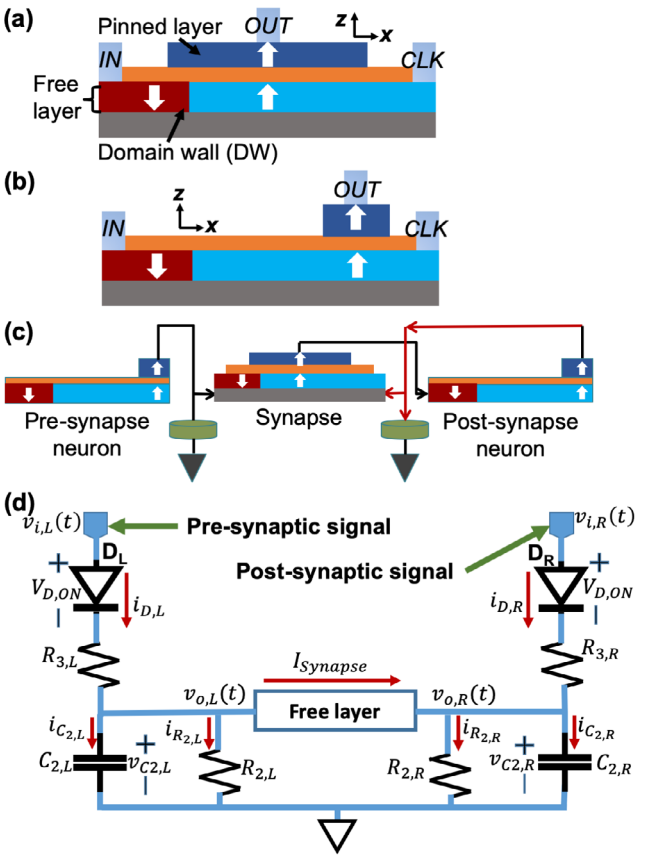

Figure 1. (a) Side-view cartoon of the 3T-MTJ synapse device. The up/down arrows and blue/red color represent the magnetization vector of the ferromagnetic thin films; the orange represents the tunnel barrier. (b) Side-view cartoon of the corresponding 3T-MTJ neuron device we developed in [24]. (c) Cartoon showing the 3T-MTJ synapse integrated with the pre-synaptic neuron and post-synaptic neuron. The capacitors (green discs) are integral in timing coordination in order to move the DW. (d) The balanced synapse circuit schematic with the MTJ free layer modeled as a resistor. $I_{Synapse}$ is the current that flows through the free layer of the MTJ and moves the DW, thereby adjusting the device weight in the form of tunneling resistance.

by spin orbit torque (SOT) exerted by a charge current flowing through an underlying heavy metal (HM) [29–31].

The majority of the work on spintronic neuromorphic computing has focused on the implementation of neurons using 2T-MTJs [19, 22, 23, 32–34] while doing most of the synaptic weight training offline. Others have attempted to use 2T-MTJs as synapses which are limited to binary weights [35]. Some work has been done on using 3T-MTJs as neurons [26], including our recent work developing a leaky, integrate, and fire (LIF) neuron with inherent lateral inhibition [24, 36]. The 3T-MTJ LIF neuron, to contrast from the synapse, is shown in figure 1(b). A shorter (in $\hat{x}$) pinned layer that is offset from the center of the free layer enables the DW motion to represent integration, and firing occurs once the DW passes the pinned layer.

Only a few efforts have used 3T-MTJs as synapses. One example is the use of a transistor circuit and a 3T-MTJ to show stochastic STDP in a binary synapse [37]. This, however, does not show a multi-state resistance or conductance weighting system that is similar to the biological synapse [38–40]. Another example is an all-spin neural network in which binary 3T-MTJ neurons are connected to binary 3T-MTJ synapses through transistor axons [26]. Although this still uses binary synapses and does not show LTP or LTD, it sought to use less CMOS-based devices, which can be beneficial for energy efficiency. However, that implementation does not allow for fine adjustments of the synaptic weights, which may be critical to implementing plasticity-based learning algorithms.

Here, we have designed and modeled a synapse circuit using 3T-MTJs that captures STDP and allows online learning. We show that there is a correlation between the current amplitude to switch the DW and the timing between the pre-synaptic signal and the post-synaptic signal, and that the response of the circuit mimics the biological neural model of potentiation and inhibition. We also show that lithographically-defined notches along the length of the DW track create controlled pinning of the DW location. This well-studied method for DW control [41–44] shows a semi-analog multiple weight state depending on the pre- and post-synaptic signals.

We first present the 3T-MTJ circuit that has been developed for STDP and provide details about its functionality. Then, we show results from the SPICE simulation of the circuit, followed by micromagnetic simulation results for current pulse timing from the circuit applied to a 3T-MTJ to achieve multiple weight states. Finally, we use a SPICE model of the 3T-MTJ that we have benchmarked against micromagnetics [45] to study the behavior of the full circuit including the current waveform and DW dynamics.

2. Methods

The model for the artificial synapse is shown in figure 1. To have the 3T-MTJ synapse, figure 1(a), show STDP behavior, we need the position of the DW, and therefore the resistance weight, to respond to the timing between spiking signals at both the *IN* and *CLK* terminals. What the DW position *does* respond to is the sign of the current $I_{Synapse}$ between the *IN* and *CLK* terminals, which if above the DW depinning current will move the DW right or left. Thus, to achieve STDP we design a circuit that converts the timing of the pre- and post- synaptic signals to a sign and magnitude change in $I_{Synapse}$. We keep the circuit small and as simple as possible so that it could be integrated into a dense array of the 3T-MTJ synapses with a small area overhead.

Figure 1(c) depicts the circuit, consisting of a 3T-MTJ sandwiched between two capacitor–resistor–diode networks (green disks) through which it is connected to the pre- and post-synaptic 3T-MTJ neurons. The pre-synaptic signal comes from the output of the pre-synaptic neuron; the post-synaptic signal comes from the output of the post-synaptic neuron; and the output of the synapse goes into the input of the post-synaptic neuron. Here, we focus on the synapse behavior; the details of how the neurons and synapses connect are not specified.

The details of the circuit are shown in figure 1(d). It includes minimal additional resistors and capacitors to enable STDP that could be integrated into a crossbar array. We have modeled the free layer in case of an STT device (or HM in case of an SOT device) as a patterned thin film resistance $R_{Synapse}$ in the balanced RC circuit. The center MTJ resistance of the device is not included. Diodes are placed on both ends of the circuit to prevent back current flow. The capacitor to the left of the 3T-MTJ $(C_{2,L})$ and the capacitor to the right $(C_{2,R})$ have equal capacitances. The left resistor $(R_{2,L})$ and right resistor $(R_{2,R})$ are equal resistances. $(R_{3,L})$ and $(R_{3,R})$ are the sum of a resistor and the contact resistance to the left and the right of the 3T-MTJ, respectively. The dynamics of the circuit depend on the arrival times of the pre-synaptic neuron signal (voltage amplitude $v_{i,\,L}(t)$) and the post-synaptic neuron signal (voltage amplitude $v_{i,R}(t)$), the states of the the diodes D_{L} and D_{R}, and the time constants of the RC networks $R_{2,L}C_{2,L}$ and $R_{2,R}C_{2,R}$. These states affect the direction of flow of $I_{Synapse}$ which will increase or decrease the conductance of the MTJ through STT or SOT switching of a DW in the free layer. The current i is labeled throughout the circuit.

For either of the diodes to be on, the input signals from the pre-synaptic or post-synaptic neurons must be such that

$$v_{i,R}\,(t) - v_{o,R} - i_{D,R}R_{3,R} \geqslant V_{D,ON} \tag{1}$$

$$v_{i,L}\,(t) - v_{o,L} - i_{D,L}R_{3,L} \geqslant V_{D,ON}. \tag{2}$$

When both diodes D_{L} and D_{R} turn on at the same time, the pre-synaptic and post-synaptic signals arrive at the same time, and assuming the voltages at the capacitors $C_{2,L}$ and $C_{2,R}$ are at the same value, no current flows through the free layer, i.e.

$$I_{Synapse} = 0;\; i_{D,L} = i_{D,R} \geqslant 0,\; v_{i,L}\,(t) = v_{i,R}\,(t)\,. \tag{3}$$

For other conditions (when both diodes are on), the complete set of parametric equations for the circuit can be written from nodal analysis as

$$v_{i,L}\,(t) - v_{o,L} - i_{D,L}R_{3,L} = V_{D,ON} \tag{4}$$

$$v_{i,R}\,(t) - v_{o,R} - i_{D,R}R_{3,R} = V_{D,ON} \tag{5}$$

$$i_{D,L} = i_{C_{2,L}} + \frac{v_{o,L} - v_{o,R}}{R_{synapse}} + \frac{v_{o,L}}{R_{2,L}} \tag{6}$$

$$i_{D,R} = i_{C_{2,R}} - \frac{v_{o,L} - v_{o,R}}{R_{synapse}} + \frac{v_{o,R}}{R_{2,R}} \tag{7}$$

$$i_{C_{2,L}} = C_{2,L}\frac{dv_{o,L}}{dt} \tag{8}$$

$$i_{C_{2,R}} = C_{2,R}\frac{dv_{o,R}}{dt}. \tag{9}$$

Using Laplace transforms, we write the input voltages as

$$v_{i,L}(s) = V_{iL} * \left(\frac{1 - \exp(-s * t_{pw})}{s * (1 - \exp(-t_p * s))}\right) \tag{10}$$

$$v_{i,R}(s) = V_{iR} * \left(\frac{\exp(-s * t_d) - \exp(-s * (t_d + t_{pw}))}{s * (1 - \exp(-t_p * s))}\right) \tag{11}$$

where s is the Laplace frequency variable, V_{iL} and V_{iR} are the pre- and post-synaptic signal amplitudes, respectively, t_{pw} is the pulse width, t_d is the delay between the pre-synaptic signal and the post-synaptic signal, and t_p is the period of both the pre-synaptic and post-synaptic signals. The current through the MTJ synapse can then be derived as:

$$I_{Synapse} = \frac{v_{o,L} - v_{o,R}}{R_{synapse}}. \tag{12}$$

When both diodes D_L and D_R are off and assuming they turn off after a cycle of the circuit at about the same time at $t > 0$, the current flowing through the free layer will be a function of the difference of the voltages of $C_{2,L}$ and $C_{2,R}$. And given that $C_{2,L} = C_{2,R} = C_2$ and $R_{2,L} = R_{2,R} = R_2$, $I_{Synapse}$ can be written as:

$$I_{Synapse} = \exp\left(-\frac{t * (2 * R_2 + R_{synapse})}{C_2 * R_2 * R_{synapse}}\right) * (v_{C2,L}(t) - v_{C2,R}(t)) \tag{13}$$

where $v_{C2,L}(t)$ and $v_{C2,R}(t)$ are the voltages of capacitors $C_{2,L}$ and $C_{2,R}$, respectively, at time $t > 0$ when both diodes are off.

3. Results and discussion

3.1. Circuit simulation results

The 3T-MTJ synapse circuit is simulated in HSpice with varying delay conditions from 0.1 ns to 5 ns between onset of the pre-synaptic neuron signal $v_{i,L}(t)$ and post-synaptic neuron signal $v_{i,R}(t)$. The signal pulse widths are 1 ns with a 10 ns period, and we use $R_{2,L} = R_{2,R} = R_2 = 10$ kΩ, $R_{Synapse}$ (resistance of the free layer) = 100 Ω, $R_{3,L} = R_{3,R} = R_3 = 50$ Ω, and $C_{2,L} = C_{2,R} = C_2 = 1 \times 10^{-12}$ F. Figure 2 shows the results of the HSpice simulation, where we plot both the transient voltage pulses and current through the free layer, $I_{Synapse}$. It can be seen from figures 2(a) and (b) that when $v_{i,L}(t)$ arrives before $v_{i,R}(t)$, a positive current flows through the 3T-MTJ synapse, which will increase the conductance of the MTJ stack. The dynamics of the circuit depend on which signal arrives first. The circuit acts as a two-port peak detector, with RC networks on both sides of the free layer. If $v_{i,L}(t)$ arrives before $v_{i,R}(t)$, then the voltage $v_{C_{2,R}}$ of the capacitor $C_{2,R}$ on the post-synaptic end, which has been stored up from the previous period, is almost fully discharged. This results in a larger voltage difference across the free layer and higher current amplitude. Conversely, if within the same period there is a greater delay between the two signals, the capacitor on the post-synaptic side will still be holding some voltage stored from the previous period, resulting in a reduced voltage difference and less current. Hence, the magnitude of the current is inversely proportional to the delay between $v_{i,L}(t)$ and $v_{i,R}(t)$.

Figures 2(d) and (e) show that if the post-synaptic neuron fires before the pre-synaptic neuron, there is a negative (depressing) current through the synapse, and its magnitude is also dependent on the delay between the signals. Then there are the cases shown in figures 2(c) and (f) in which the pre-synaptic neuron fires midway between the span of the post-synaptic neuron firing twice in the first case; and the post-synaptic neuron fires midway between the span of the pre-synaptic neuron firing twice in the second case. In both cases there are equal magnitudes of both positive and negative current spikes flowing through the synapse. This can lead to oscillation of the output MTJ resistance. It should be noted that in all the simulations there is an initial larger current spike, which is an artifact of the circuit starting at time $t = 0$.

To compare with the behavior of biological synapses, the current that passes through a chemical synaptic channel, $I_{syn,bio}(t)$, can be represented by [4, 46]

$$I_{syn,bio}(t) = g_{syn}(t)(u(t) - E_{syn}) \tag{14}$$

which depends on the difference between its reversal potential E_{syn} and the actual value of the membrane potential, $u(t)$. $g_{syn}(t)$ is a superpostion of synaptic conductances $\bar{g}_{syn}$ with exponential decay of time constant τ and given by

$$g_{syn}(t) = \sum_f \bar{g}_{syn} e^{-\frac{t-t^f}{\tau}} \Theta(t - t^f) \tag{15}$$

where t^f is the arrival time of a pre-synaptic action potential and $\Theta(t - t^f)$ is a Heaviside step function. $g_{syn}(t)$ can be simplified for a single neuron-to-neuron synaptic connection by the alpha-function [46]

$$g_{syn}(t) = \frac{t}{\tau_s} e^{-\frac{t}{\tau_s}} \tag{16}$$

where τ_s is the time constant of the response which specifies slow or fast transmission.

In figure 3(a), we plot $I_{Synapse}(t)$ from the HSpice simulation for the figure 2(a) condition ('SPICE'), compared to the analytical solution equation (12), using parameters from equations (4)–(11) ('Analytical'), with $t_{pw} = 1$ ns, $t_d = 0.2$ ns, $t_p = 10$ ns, $R_2 = 10$ kΩ, $R_{Synapse} = 100$ Ω, $R_3 = 50$ Ω, and $C_2 = 1 \times 10^{-12}$ F. We also compare to the biological synapse transient current behavior using $\tau_s = 0.1$ ns ('Biological'). The plots are normalized to their maximum values. It can be seen that we closely capture the biological transient behavior with the circuit, which agrees well with simulations, mathematical modeling, and analysis of biological neurons [46–54].

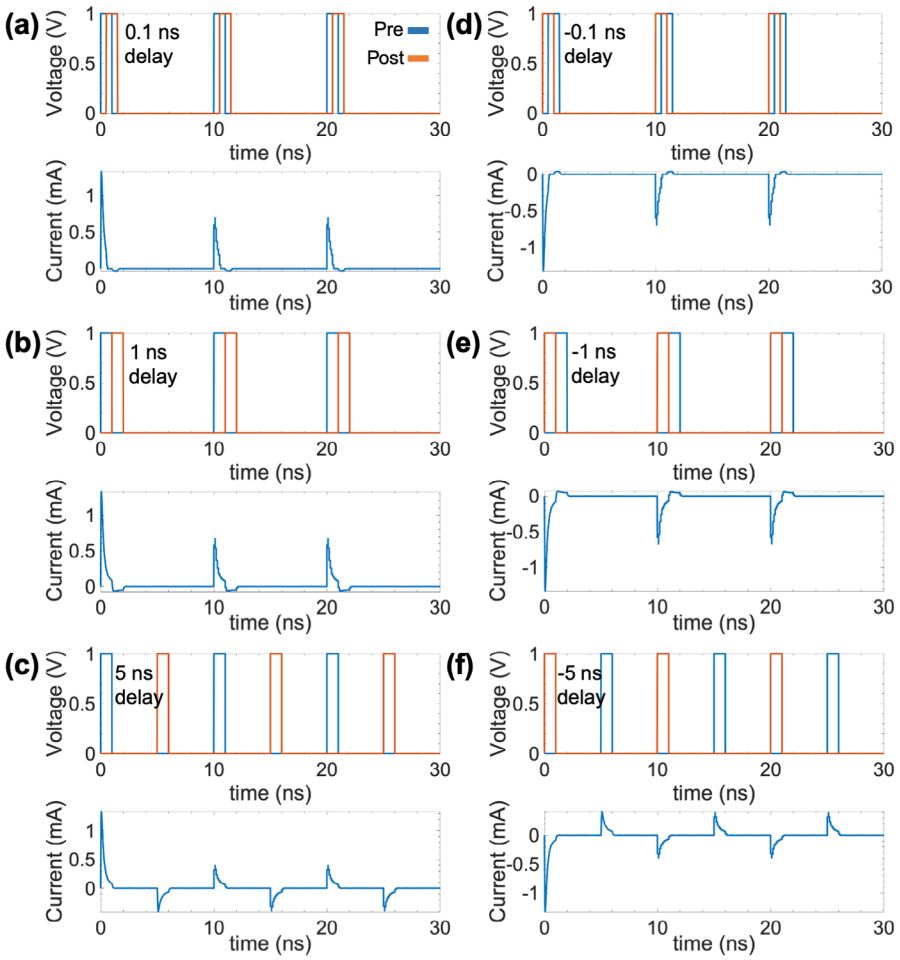

Figure 2. Spice simulation results for different delay scenarios between the pre-synaptic neuron signal and post-synaptic neuron signal. (a)–(c) The currents (lower plots) that flow through the free layer when the pre-synaptic neuron fires 0.5 ns, 1 ns, and 5 ns, respectively, before the post-synaptic neuron fires. (d)–(f) The currents (lower plots) that flow through the free layer when the pre-synaptic neuron fires 0.5 ns, 1 ns, and 5 ns, respectively, after the post-synaptic neuron fires. Both the pre- and post-synaptic firing are represented by voltage pulses of 10 ns period and 10% duty cycle as shown in the upper plots.

It can also be seen that the RC networks on both sides of the free layer also act as a low pass filter modeled in glutamate channels with N-methyl-D-aspartate receptors [4].

Figure 3(b) shows the $I_{Synapse}\,(t)$ dependence on $R_{Synapse}$. As the resistance increases, the current decreases exponentially. This provides a design requirement for the 3T-MTJ device to keep the resistance of the bottom layers under 1–2 kΩ to have enough current to drive a DW in the free layer. This resistance value is a reasonable requirement for 3T-MTJ devices (e.g. in [20] $R_{\mathrm{Synapse}} = 1.2$ kΩ), and it can be tuned by choosing the material and geometry of the bottom layers. The resistance needed depends on the required current for depinning the DW for a given device size and materials.

To calculate how much the circuit can tolerate imperfections between the matched capacitors, in figure 3(c) we plot $I_{Synapse}$ while increasing the difference between the capacitance of C_{2L} and C_{2R} up to a factor of three mismatch. The figure shows the circuit is more tolerant of $C_{2R} > C_{2L}$ with a $3\times$ mismatch producing a 25% change in $I_{Synapse}$. For $C_{2R} < C_{2L}$, the $3\times$ mismatch reduces the synapse current by a larger factor up to 64%. This analysis assumes the pre-synaptic signal $v_{i,L}$ leads the post-synaptic signal $v_{i,R}$ by 0.1 ns. It is expected that the graph will be similar but flipped along the y-axis if the pre-synaptic signal lags the post-synaptic signal by the same amount of time (0.1 ns).

To investigate how the response time of the current through the 3T-MTJ free layer to the pre- and post-synaptic signals varies with the capacitance mismatch on either side of the MTJ, we took the the onset time for signal $I_{Synapse}$ on the second period, using a period of 10 ns and plotted it against the capacitance mismatch. The second period was used rather than the first period because of the artifact that comes with starting the simulation at $t = 0$. Figure 3(d) shows the timing of the current through the synapse is tolerant to capacitance mismatches with little or no difference in the current timing as the capacitance mismatch gets larger. The current pulse comes quicker on the average if C_{2R} is increased with respect to C_{2L} and saturates as the difference approaches -2 pF. The reason for the small 0.3% dip in timing shown in figure 3(d) is not yet fully understood.

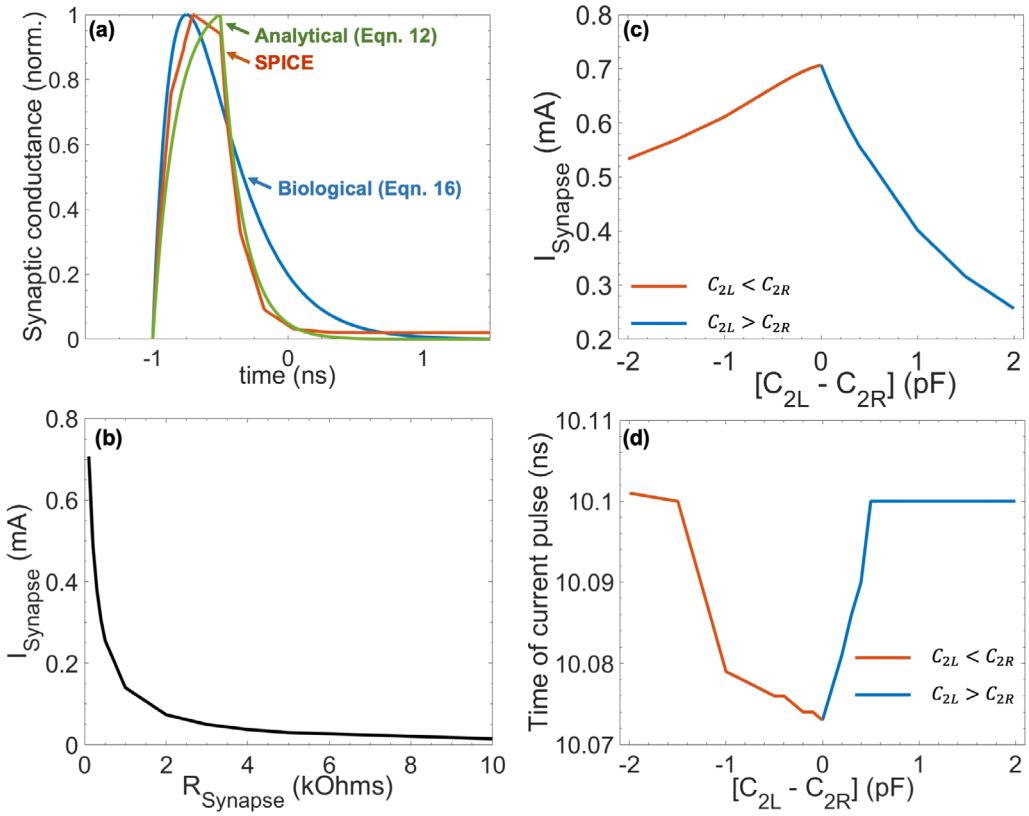

Figure 3. (a) Comparison of the transient synaptic current from the SPICE circuit to the analytical expression of the circuit from equation (12) and the biological synapse alpha-function from equation (16). The plots have been normalized to their maximum values. (b) Plot of current at the synapse versus resistance of the 3T-MTJ free layer. (c) Plot of current at the synapse and (d) current pulse timing versus difference in capacitance of the two capacitors in the circuit; orange traces correspond to $C_{2L} < C_{2R}$ and blue traces correspond to $C_{2L} > C_{2R}$.

3.2. Spike-timing-dependent plasticity (STDP)

Taking the different current magnitudes flowing through the synapse at different timing conditions, we graph the current magnitude against time delay between the pre-synaptic neuron signal and the post-synaptic neuron signal. The plot is shown in figure 4. It is seen that the smaller the delay, the higher the current magnitude that flows through the synapse. Thus, the circuit captures both potentiation and depression, and also captures that the amplitude of the strengthening or weakening of the synapse is based on the timing between the pre- and post- signals. This has a high resemblance to the work of Bi and Poo's clinical experiment on STDP which shows LTP and LTD induced in synapses between hippocampal glutamatergic neurons [55]. Additionally, when the circuit has no correlation between the two signals, we get oscillation in time back and forth between two resistance states, maintaining the state of the synapse conductance.

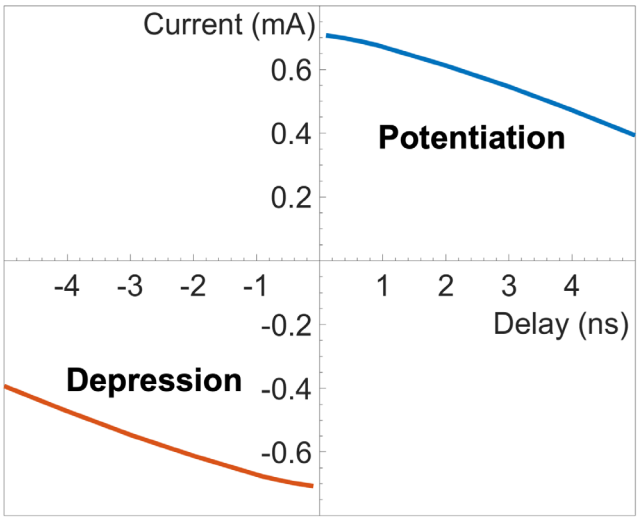

Figure 4. Potentiation and depression currents from the SPICE simulation as a function of spiking delay between pre-synaptic and post-synaptic neurons.

3.3. Micromagnetic simulations

To observe how the circuit will affect the magnetic behavior of the 3T-MTJ synapse, we run the HSpice model and input the *vector direction* of the resulting $I_{Synapse}$ into a micromagnetic simulation using MuMax3 [56] and rendered in OOMMF [57]. While 3T-MTJs have been modeled as a synapse in perfect wires [19, 26, 35, 58–61], it is a challenge in a real device to repeatably control the distance of the DW along the free layer racetrack under the MTJ. One solution, implemented here, is to use lithographically defined notches, which are anisotropy barriers that pin the DW. We model a 1 μm long $\times$ 32 nm wide $\times$ 4 nm thick CoFeB free layer with a discretization cell size of 1 nm $\times$ 1 nm $\times$ 1 nm, perpendicular

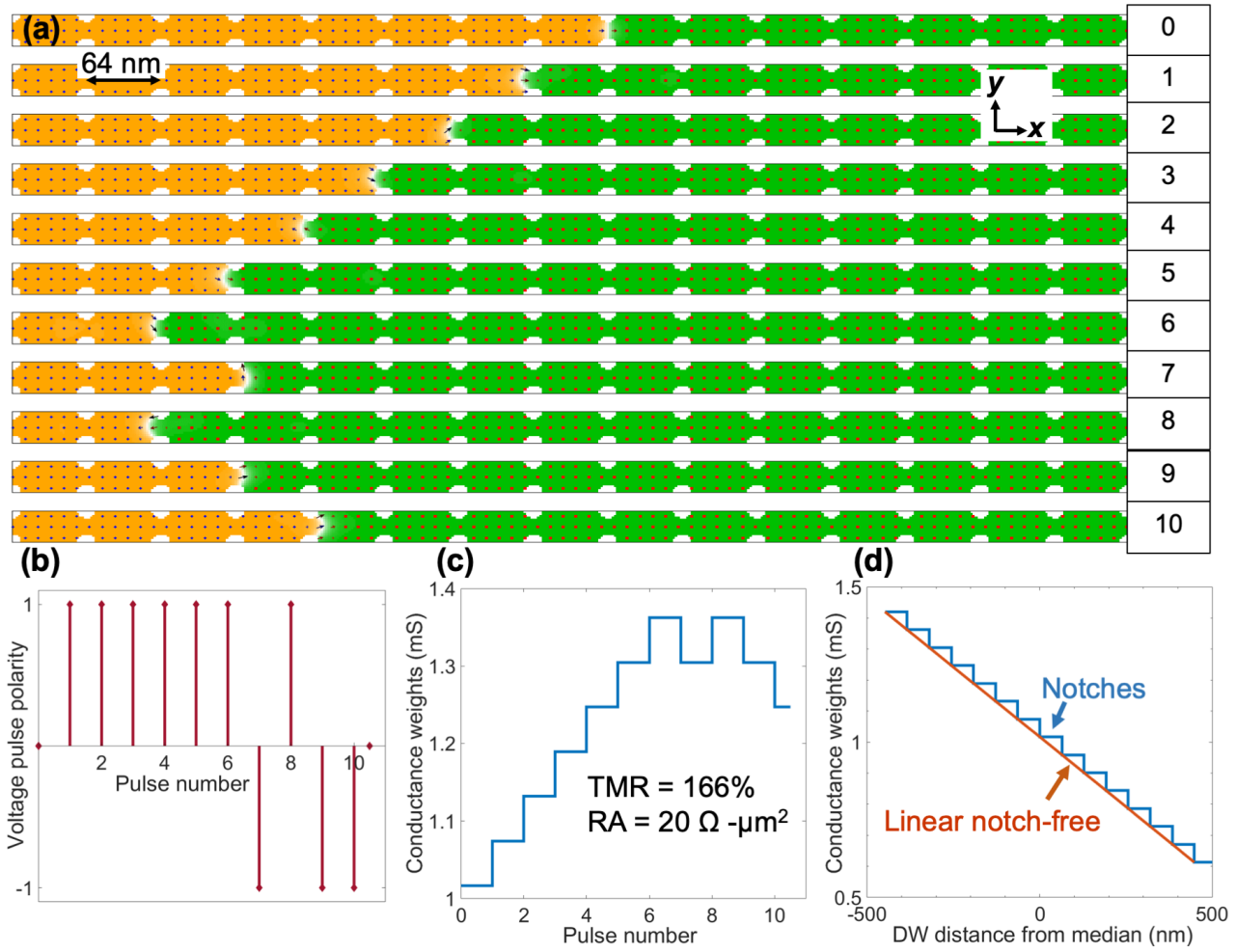

Figure 5. (a) Micromagnetic simulation snapshots for the current pulse train shown in (b) through a 1 μm long $\times$ 32 nm wide $\times$ 4 nm thick CoFeB free layer. The notches introduce anisotropies which pin the DW. (c) Plot of the resulting conductance weights versus pulse number, assuming that the green-colored (right) domain is parallel to the pinned layer and the orange-colored (left) domain is anti-parallel to the pinned layer. (d) Calculated conductance of the MTJ versus DW position at each notch in the free layer (blue curve) compared to a linear fit to the conductance change assuming no DW pinning (orange).

magnetic anisotropy of 1.5×10^6 J m^{-3}, exchange stiffness of 13×10^{-12} J m^{-1}, damping constant of 0.02, saturation magnetization of 1.44×10^6 A m^{-1}, and non-adiabatic constant of 0.02. The notches are 16 nm in diameter with a pitch of 64 nm. Using STT, we use 1 ns pulses of current density 2×10^{12} A m^{-2}, where the direction of the current depends on the relative timing of the pre- and post-synaptic neurons from the circuit model. The current density was chosen such that the current across the synapse is the same order of magnitude as the peak transient current in the circuit model. The pulses have a period of 10 ns.

The results of the micromagnetic simulation are shown in figure 5(a) as snapshots of the wire magnetization after the DW motion has stopped after each current pulse (view is $-\hat{z}$ compared to figure 1(a)). At the initial state 0 the DW is in the center of the free layer. Figure 5(b) depicts the polarity of the ten current pulses applied sequentially across the free layer.

We see that each current pulse moves the DW left or right depending on the timing delay between the pre- and post- signals. Thus, with a long MTJ placed on top of the free layer (not shown), this will controllably increase or decrease the MTJ conductance, setting the synaptic weight. It can be seen that each positive current pulse moves the DW to the left, getting pinned at subsequent notches, while each negative current pulse moves the DW to the right, also getting pinned at subsequent notches. Positive current pulses reduce the tunneling resistance of the device and hence increase the weight of the synapse while negative current pulses do the contrary.

In figures 5(c) and(d) we use measured numbers for CoFeB MTJs fabricated in our group of 166% tunnel magnetoresistance and 20 Ω μm^2 resistance-area (RA) product to convert the DW position to expected conductance weight. Figure 5(c) shows the expected conductance for each corresonding DW position in figure 5(a). Figure 5(d) shows the expected MTJ resistance when the DW sits at each notch (blue curve), compared to a linear fit if no notches are present (orange curve). Because the DW can be pinned at a particular notch for a long time if there is no current flowing, this gives the synapse a long-term memory effect. Also because the position of the DW along the free layer is a resultant effect of potentiation and depression over time, we can safely say that the synapse undergoes LTP and LTD.

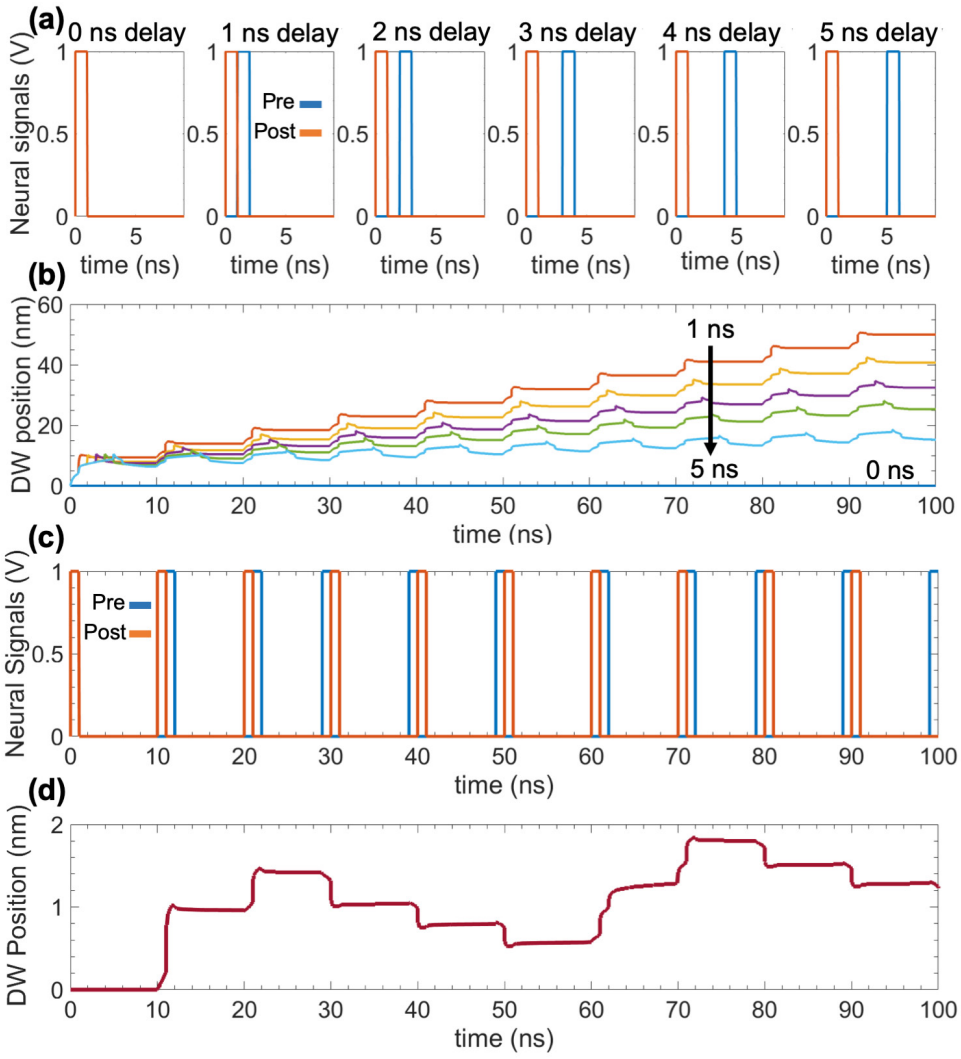

Figure 6. (a) Six modeled delay conditions between the pre- and post-synaptic signals, each simulated for ten cycles of 10 ns. (b) DW position output over time from the full SPICE model for the conditions in (a). Here the DW was initiated at the leftmost end of the free layer. (c) Modeled random train of delay conditions between the pre- and post-synaptic signals, with lead and lag times of 1 ns. (d) DW position output over time from the full SPICE model for the conditions in (c), showing the DW position, and therefore synaptic weight, is controlled by the timing between the signals.

The length of the MTJ compared to the length of the DW in x determines the number of notches and hence the number of DW positions that can represent different resistance or conductance weights. In a free layer with perpendicular magnetic anisotropy, the length of the DW L_{DW} is approximately determined by the width in $\hat{y}$ of the free layer, which is equal to the width of the MTJ, w_{MTJ}, as $L_{\mathrm{DW}} \approx \frac{W_{\mathrm{MTJ}}}{4}$ [62]. This means that with a MTJ of length L_{MTJ}, the maximum number of weights ($n_{weights}$) achievable will be given by the relation

$$n_{weights} \leqslant (L_{\mathrm{MTJ}}/L_{\mathrm{DW}}) \approx 4 \times L_{\mathrm{MTJ}}/w_{\mathrm{MTJ}}. \qquad (17)$$

Depending on the number of weights needed, the length of the free layer could be shortened to create more compact circuits. The notch depth and period was chosen empirically for given materials parameters to catch the DW after each pulse [63, 64].

It should be noted that the short pulse width of 1 ns used here mitigates heating effects from the higher current density [65] and hence ensures uniform predictable behavior of the synapse circuit. For short current pulses between 1–10 ns, the thermal diffusion length is 0.1–1 μm, larger than the free layer thickness of 4 nm; thus, we predict Joule heating will have little effect on the DW motion [65, 66].

3.4. Full SPICE simulation including domain wall dynamics

In sections 3.1–3.2, for the SPICE circuit model we used a resistor to represent the 3T-MTJ free layer. In section 3.3, to observe the effect of the circuit on the micromagnetic behavior of the 3T-MTJ synapse, we input the resulting current polarity from the circuit as a 1 ns current pulse of a fixed amplitude. Here, to capture the full dynamics of the circuit signal waveform (e.g. figure 3(a)) on the 3T-MTJ magnetic response, we implement a SPICE-only model of the full circuit that includes DW dynamics. We use a model of the 3T-MTJ for a notch-free free layer that we have previously developed with Verilog A and is benchmarked against micromagnetic simulations [45]. The 3T-MTJ model is connected via the *IN* and *CLK* terminals

Table 1. Head-to-head comparison of critical parameters for nanodevice and CMOS co-integrated unit cells for providing analog STDP learning (we do not consider here the comparison to probabilistic or binary schemes).

	CBRAM [67]	Metal oxide (Al_2O_3/TiO_{2-x}) [68]	Metal oxide ($BiFeO_3$) [69]	Polymer (PEDOT:PSS)/Ta [70]	2T-MTJ [37]	3T-MTJ (our approach)
$R_{Synapse}$	5–50 kΩ	10–40 kΩ	~1 MΩ	1–2.5 kΩ	400 Ω	100 Ω–10 kΩ
Switching time	2–4 μs	20 ms	125 μs	50 ms	<5 ns	<5 ns
$V_{post/pre}$	±1.3 V	±0.6–1.0 V	3.0 V+	±2.0 V	1.0 V	1.0 V
Analog STDP resolution	Intermediate (~5–10 states)	High (>20 states)	Intermediate (~10 states)	High (>30 states)	Low (2 states)	Intermediate (~10 states)

to the circuit, replacing the free layer resistor in the figure 1(d) circuit schematic.

With the same capacitance and resistance values ($R_{2,L} = R_{2,R} = R_2 = 10$ kΩ and $C_{2,L} = C_{2,R} = C_2 = 1 \times 10^{-12}$ F) used for the simulation in figure 2, we simulate ten cycles of six constant delay conditions between onset of the pre-synaptic signal and onset of post-synaptic signal. The six delay conditions are shown in figure 6(a). The transient DW position is shown in figure 6(b). With 0 ns delay, the DW does not move. The DW responds to each spiking of the circuit by moving an incremental distance across the free layer, and it is evident that the shorter the non-zero delay, the farther the DW moves after each firing and over the ten cycles, showing STDP behavior.

In figure 6(c), we randomly vary the timing of the pre- and post-synaptic signals with 1 ns lead or lag between the signals. Figure 6(d) shows that in response to this pulse train the DW moves left or right depending on the polarity of the resulting current spikes across the 3T-MTJ free layer. These results show that including the precise waveform of the circuit corroborates the micromagnetic results. We do see some irregularities in how far and how smoothly the DW moves in response to multiple similarly-timed pulses, which shows that external pinning may be important for controlling the conductance weights.

3.5. Benchmarking against competing STDP implementations

The results of our micromagnetic and SPICE simulations allow us to make a comparison to other state-of-the-art proposals for nanodevice plaforms for implementing online STDP learning. Specifically, we consider how our analog STDP implementation using 3T-MTJ devices compares to phyically realized or proposed analog STDP building block cells using 2T-MTJs [37], CBRAM [67], metal oxide [68, 69], or polymeric [70] active switching layers. As visible in table 1, the signature advantage of our system is its extreme (nanosecond range) STDP time window; the second fastest device, a CBRAM option, is over two orders of magnitude slower, and the other listed nanodevice options are slower still. Since this window serves as a speed limit for overall STDP learning, this could finally allow for online STDP learning functions in an integrated circuit co-integrated with NVM devices in an industrially-relevant context. Our proposal compares favorably in terms of required voltage, and is comparable though not superior in terms of analog resolution provided by other nanodevices. Our proposal's major weak point relative to competing options is the relatively low resistance and on/off ratio provided by MTJ devices. However, this issue may be ameliorated by further device engineering.

4. Conclusions

We have successfully designed a 3T-MTJ synapse circuit that achieves STDP, LTP, and LTD, essential characteristics of biologically-inspired artificial synapses. We observe that the transient form of the current generated across the synapse corresponds to what is seen in biology, and that shorter delay between the pre- and post- neuron firing results in higher current for potentiation or depression, which shows high similarity to biological neuron behavior. We show that the circuit can acheive a semi-analog pinning of the DW along the length of the ferromagnetic free layer of a 3T-MTJ using notches, and that the DW position can be set using the concept of STDP when integrated with the circuit. Including a SPICE model for the 3T-MTJ, we see the DW responds to the transient current with LTP and LTD behavior. This is key progress towards making more bio-realistic artificial synapses with multiple weights, which can also be trained online with a promise of CMOS compatibility and energy efficiency. Future work is needed to understand the impact of the additional circuitry for STDP on scaling and circuit density. The results shown can be in the future integrated with the LIF neuron in a crossbar array fashion and used for online machine learning applications in tasks like pattern or speech recognition.

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