Two-Stage 48V-1V Hybrid Switched-Capacitor Point-of-Load Converter with 24V Intermediate Bus

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***Abstract*—This paper presents a 90.6% 48 V-1 V/150 A two-stage hybrid switched-capacitor point-of-load (PoL) converter with a 24 V intermediate bus. The first stage of the converter is a 2:1 resonant charge pump which converts the 48 V input voltage to 24 V. The second stage of the converter is a 24:1 four-phase series capacitor buck converter which is capable of delivering 150 A with two customized four-phase coupled inductor for vertical power delivery. The two-stage architecture combines the resonant switched-capacitor structure and the series capacitor buck configuration to achieve high efficiency, high power density, and voltage regulation. The effectiveness of the topology is verified by a 48 V-1 V/150 A prototype with a peak efficiency of 90.6% at 60 A and a full load efficiency of 86.2% at 150 A. The power density of the prototype is 283 W/in^3.**

***Index Terms*—point-of-load, switched-capacitor converter, voltage regulator, soft-switching, soft-charging.**

I. Introduction

The power consumption of modern microprocessor is growing as the computing needs, yielding challenges to both point-of-load (PoL) voltage regulation and data center power delivery. High efficiency, high power density and high bandwidth PoL converters are needed to support hundreds of ampere of current at very low voltage (i.e., <1 V) for future high performance microprocessors. The data center industry is undergoing the transition from the conventional 12 V bus architecture to the 48 V bus due to the increasing server power consumption, which provides the benefits in higher overall rack efficiency and thinner wire [1]. Delivering power at 48 V bus can also leverage the existing 48 V telecom power ecosystem. Various 48 V PoL topologies have been explored [2]–[7]. Among these the two-stage intermediate bus architecture (IBA) is widely adopted due to its balanced performance in efficiency, density, and ease of implementation. In a two-stage IBA design, the front-end stage is usually implemented as a 48 V-12 V isolated dc-dc converter [2], [3], or switched-capacitor circuits [4]–[7] without voltage regulation capability. A 12 V multiphase interleaved buck converter is usually used as the second stage.

A few 48 V two-stage architectures with lower intermediate bus voltage (e.g., 4 V, 6 V, 8 V) have been explored recently [5], [8], [9]. Lower intermediate bus voltage brings the benefits of better switch utilization and better device performance to the buck stage. Fig. 1 shows the specific on-resistance of a group of N-channel MOSFET bare die manufactured by Infineon [10]. The specific on-resistance is the product of the switch's on-resistance and the die area. The device with lower breakdown voltage has lower specific on-resistance, which means higher current capacity for the same die area. Furthermore, the multiphase buck converter can switch faster with lower intermediate bus voltage to provide better transient response for the microprocessors. Lower bus voltage can also reduce the switching loss and switch stress. However, reducing the intermediate bus voltage requires higher voltage conversion ratio in the first step-down stage with either higher power stress or higher component count. The trade off between the two stages' voltage conversion ratios must be well balanced to achieve the optimal system performance.

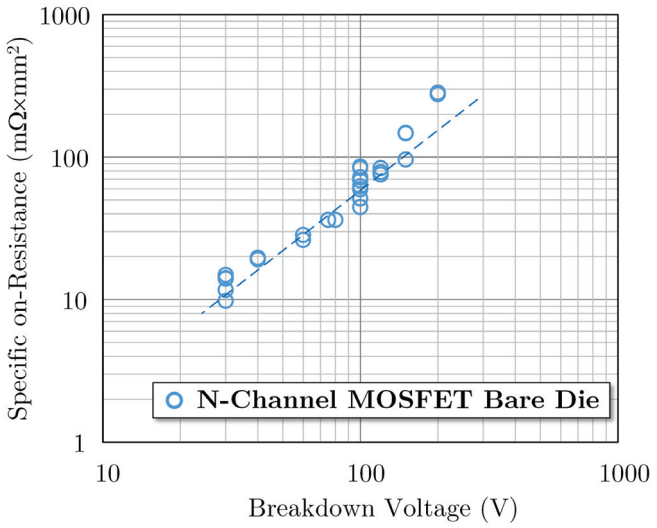

Fig. 1. Survey of the specific on-resistance of silicon MOSFETs. The data is collected from Infineon's N-channel MOSFET bare die datasheets [10].

This paper presents a two-stage hybrid switched-capacitor (HySC) converter for high current 48 V PoL applications with a 24 V intermediate bus. Benefiting from a four-level series-capacitor mechanism in the second stage, the effective intermediate bus voltage is only 6 V. Switched-capacitor circuits are used in both stages to balance the voltage conversion ratio and the power loss. The first stage is a 2:1 resonant charge pump converter performing 48 V-24 V conversion with very high power density and efficiency. The second stage is a four-phase series capacitor buck converter which performs 24 V-1 V conversion and output voltage regulation. Compared to a transformer based first stage, the 48 V-24 V resonant

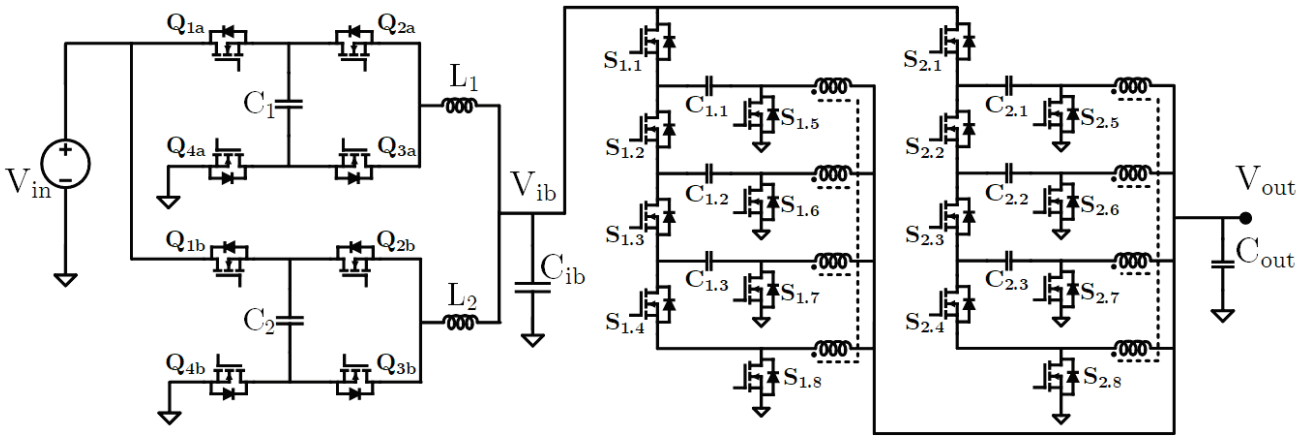

Fig. 2. The 48 V-1 V two-stage hybrid-SC topology: a front-end interleaved resonant charge pump and a second series capacitor buck stage with two parallel modules for high current load. The output inductors of the series-capacitor buck converter are coupled.

charge pump implementation eliminates the transformer and offers greatly reduced device stress. Compared to a multiphase buck second stage, the series capacitor buck converter offers reduced device rating and extended duty ratio for 24 V-1 V conversion. This paper also investigates the use of coupled inductor in the series capacitor buck converter, which can enhance the transient response to the load steps [11], [12]. The circuit topology and operation principles of the 48 V-1 V two-stage hybrid switched-capacitor converter are presented. The 48 V-1 V/120 A prototype has achieved a peak efficiency of 90.6% at 60 A and a full load efficiency of 86.2% at 150 A.

II. Topology and Operation Principles

A. 48 V-24 V 2:1 Resonant Charge Pump

Fig. 2 shows the full topology of the 48 V-1 V two-stage hybrid-SC converter. The first stage comprises two interleaved resonant charge pump converters for 48 V-24 V conversion. They are controlled by a pair of complementary gate drive signals with 50% duty ratio. The resonant operation enables high utilization of magnetics as well as soft-switching opportunities. The interleaving operation of the two resonant charge pumps guarantees continuous input current and reduces the input capacitor size. This 2:1 resonant charge pump converter is unregulated. It operates at a fixed frequency and can achieve very high efficiency and power density.

The control signals of the resonant charge pump stage are shown in Fig. 3. One switching cycle (T_{s1}) can be divided to four operational phases: two charging/discharging phases (Phase 1 and Phase 2) and two dead-time phases (DT 1 and DT 2). The control signals of the lower switches (Φ_{3a}, Φ_{4a}, Φ_{3b}, Φ_{4b}) are modified from the high side control signals (Φ_{1a}, Φ_{2a}, Φ_{1b}, Φ_{2b}) by increasing the dead-time to ensure zero-current-switching. The circuit states of the resonant charge pump in Phase 1 and Phase 2 are shown in Fig. 4. The charging and discharging state of the the two capacitors in the charge pump are swapped. During the dead-time period low side control signals are low while high side control signals are still high. The resonant current is freewheeling in the body-diode of MOSFET and will be naturally blocked after it falls to zero.

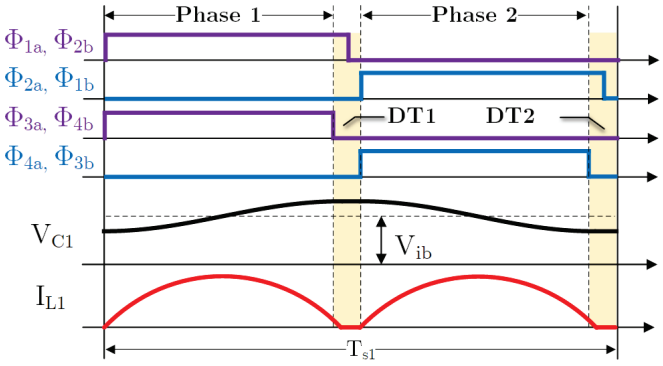

Fig. 3. Control signals, capacitor voltage and inductor current of the resonant charge pump stage. There is a deadtime between the switching of the two switches in the resonant charge pump.

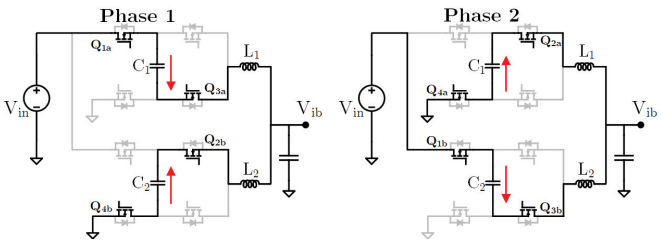

Fig. 4. Circuit states of the resonant charge pump in Phase 1 and Phase 2. The charging and discharging states of the the two capacitors in the charge pump are swapped and the center node voltage is 1/2 of the input voltage.

Thus, all the switches in the resonant charge pump stage can achieve zero-current-switching for both turn-on and turn-off actions. The two inductors at the output of the resonant charge pump can be merged together.

In a typical switched-capacitor converter, capacitors are forced to be connected in parallel. The voltage difference among capacitors causes high current spikes and charge sharing loss. In the resonant charge pump stage, capacitors C_1 and C_2 are never directly connected in parallel. C_1 and C_2 are softly charged/discharged by the sinusoidal resonant current with low root-mean-square value and low peak stress.

B. 24 V-1 V Four-Level Series Capacitor Buck Converter

The second stage comprises two parallel connected series capacitor buck modules with multiphase coupled inductors. Similar series capacitor multiphase buck converters with non-coupled discrete inductors were explored in [14]–[16]. The series-input parallel-output configuration of the series capacitor buck converter decouples the voltage stress from the input side and current stress from the output side. The 24 V intermediate bus voltage is equally distributed among the four levels. Four series-stacked switches and their complementary switches are controlled in a similar way as an interleaved multiphase buck converter with 6 V as the switch node voltage. The dc voltage bias is supported by three series capacitors ($C_{1.1}$, $C_{1.2}$, $C_{1.3}$ and $C_{2.1}$, $C_{2.2}$, $C_{2.3}$) with dc bias of 18 V, 12 V, 6 V from top to bottom, respectively.

Fig. 5 shows the control signals, the drain-source voltage, and the drain-source current of one four-phase series capacitor buck module. Fig. 6 shows the current flow of the series capacitor buck module in one switching cycle (T_{s2}). The control signals of the four phases are equally interleaved. The duty ratios ($D_1 - D_4$) of each high side switch ($S_{1.1} - S_{1.4}$) are smaller than 25% to charge/discharge the series capacitors ($C_{1.1} - C_{1.3}$) in sequence. Each series capacitor buck phase is performing 6 V-1 V conversion and all switches are switching at 6 V. The voltage stress of the low side switches ($S_{1.5} - S_{1.8}$) is 6 V, which is the same as the low side switches in a 6 V-1 V buck converter. The voltage stress of $S_{1.1}$ is also 6 V. The maximum voltage blocked by $S_{1.2}$, $S_{1.3}$ and $S_{1.4}$ are 12 V. The maximum current of each high side switch is equal to the inductor current, which is also similar to a 6 V-1 V buck converter. The current ratings of the three low side switches ($S_{1.5} - S_{1.7}$) are higher because they need to carry the freewheeling current for their own phase and the charging current for the neighboring phase for a short period. This results in higher root-mean-square (RMS) current and higher conduction loss compared to a multiphase buck converter. The current waveform of $S_{1.8}$ remains the same as a low side switch in a 6 V-1 V buck converter.

With similar voltage stress, current stress and duty ratios, the 24 V-1 V four-phase series capacitor buck converter is expected to achieve similar performance as a 6 V-1 V four-phase buck converter. Furthermore, as a hybrid switch-capacitor topology, $C_{1.1} - C_{1.3}$ in the series capacitor buck converter are softly charged/discharged by the inductor current with square wave operation. The size of these capacitors are limited by the equivalent series resistance but not the maximum voltage ripple. The capacitors can be sized small because charge sharing loss is eliminated by soft-charging.

III. Current Sharing and Voltage Balancing

Each switched capacitor of the second stage is charged by one inductor current for one ON-period, and discharged by another inductor current during the ON-period of the next level. For example, $C_{1.1}$ is charged by $i_{L1.1}$ from t_0 to t_1 and discharged by $i_{L1.2}$ from t_2 to t_3. By applying the voltage-second balance of inductor and the charge balance of the series capacitor in each phase, the large signal average capacitor

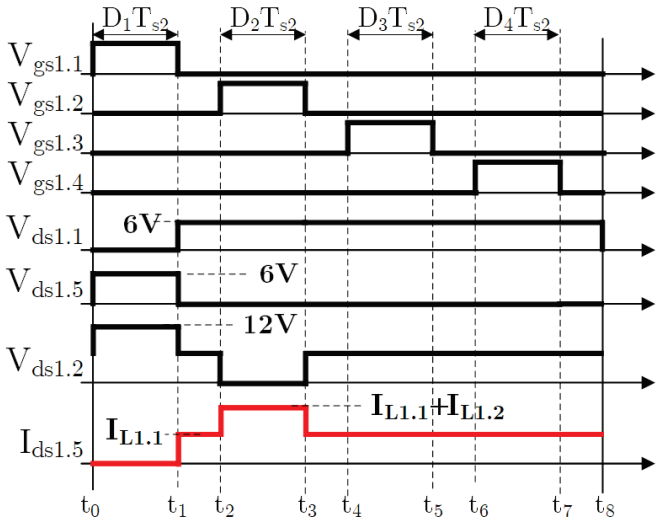

Fig. 5. Control signals and drain-source voltages of one four-phase series capacitor buck module. The peak current stress of three low side switches ($S_{1.5} - S_{1.7}$) and peak voltage stress of three high side switches ($S_{1.2} - S_{1.4}$) are doubled for a short period of time.

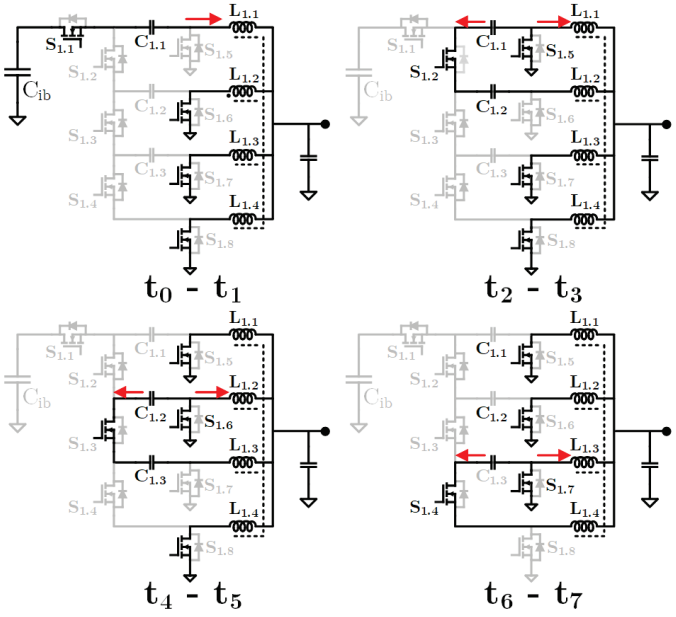

Fig. 6. The current flow in the four-phase series capacitor buck module. Charge is transferred step-by-step from the top level to the bottom level while soft-charging all the series capacitors.

voltage and inductor current of the four-phase series capacitor buck converter are:

$$V_{out} = D_1(V_{ib} - V_{C1.1}) = D_2(V_{C1.1} - V_{C1.2}) = D_3(V_{C1.2} - V_{C1.3}) = D_4 V_{C1.3}, \quad (1)$$

$$D_1 I_{L1.1} = D_2 I_{L1.2} = D_3 I_{L1.3} = D_4 I_{L1.4}. \quad (2)$$

Here $V_{C1.1} - V_{C1.3}$ are the average voltage of $C_{1.1} - C_{1.3}$ and $I_{L1.1} - I_{L1.3}$ are the average current of $L_{1.1} - L_{1.4}$. Combining

TABLE I
BILL-OF-MATERIAL OF THE PROTOTYPE

C_1, C_2	Murata 0805 35 V/10 μF×6, C_{eq}=7.62 μF
C_{ib}	TDK 0805 35 V/15 μF×40, C_{eq}=40 μF
$C_{1.1}$, $C_{2.1}$	Murata 0805 25 V/22 μF×7, C_{eq}=17.4 μF
$C_{1.2}$, $C_{2.2}$	Murata 0805 25 V/22 μF×4, C_{eq}=15.0 μF
$C_{1.3}$, $C_{2.3}$	Murata 0805 25 V/22 μF×2, C_{eq}=17.2 μF
C_{out}	Murata 0805 6.3 V/47 μF×40, C_{eq}=1.6 mF
L_1, L_2	Coilcraft 110 nH/1.5 mΩ, 4 × 4 × 2 mm
$L_{1.1}$-$L_{1.4}$, $L_{2.1}$-$L_{2.4}$	Coupled Inductor shown in Fig. 8
$S_{1.1}$-$S_{1.4}$, $S_{2.1}$-$S_{2.4}$	BSZ0506NS, 25 V/4.4 mΩ
$S_{1.5}$-$S_{1.8}$, $S_{2.5}$-$S_{2.8}$	BSZ011NE2LS5I, 25 V/1.1 mΩ
Charge pump switch	IPZ40N04S5L-7R4, 40 V/7.4 mΩ
Gate driver	TI LM5108, half bridge

(1) and (2), the steady state value of the state variables are:

$$\begin{aligned} V_{C1.1} &= GV_{ib}\left(\frac{1}{D_2}+\frac{1}{D_3}+\frac{1}{D_4}\right), \\ V_{C1.2} &= GV_{ib}\left(\frac{1}{D_3}+\frac{1}{D_4}\right), \\ V_{C1.3} &= GV_{ib}\frac{1}{D_4}, \\ I_{L1.1} &= \frac{I_{out}}{GD_1}, I_{L1.2} = \frac{I_{out}}{GD_2}, \\ I_{L1.3} &= \frac{I_{out}}{GD_3}, I_{L1.4} = \frac{I_{out}}{GD_4}. \end{aligned} \tag{3}$$

Here I_{out} is the average output current. $G = \frac{V_{out}}{V_{ib}} = \frac{1}{\frac{1}{D_1}+\frac{1}{D_2}+\frac{1}{D_3}+\frac{1}{D_4}}$ is the voltage conversion ratio. If all four phases have the same duty ratio, their average inductor currents are equal as well. Thus, the current balancing is ensured when $D_1 = D_2 = D_3 = D_4$. The average voltage of the series capacitors are also controlled by the duty ratio. With equal duty ratio the average voltages of three series capacitor are $\frac{3V_{ib}}{4}$, $\frac{2V_{ib}}{4}$ and $\frac{V_{ib}}{4}$, respectively.

Usually, the duty ratio of each phase of the series capacitor buck converter needs to be smaller than $1/N$, where N is the number of phases. It is possible to operate the series capacitor buck converter with $D > 1/N$, which is beyond the scope of this paper. The maximum voltage conversion ratio of a series capacitor buck converter with N series-stacked phases is N^2 : 1. For a 4-phase series capacitor buck design, a 25% duty ratio leads to a voltage conversion ratio of 16:1. For example, with a 24 V input voltage, the nominal output voltage is 1.5 V, and can be regulated between 0 V and 1.5 V by changing the duty ratio. A lower duty ratio leads to lower output voltage for the point-of-load converter. With the 2:1 front-end stage, the overall voltage conversion ratio is:

$$\frac{V_{out}}{V_{in}} = \frac{1}{2}\frac{1}{\frac{1}{D_1}+\frac{1}{D_2}+\frac{1}{D_3}+\frac{1}{D_4}}. \tag{4}$$

With equal duty ratio of four levels ($D_1 = D_2 = D_3 = D_4 = D$), the overall voltage conversion ratio is $D/8$.

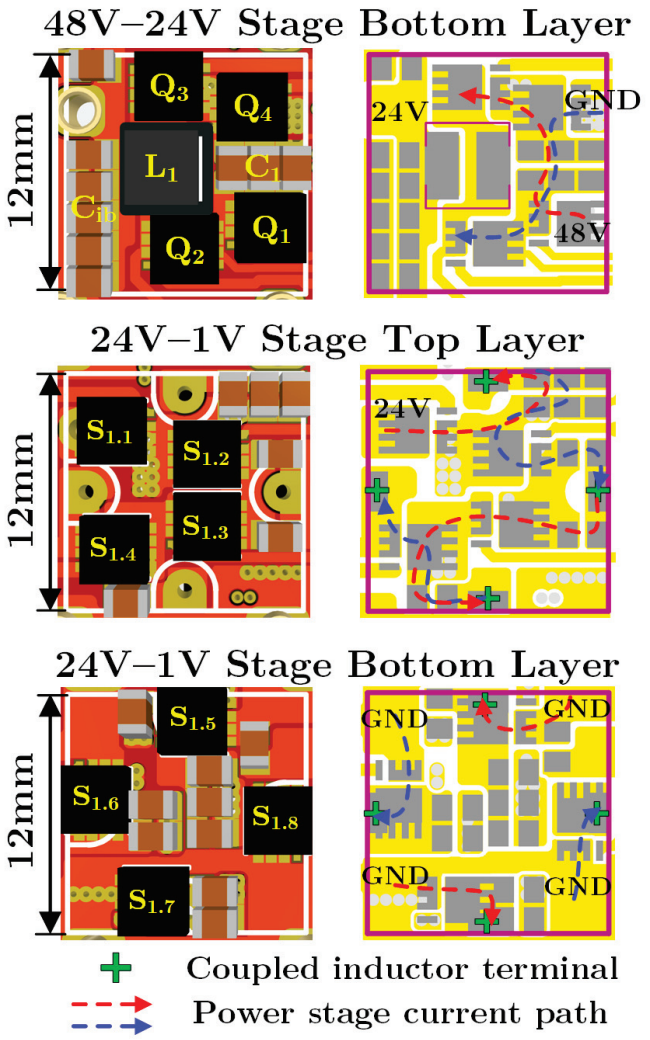

Fig. 7. The components placement and the power stage layout of 48 V-24 V charge pump stage and the 24 V-1 V series buck stage. The components of one charge pump module and one series capacitor buck module are placed within a 12 mm×12 mm square area.

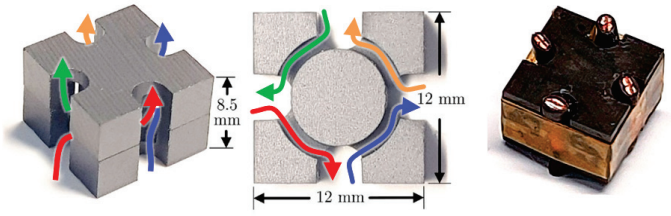

Fig. 8. The customized four phase coupled inductor. The inductor size is 12 mm×12 mm×8.5 mm. The turns number of each winding is 1. The winding current is wrapped around the center rod for 90° and vertically delivered from the series capacitor buck stage to the motherboard.

IV. PROTOTYPE DESIGN

A 48 V-1 V 150 A two-stage hybrid-SC converter was designed and fabricated. The circuit schematic is the same as Fig. 2 including two 48 V-24 V resonant charge pump converters and two 24 V-1 V series capacitor buck converters. Table I listed the bill-of-material (BOM) of the prototype.

The charge pump switches are all zero-current-switching. The switching loss is mostly contributed by the output capacitance (C_{oss}) loss. It grows linearly with the switching frequency. The current rating of the first 48 V-24 V stage is not as high as the second stage and it is beneficial to use switches with low C_{oss} to maximize the efficiency. Reducing the switching frequency can also improve the efficiency of the resonant charge pump stage but the resonant elements (capacitors and inductors) may become larger. The measured resonant frequency of the resonant charge pump stage is 174 kHz (considering capacitance degrading). The switching frequency is adjusted and selected as 166 kHz to guarantee sufficient dead-time for the zero-current-switching operation.

Fig. 7 shows the components placement and the power stage layout of 48 V-24 V charge pump stage and the 24 V-1 V series buck stage. Each charge pump module and series capacitor buck module occupies a 12 mm×12 mm square area for the components of the power stage (switches, capacitors and inductors). The top layer of the charge pump stage is used for intermediate bus capacitors and not shown in Fig. 7. The dash lines point out the current flow path of the power stages. The PCB layout can guarantee symmetrical current paths for the two operational phases of the charge pump stage and four series capacitor buck phases.

A four-phase coupled inductor is designed for the series capacitor buck stage. Fig. 8 shows a few pictures of the coupled inductor. The coupled inductor is placed between the buck board and the motherboard. The length and width of the coupled inductor are equal to the length and width of one series capacitor buck module. The magnetic core is customized with 3F4 ferrite material with a 2.3 mm air gap on the center rod. All windings are single turn windings with Litz wire (Φ=5 mm×160×2) and wrapped around the center rods for 90°. With D=1/6, the per phase transient inductance L_{ptr} is 73 nH and the per phase steady state inductance L_{pss} is 400 nH [11], [12]. The coupled inductor reduces the output current ripple by 82% while maintaining the same transient response.

Fig. 9 shows a picture of the prototype including two daughter boards (resonant charge pump and series capacitor buck) and one motherboard. The middle board and the top board have the same board size and are stacked on the motherboard. The PCB area of the power stage (switches, capacitors and inductors) is 12 mm×12 mm. Fig. 10 shows the 3D assembly drawing of the prototype. Power is vertically delivered from the charge pump stage to the series capacitor buck stage, then to the motherboard. Three PCB boards are connected by plug-in power connectors. Fig. 11 shows the 3D drawing of the power stage. The dimension is 31 mm×14 mm×20 mm. The volume of the power stage including two charge pump modules, two series capacitor buck modules, output capacitors and power connectors is 8,680 mm^3 (0.53 in^3).

V. Experimental Results

Fig. 12 shows the measured capacitor voltage ripple, resonant inductor current and the drain-source voltage of the bottom switch in the resonant charge pump stage. The switching

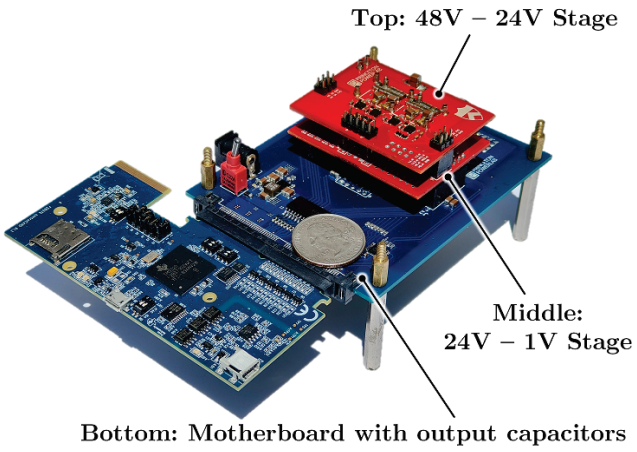

Fig. 9. The picture of the 48 V-1 V/150 A PoL converter. The middle board and the top board have the same board size and are stacked on the motherboard. The PCB area of the power stage (switches, capacitors and inductors) is 12 mm×12 mm.

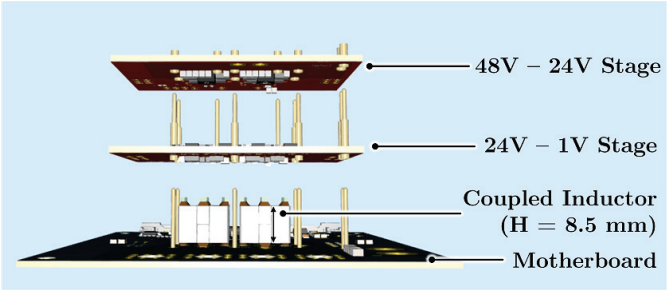

Fig. 10. 3D assembly drawing of the prototype. Power is vertically delivered from top (48 V), middle (24 V), to bottom (1 V).

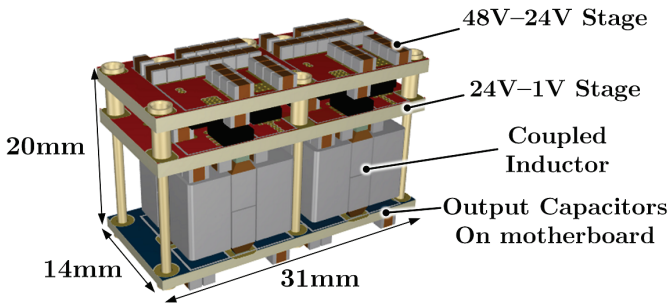

Fig. 11. 3D assembly drawing of the power stage including all MOSFETs, capacitors, and inductors. The gate drivers and control circuitry are not included. The dimension is 31 mm×14 mm×20 mm. The volume of the power stage including two charge pump modules, two series capacitor buck modules, output capacitors and power connectors is 8,680 mm^3 (0.53 in^3).

frequency of the interleaved resonant charge pump stage is 166 kHz which is slightly lower than the resonant frequency. Small period of zero-current state can be observed during the dead-time showing zero-current-switching is achieved. Fig. 13 shows the measured efficiency of the 48 V-24 V interleaved resonant charge pump stage. This stage achieves 99.2% peak efficiency at 100 W, and maintains above 99% efficiency at 300 W. Benefiting from the high efficiency, the power capacity of the first stage is much higher than the second series

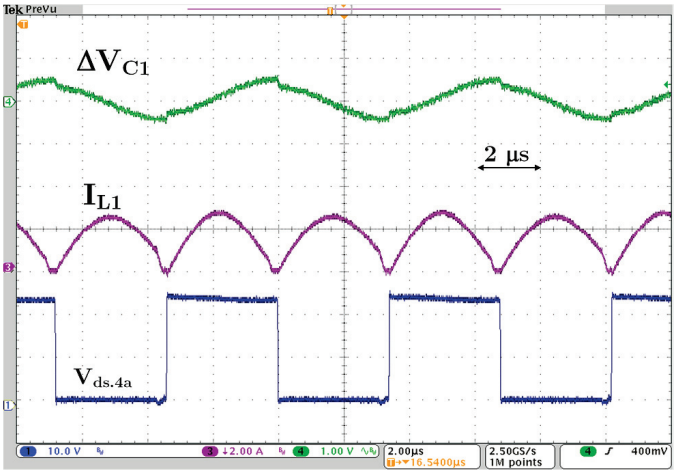

Fig. 12. Measured capacitor voltage ripple, resonant inductor current and the drain-source voltage of the bottom switch in the resonant charge pump stage.

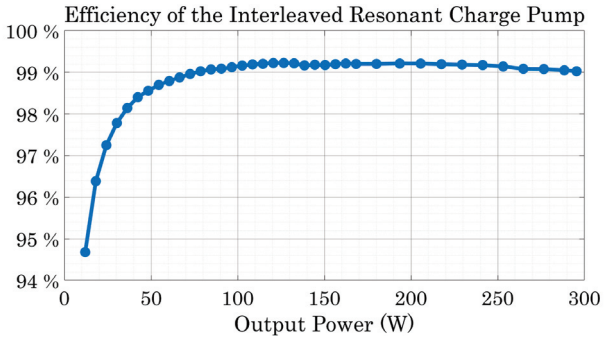

Fig. 13. Measured efficiency of the interleaved resonant charge pump stage with power up to 300 W.

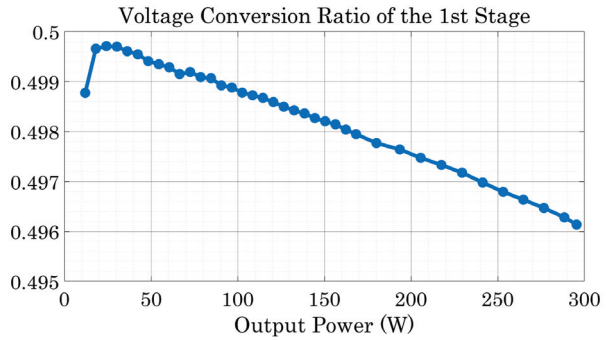

Fig. 14. Measured actual conversion ratio of the interleaved resonant charged pump stage. The output resistance of the 48 V-24 V stage is about 15.3 mΩ.

capacitor buck stage. It is able of delivering power to more paralleled series capacitor buck modules to cover higher output current range. Fig. 14 shows the measured voltage conversion ratio $\frac{V_{ib}}{V_{in}}$ of the first stage as a function of the output power. The output impedance of the first stage is very low. Its actual voltage conversion ratio slightly drops as the increment of the output power. The reduction of the intermediate bus voltage is less than 0.8% with the power up to 300 W.

The waveform of the series capacitor buck converter shown in Fig. 15 was measured with the customized coupled inductor at the switching frequency of 833 kHz. The duty ratio of

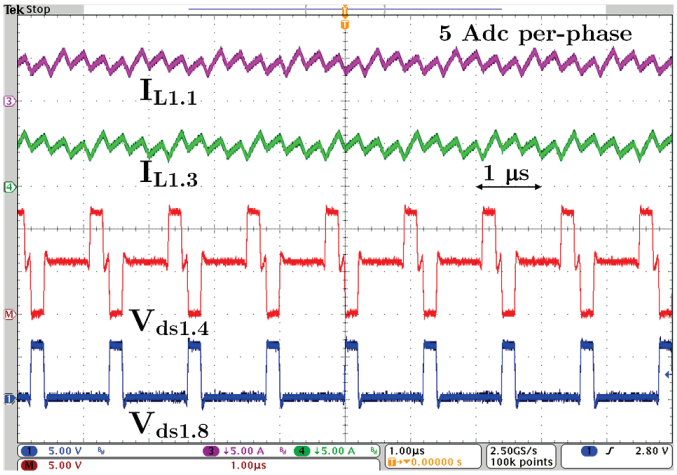

Fig. 15. Measured coupled inductor current, the drain-source voltage of a high side switch and a low side switch in the 24 V-1 V series capacitor buck converter working at 20 A/833 kHz.

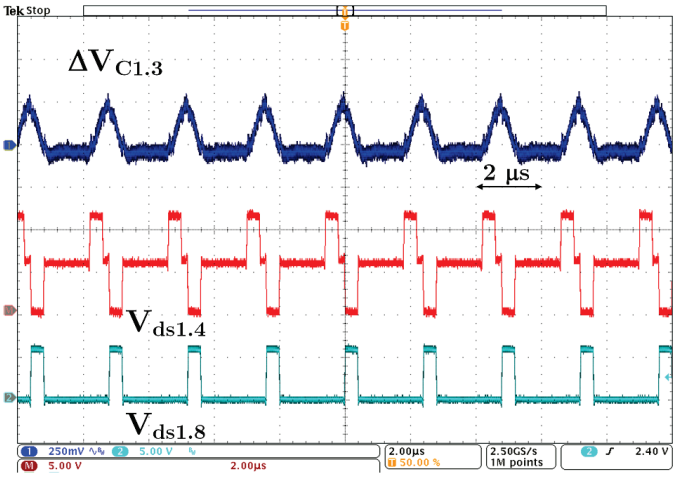

Fig. 16. Measured capacitor voltage ripple, the drain-source voltage of a high side switch and a low side switch in the 24 V-1 V series capacitor buck converter working at 60 A/416 kHz.

the four-phase series capacitor buck converter for 48 V-1 V conversion is 1/6. The ripple frequency of the coupled inductor current is four times of the switching frequency of the series capacitor buck converter. The peak-to-peak current ripple is 2.5 A, which means the per phase steady state inductance L_{pss} is 400 nH. The drain-source voltages of the high side switch and the low side switch match the theoretical analysis. The maximum voltage of $S_{1.4}$ is 12 V and the maximum voltage of $S_{1.8}$ is 6 V. Both of them are switching at 6 V. Fig. 16 shows the measured voltage ripple of $C_{1.3}$, the drain-source voltage of $S_{1.4}$ and $S_{1.8}$ in the 24 V-1 V series capacitor buck converter working at 60 A/416 kHz. The series capacitor is only charged for a period of DT_{s2} and then discharged for another period of DT_{s2} by the neighboring phase.

Fig. 17 shows the efficiency comparison of one 24 V-1 V series capacitor buck module with coupled inductor working at 416 kHz and 833 kHz. The output voltage is regulated at 1 V by a feedback loop during the efficiency measurement. The series capacitor buck module achieves 92.1% peak efficiency

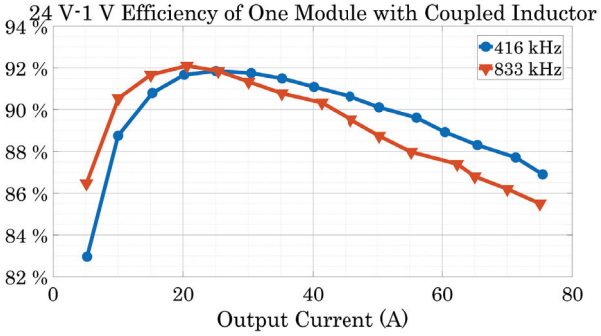

Fig. 17. Measured efficiency of one 24 V-1 V series capacitor buck module with coupled inductor.

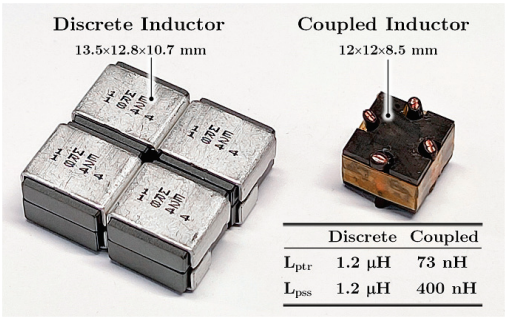

Fig. 18. Photograph of four discrete inductors and one four-phase coupled inductor. The per phase transient inductance (L_{ptr}) and the per phase steady state inductance (L_{pss}) of the discrete inductor are 1.2 μH. The L_{ptr} of the coupled inductor is 73 nH and the L_{pss} of the coupled inductor is 400 nH.

at 1 V/20 A, and above 85.5% efficiency at 1 V/75 A with the switching frequency of 833 kHz. It reaches a 91.8% peak efficiency at 1 V/25 A, and above 87% efficiency at 1 V/75 A with the switching frequency of 416 kHz. Two efficiency curves cross at output current of 25 A. Efficiency with 813 kHz is higher below 25 A, and efficiency with 416 kHz is higher above 25 A. One possible explanation is that the conduction loss is dominated by the current ripple with light load and by the average current with heavy load. Based on the coupled inductor design and the measured results, the peak-to-peak current ripple is 2.5 A with 833 kHz and 5 A with 416 kHz. In the case ripple is close or even larger than the average current, the root-mean-square (RMS) current of switches, capacitors and inductors is mostly determined by the current ripple. Higher current ripple leads to higher conduction loss. When the output current goes higher, the conduction loss with 2.5 A ripple and 5 A ripple is similar. The measured efficiency at 416 kHz is higher due to lower switching loss.

The four-phase series capacitor buck module is also tested with four discrete inductors (Wurth 34 A / 1.2 μH / 0.42 mΩ). The dimension of the 1.2 μH inductor is 13.5 mm$\times$12.8 mm$\times$10.7 mm. The total volume of the four discrete inductors is 7,396 mm^3 and the volume of the four-phase coupled inductor is 1,224 mm^3 (6x reduction). A photograph of them is shown in Fig. 18 and the measured efficieny is shown in Fig. 19 and Fig. 20. The per phase current ripple of the discrete inductor is 1/3 of the coupled inductor. The measured 24 V-1 V efficiency of the series-buck

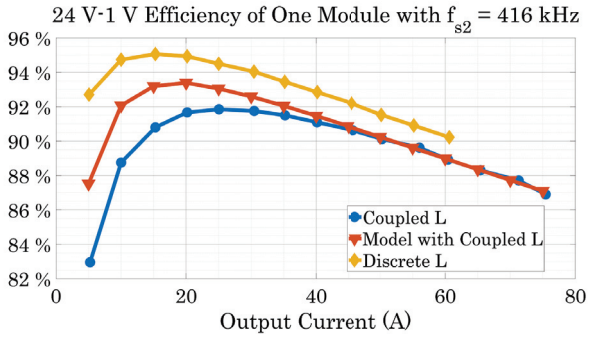

Fig. 19. Measured and calculated efficiency of one 24 V-1 V series capacitor buck module working at 416 kHz.

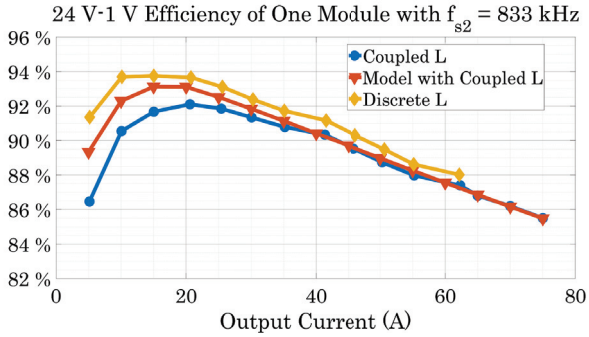

Fig. 20. Measured and calculated efficiency of one 24 V-1 V series capacitor buck module working at 833 kHz.

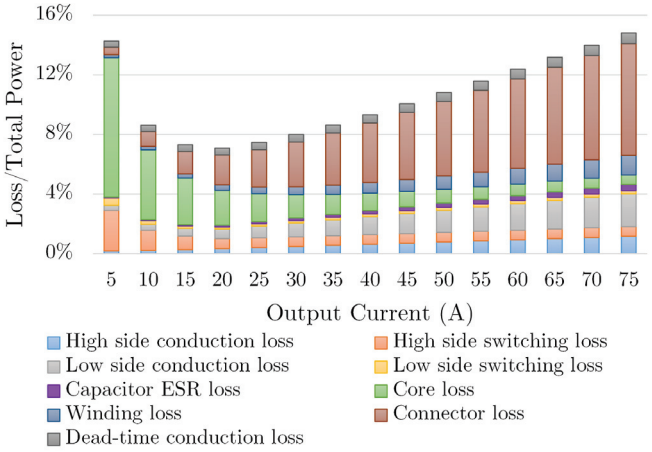

Fig. 21. Power loss analysis of one 24 V-1 V series capacitor buck converter with the coupled inductor inductor working at 416 kHz.

converter with discrete inductors is higher than the efficiency with coupled inductor. However, the overall volume of the four discrete inductors is 6x larger than that of the coupled inductor. The 6x smaller coupled inductor is slightly less efficient, but offers much higher power density and faster transient speed.

The calculated efficiencies of this design by modeling the coupled inductor are also shown in Fig. 19 and Fig. 20. The model closely matches with the experiment results at heavy load. The higher mismatch between them at light load is because of the uncaptured parasitic losses. Fig. 21 shows the loss analysis of one series capacitor buck module with

TABLE II
PERFORMANCE SUMMARY OF THE TWO-STAGE 48 V-1 V HYBRID SC CONVERTER

Circuit	Input	Output	Peak eff.	Full load eff.	PCB area	Box vol.	Power Density	Current Density
2:1 Resonant Charge Pump	48 V	~24 V	99.2% @120 W	99.0% @150 W	434 mm^2	0.122 in^3	1230 W/in^3	0.014 A/mm^2
24:1 Series Capacitor Buck	24 V	1 V	92.1% @40 W	87.0% @150 W	434 mm^2	0.408 in^3	368 W/in^3	0.346 A/mm^2
Two-Stage 48V-1V PoL	48 V	1 V	90.6% @60 W	86.2% @150 W	434 mm^2	0.530 in^3	283 W/in^3	0.346 A/mm^2

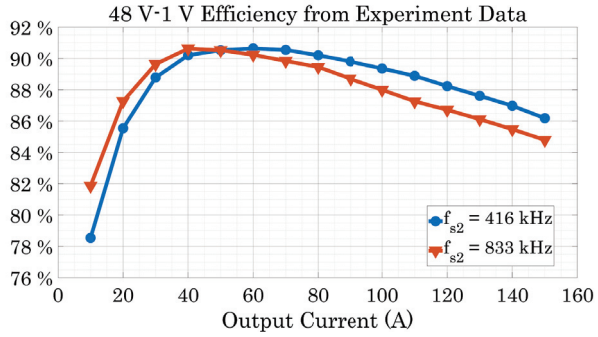

Fig. 22. Two-stage 48 V-1 V efficiency with output current up to 150 A.

416 kHz. The core loss of the coupled inductor dominates the overall loss at light load. The connector loss is the main obstacle which limits the efficiency and power capability of the second stage. The connector loss comes from the contact resistance of the power connectors and the resistance of the connector itself. As shown in Fig. 10, there are six pairs of connectors to connect the series capacitor buck board and the motherboard as the returning path for the output current. The measured resistance of the returning current path is around 1 mΩ, which takes almost 7.5% of the total output power with 75 A output current.

Fig. 22 shows the full system efficiency by combining the two stages with a 24 V intermediate bus. The peak system efficiency is 90.6% at 1 V/60 A, and the full load efficiency is above 86.2% with the series capacitor buck stage working at 416 Hz. The performance of the many building blocks of the two-Stage 48 V-1 V Hybrid SC converter is summarized in Table II. The power density of the 48 V-1 V system is 283 W/in^3, with a current density of 0.346 A/mm^2.

VI. CONCLUSIONS

This paper presents a two-stage hybrid switched-capacitor topology for 48 V-1 V point-of-load applications. The two-stage hybrid SC converter achieved soft-charging and soft-switching for both the front-end 48 V-24 V resonant charge pump and the back-end 24 V-1 V series capacitor buck. The series-input parallel-output configuration of the series capacitor buck stage decouples the voltage stress and current stress. Output current balancing of the 24 V-1 V stage is naturally achieved by the charge sharing mechanism with proper duty ratio control. A 48 V-1 V / 150 A point-of-load prototype with a peak efficiency of 90.6%, a full load efficiency of 86.2%, a power density of 283 W/in^3, and a current density of 0.346 A/mm^2 proved the effectiveness of the two-stage hybrid switched-capacitor architecture.

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