A Pattern-Based Analytical Method for Impedance Calculation of the Power Distribution Network in Mobile Platforms

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***Abstract*—A power distribution network (PDN) is essential in electronic systems to provide reliable power for load devices. With faster load transient current and lower voltage tolerance margin for microprocessors in mobile platforms, it is crucial to optimize the printed circuit board (PCB) design to satisfy the strict target impedance. Conventional modeling methods become impractical in mobile platforms due to the characteristics of high-density interconnect PCB and limited layout space. To overcome these issues, a pattern-based analytical method for the PDN impedance calculation is presented in this article. Based on the localized patterns formulated by the relative relationships between the adjacent vias, parasitic elements are analytically determined for different regions of the entire PCB structure. With the assistance of this method, a practical modeling methodology is developed to construct an equivalent circuit with one-to-one correspondence to the PCB's physical geometry. As a result, the PDN design can be efficiently optimized, especially in the predesign stage, to accelerate the development process. Finally, the proposed method is validated by measurements and full-wave simulations using a real mobile phone PCB in production.**

***Index Terms*—Design methodology, mobile platform, pattern-based analytical modeling, power distribution network (PDN), via inductance extraction.**

I. Introduction

A POWER distribution network (PDN) is essential in electronic systems to provide reliable power for load devices [1]. The primary objective of the PDN design is to ensure normal IC operations by minimizing voltage fluctuations [2]. With the evolution in technologies, modern active devices are being designed with lower voltage to meet faster and more efficient data processing demands. As a result, the current draw and slew rate keep increasing, while the voltage tolerance margin becomes tighter [3]. The mobile platform, being a typical industrial application that follows these trends, poses serious challenges to the PDN design. Driven by the ambitious user requirements, more aggressive architectures for mobile processors have been deployed to provide significant performance improvements [4]. However, it also results in a fast transient current and a strict target impedance at both dc and higher frequencies [5]. Furthermore, the high-density interconnect (HDI) printed circuit board (PCB) is commonly used in mobile platforms to increase the circuitry density. The complicated interconnect structure brings nonnegligible parasitic effects. In addition, the slim form factor of mobile phones limits the layout space and the number of surface mount decoupling capacitors, which causes difficulties to lower the PDN impedance. Thus, the PCB-level PDN design, including the parasitic elements associated with vias/power-ground planes and the decoupling capacitors, becomes more and more critical for mobile platforms.

Over the past few decades, PDN modeling has been extensively investigated. First, full-wave electromagnetic modeling methods were applied to study this problem, including the finite-difference time-domain method [6], the finite-element method [7], the method of moments [8], and the partial-element equivalent circuit [9]–[11]. In addition, a fast and straightforward transmission-line method (TLM) compatible for SPICE implementation was developed to model planes with bypass capacitors [12]–[14]. Another fast method based on the cavity model was commonly used to calculate the input impedance between the power-ground planes [15], [16]. The reduction techniques for the cavity model were also proposed to combine parasitic via inductance and generate equivalent circuits [17], [18]. However, due to the characteristics of the PCB in mobile phones, the existing methods either become impractical or have limitations to model the PDN in mobile platforms.

Fig. 1 compares the PCBs in mobile platforms and other common platforms, such as server or personal computer. The interconnect structure of PCB can be very complicated, especially for the HDI PCB in mobile platforms. As shown in Fig. 1(a), the 0.075-mm-diameter microvias in mobile platform PCB could result in a huge number of mesh cells for full-wave electromagnetic modeling methods. Hence, the computational burden is heavy and the simulation time is long. Similarly, due to the complexity of the geometry, the TLM model has to use a large

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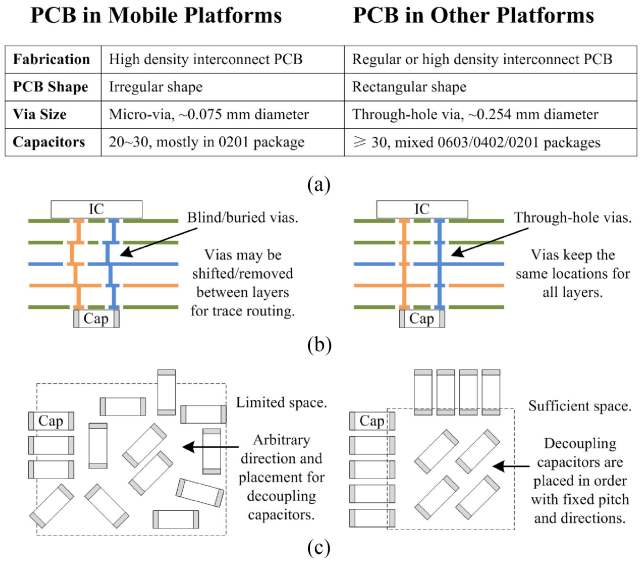


Fig. 1. Comparison of PCB in mobile platforms and PCB in other platforms. (a) Complexity of the interconnect structure. (b) Via types, blind/buried versus through-hole. (c) Direction and placement of the decoupling capacitors.

number of circuit elements to converge with a good simulation accuracy. Fig. 1(b) illustrates the difference in via types. All the vias in mobile platform PCB are blind/buried, while those in regular PCB are through-hole. The cavity model method, which requires the positions of all the vias as the model's ports, is only suitable for the through-hole case. For through-hole vias, the port locations for all the cavities formed by different plane pairs are exactly the same. Thus, the positions only need to be identified once using one cavity; then, they can be applied to other cavities for further calculation. However, the blind/buried vias may be removed or shifted between cavities to make room for routing traces within a limited layout space. In this case, the via positions have to be determined separately for every cavity, which significantly increases the workload. In addition, the cavity model method cannot handle the "dog-bone" traces between the blind/buried vias easily. Another factor related to the port locations is depicted in Fig. 1(c). Since the decoupling capacitors should be placed close to the power/ground vias to minimize the parasitic inductance, the positions of decoupling capacitor's power/ground pads can be used to identify the port locations of the cavity model. For the regular PCB with sufficient layout space, the decoupling capacitors are placed in order with fixed pitch size and the same direction, so their positions can be easily determined. However, for the mobile platform PCB with limited layout space, the decoupling capacitors are arbitrarily placed with random directions. It is difficult to find the absolute positions for all the decoupling capacitors. Therefore, the cavity model method is impractical to model the PCB in mobile platforms. At last, technical change and new product proliferation have made the mobile phone industry extremely dynamic [19], which places greater demands on accelerating the development process. In spite of the existing methods that only focus on the postvalidation stage (the PCB layout has already been completed), the PDN design and modeling in the predesign stage are rarely investigated. Thus, it is desired to develop a PDN modeling method that is suitable for mobile platforms and applicable in the predesign stage.

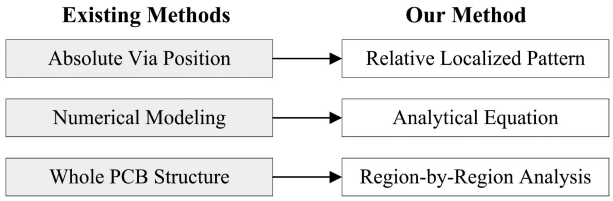


Fig. 2. Major improvements of the proposed pattern-based analytical method.

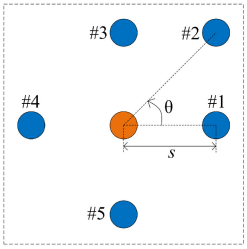
To overcome the limitations of the existing methods for the PCB in mobile platforms, a novel pattern-based analytical method is proposed for PDN impedance calculation. Our method aims to achieve three major improvements, as shown in Fig. 2. First, instead of using the absolute positions of all the vias and decoupling capacitors, the parasitic elements are calculated based on the localized patterns. Section II discusses the formulation of pattern and its benefits. Second, the complicated numerical solutions lack flexibility in the predesign stage, so, in Section III we integrate the analytical equations and introduce a modeling methodology applicable to both predesign and postvalidation stages. Third, in addition to modeling the whole PCB structure, our method is capable of conducting region-by-region analysis. These regions still maintain one-to-one correspondence to the physical geometry, which is helpful to identify the dominant factors in the PDN design. In Section IV, our method is validated by both whole structure and region-by-region comparisons using a real mobile phone PCB in production. Finally. Section V concludes this article.

II. Pattern Formulation and Calculation

A novel approach to calculate the parasitic elements of vias is presented in this section based on the localized via patterns. Compared with the conventional methods using the absolute via positions, our method possesses better flexibility to handle the complicated PCB structures in mobile platforms. The accuracy of our method is validated by simulations under various conditions. Since the via pattern is a 2-D structure, the sensitivity of the edge effect is also investigated.

A. Pattern Formulation

As discussed earlier, the conventional PDN modeling methods become impractical in mobile platforms. It is desired to develop a new modeling method based on the characteristics of the mobile platform PCB. With the limited layout space and tight trace routing restriction, the via-in-pad technique is extensively used for space optimizations. As a result, the relative relationships (distance and angle) between the adjacent vias on the top and bottom layers can be directly obtained from the IC's pinout and decoupling capacitor's footprint. If the blind/buried via is shifted or removed on the internal layers, only the moved via needs to establish new relative distance and angle with its adjacent vias, while the relative relationships of all other vias remain the same.



Ground Via	Distance (s)	Angle (θ)
#1	s_{min}	0°
#2	$\sqrt{2}s_{min}$	45°
#3	s_{min}	90°
#4	s_{min}	180°
#5	s_{min}	270°

Power Via Ground Via

Fig. 3. Localized via pattern of the power via and its surrounding ground vias. The distance s and angle θ of ground vias are referenced to the power via. The minimal distance between the power and ground vias is $s_{\min}$.

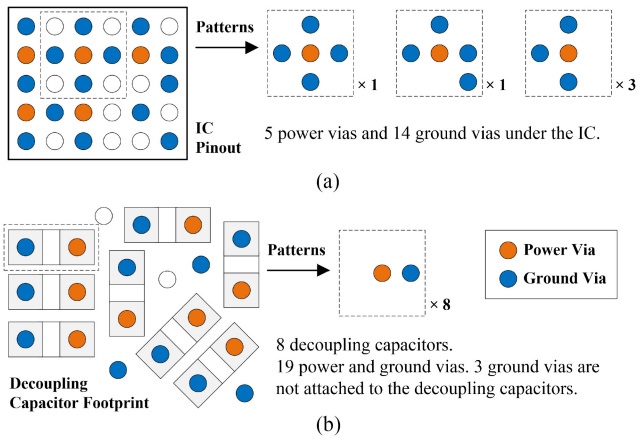


Fig. 4. Formulated via patterns of two categories. (a) Via patterns in the IC region. (b) Via patterns for decoupling capacitors.

Therefore, the relative distances and angles of the power and ground vias can be easily determined across all layers. Another attribute of the mobile platform PCB, as shown in Fig. 1(a), is the usage of decoupling capacitors with the same package. Restricted by the limited space, almost all the surface mount decoupling capacitors use the small 0201 package. It not only simplifies the PCB layout, but also reduces the variations of the relative distance between the power and ground vias for all the decoupling capacitors.

To represent the relative relationships between the adjacent vias, the localized via pattern is defined to include each power via and its surrounding ground vias. To effectively identify each via's position, the via pattern records the distance s and angle θ between each ground via and the centered power via, as illustrated in Fig. 3. Note that the zero-degree axis can be defined from any ground via, because we only care about the relative relationships of the vias. Based on the information in Fig. 3, the distance between any two ground vias can be further calculated. Thus, the relative positions of the included vias can be uniquely determined by the via pattern.

Depending on the connected components, there are mainly two categories of vias on the top and bottom layers: the IC vias and the decoupling capacitor vias. Examples of these two categories are depicted in Fig. 4.

1) For the IC vias in Fig. 4(a), three patterns are formulated based on the IC pinout. Since the pads under IC are well organized with the fixed pitch size, by applying the via-in-pad technique, the distances between the power and ground vias can be easily determined as either 1 or $\sqrt{2}$ times of the pitch size. The angles are simply multiples of 45°.
2) For the decoupling capacitor vias in Fig. 4(b), only one pattern is needed to represent all eight decoupling capacitors with the same package. This pattern is formulated by the two vias in each capacitor's power and ground pads, as it provides the least impedance path for the current. Even though these capacitors are randomly placed and the absolute via positions are difficult to determine, the relative distance between the power and ground vias in each pattern is identical because of the same package size.

At last, if the blind/buried vias are moved on the internal layers, the via patterns need to be adjusted accordingly based on the formulated patterns from the top or bottom layers.

This pattern formulation approach assumes that the power and ground vias in the IC region are alternately placed, as illustrated in Fig. 4(a). It is because the alternating via placement achieves lower parasitic via inductance than the grouped via placement [20], [21]. As a result, the magnetic flux is confined between the power via and its surrounding ground vias, so the coupling among the power vias can be neglected in practical PCB designs. The examples in Fig. 4 demonstrate the flexibility of our pattern-based method to handle the complicated PCB structures in mobile platforms. The localized via patterns serve as the fundamental units to calculate the parasitic via inductance and resistance for the entire PCB structure.

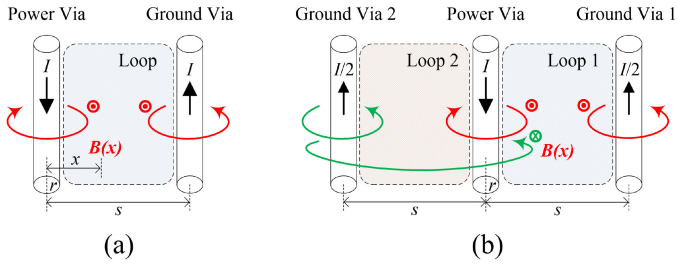


Fig. 5. Magnetic flux penetrating though the loop formed by adjacent vias. (a) One power and one ground via. (b) Two ground vias near one power via.

B. Pattern Calculation

One of the most critical parasitic elements in the PDN design is the via inductance. It is caused by the current-induced magnetic flux penetrating through the loop formed by the adjacent power and ground vias.

Fig. 5(a) shows a simple case that contains one power via carrying current I and one ground via with the same return current. h is the via length, s is the distance between these two vias, and r is the via radius. Since the power and ground vias are typically placed between paralleled planes, they can be regarded as relatively long straight wires based on the image theory (equivalent to the $h \gg r$ condition) [22]. From the Biot–Savart

law for this case, the total magnetic flux Φ can be calculated as

$$\Phi^{(a)} = 2\int_0^h \int_r^s B(x)dxdz = \frac{\mu I h}{\pi}\ln\left(\frac{s}{r}\right) \quad (1)$$

where B is the magnetic flux density, x is the distance to the power via, and μ is the magnetic permeability. Note that the current flowing on the power and ground vias equally contributes to the magnetic flux penetrating through the loop. The per-unit-length (PUL) inductance for this simple case is

$$L_{\text{pul}}^{(a)} = \frac{\Phi^{(a)}}{Ih} = \frac{\mu}{\pi}\ln\left(\frac{s}{r}\right). \quad (2)$$

For a more complicated case, the power via may be surrounded by multiple ground vias, as shown in Fig. 5(b). In loop 1, the induced magnetic flux of ground via 2 has an opposite direction from that of ground via 1 and power via. It implies that the presence of ground via 2 reduces the total magnetic flux in loop 1. With the same distance s to the power via, the return current is evenly distributed on the two ground vias ($I/2$ on each ground via). The total magnetic flux in loop 1 can be calculated as

$$\begin{aligned}\Phi_{\text{loop,1}}^{(b)} &= \frac{3}{2}\int_0^h\int_r^s B(x)dxdz - \frac{1}{2}\int_0^h\int_s^{2s} B(x)dxdz \\ &= \frac{\mu I h}{2\pi}\left[\frac{3}{2}\ln\left(\frac{s}{r}\right) - \frac{1}{2}\ln(2)\right]. \end{aligned} \quad (3)$$

Symmetrically, the total magnetic flux in loop 2 is equal to the total magnetic flux in loop 1: $\Phi_{\text{loop,2}}^{(b)} = \Phi_{\text{loop,1}}^{(b)}$. Then, the PUL inductance for this case is determined by the magnetic flux of these two paralleled loops

$$\begin{aligned} L_{\text{pul}}^{(b)} &= \frac{\Phi_{\text{loop,1}}^{(b)}}{\frac{1}{2}Ih}\Big|\Big|\frac{\Phi_{\text{loop,2}}^{(b)}}{\frac{1}{2}Ih} \\ &= \frac{\mu}{2\pi}\left[\frac{3}{2}\ln\left(\frac{s}{r}\right) - \frac{1}{2}\ln(2)\right]. \end{aligned} \quad (4)$$

The derivations of (2) and (4) demonstrate the fundamental principles to calculate the PUL inductance based on the two simple cases. However, a real PCB structure may contain more complicated patterns. Therefore, a generalized equation for PUL inductance calculation needs to be developed based on an arbitrary via pattern.

Suppose a via pattern has N ground vias and the via radius is r, as illustrated in Fig. 6. For each ground via i, where $i \in [1, N]$, its distance to the power via is s_i. To maintain the law of current conservation, the total returning current I is distributed among all the ground vias. The ground via with longer distance to the power via shares less current. Therefore, a current coefficient c_i is defined to represent the portion of the current flowing on ground via i, where $\sum_{i=1}^{N} c_i = 1$. From (2), the impedance to the ground via is proportional to the logarithm of its distance $\ln(s)$. Therefore, the current coefficient c_i is based on the inverse logarithmic relationship of the distance as

$$c_i = \frac{1}{\ln(s_i)\cdot\sum_{k=1}^{N}\frac{1}{\ln(s_k)}}. \quad (5)$$

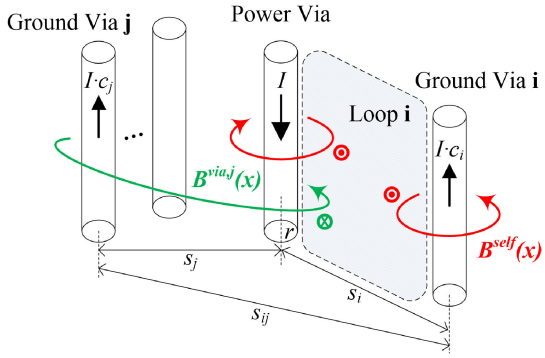


Fig. 6. Illustration of the magnetic flux for an arbitrary via pattern.

When the locations of ground vias are symmetrical (rotatable), c_i is exactly the true value. Otherwise, c_i becomes an approximated estimation.

Similar to (1), in the loop formed by ground via i and power via, the magnetic flux contributed by these two vias is

$$\begin{aligned}\Phi_{\text{loop,i}}^{\text{self}} &= (1+c_i)\int_0^h\int_r^{s_i} B^{\text{self}}(x)dxdz \\ &= \frac{\mu I h}{2\pi}\left[(1+c_i)\ln\left(\frac{s_i}{r}\right)\right]. \end{aligned} \quad (6)$$

The magnetic flux induced by other ground vias should also be considered. For a different ground via j, where $j \in [1, N]$ and $j \neq i$, its distances to the power via and ground via i are s_j and s_{ij}, respectively. The current coefficient of ground via j is c_j. The magnetic flux, induced by ground via j and penetrated through the loop formed by ground via i and power via, is calculated as the integral of magnetic flux density from s_{ij} to s_j

$$\begin{aligned}\Phi_{\text{loop,i}}^{\text{via,j}} &= c_j\int_0^h\int_{s_{ij}}^{s_j} B^{\text{via,}}j(x)dxdz \\ &= \frac{\mu I h}{2\pi}\left[c_j\ln\left(\frac{s_j}{s_{ij}}\right)\right]. \end{aligned} \quad (7)$$

Note that the sign of $\Phi_{\text{loop,i}}^{\text{via,j}}$ is determined by the ratio of s_j and s_{ij}, which implies that other ground via's impact on the total magnetic flux also depends on the relative positions of the vias.

Combining (6) and (7), the total magnetic flux in the loop formed by ground via i and power via is

$$\begin{aligned}\Phi_{\text{loop,i}} &= \Phi_{\text{loop,i}}^{\text{self}} + \sum_{j=1,j\neq i}^{N}\Phi_{\text{loop,i}}^{\text{via,j}} \\ &= \frac{\mu I h}{2\pi}\left[(1+c_i)\ln\left(\frac{s_i}{r}\right) + \sum_{j=1,j\neq i}^{N} c_j\ln\left(\frac{s_j}{s_{ij}}\right)\right]. \end{aligned} \quad (8)$$

Applying (8) to all the ground vias, the total magnetic flux in the N loops can be obtained, respectively. Following the same principle of (4), the PUL inductance for the generalized via pattern is calculated based on the magnetic flux of all the loops

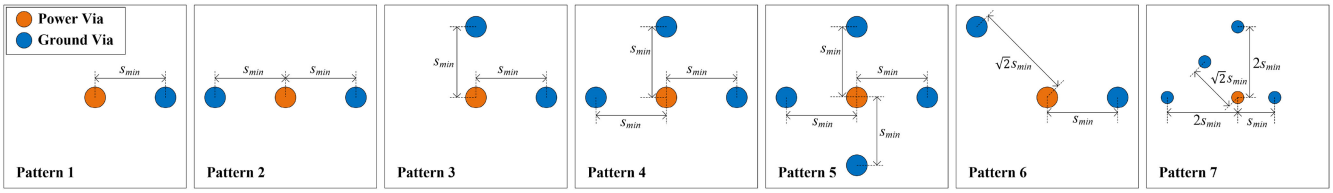


Fig. 7. Arbitrary via patterns for validation. The via diameter is 0.075 mm. The minimal via distance between power and ground vias is $s_{\min}$.

connected in parallel

$$L_{\text{pul}} = 1\Big/\left(\sum_{i=1}^{N}\frac{c_i I h}{\Phi_{\text{loop,i}}}\right) = \frac{\left(\frac{\mu}{2\pi}\right)}{\sum_{i=1}^{N}\frac{c_i}{(1+c_i)\ln\left(\frac{s_i}{r}\right)+\sum_{j=1,j\neq i}^{N}c_j\ln\left(\frac{s_j}{s_{ij}}\right)}}. \quad (9)$$

Another parasitic element is the via resistance, which has a secondary effect on the PDN impedance mainly at dc and the resonant frequencies. Depending on the frequency f, the skin depth is δ. For a standard-size via when the via radius $r \gg \delta$, the effective conduction area A_{eff} can be determined using a simplified equation: $A_{\text{eff}} = \pi[r^2 - (r-\delta)^2]$. However, the dimension of the microvia used in mobile platform PCB is comparable with the skin depth in the frequency range of interest (300 kHz–300 MHz). Hence, a more accurate method using the "truncated exponential decay" approach [23] is used to derive the modified skin depth δ' for the via resistance calculation

$$\delta' = \delta(1 - e^{-\frac{r}{\delta}}). \quad (10)$$

The asymptotically correct formula for the effective area is

$$A_{\text{eff}} = \pi[2r\delta' - \delta'^2]\cdot(1+y) \quad (11)$$

where $(1+y)$ is a divisor correction coefficient based on a modified Lorentzian function y. The fitted expression of y is also provided in [23]

$$y = \frac{0.19}{(1+0.27\cdot[z^{1.83}-z^{-0.99}]^2)^{1.09}}$$
$$z = 0.62\frac{r}{\delta}. \quad (12)$$

Finally, the PUL resistance for a single via is calculated as

$$R_{\text{pul}} = \frac{\rho}{A_{\text{eff}}} \quad (13)$$

where ρ is the resistivity of the conductor material.

C. Simulation Studies on Accuracy and Edge Effect

The pattern-based analytical equation (9) can be applied to an arbitrary via pattern. A commercial radio frequency simulation tool, ANSYS 2-D Extractor, was used to validate this equation for various via patterns and distances. As illustrated in Fig. 7, seven patterns were built in the simulation tool with different numbers and positions of the ground vias. The via diameter was 0.075 mm. The minimum via distance $s_{\min}$ was sweeping from 0.3 to 0.8 mm for all the patterns. These values were chosen based on the typical specification of the HDI PCB in mobile platforms. The simulated magnetic flux for each via pattern is shown in Fig. 8. It can be observed that the current distributions on each ground via are following the inverse relationship of the distance, as suggested by (5). The simulated PUL via inductance and the calculated PUL via inductance, obtained based on the proposed analytical equation, are compared in Fig. 9. Good correlations are observed for all the cases, where the largest difference between the calculated and simulated PUL inductances is 9.54 pH/mm (with a maximum discrepancy of 1.6%). It verifies the accuracy of our proposed analytical equation for an arbitrary via pattern. Equation (13) for the PUL via resistance is validated in Section IV-B.

Since the pattern is a 2-D structure, the vias are equivalently treated as relatively long wires during the calculation of the PUL parasitic elements. Therefore, the edge effect, such as the fringing fields at the end of the vias or the proximity to the plane edges, may affect the accuracy of our method. To investigate the impact of the edge effect, another 3-D electromagnetic field simulation tool, CST Studio, was used to simulate the via inductance of different lengths. "Pattern 1," "Pattern 5," and "Pattern 7" in Fig. 7 were evaluated to check the smallest, median, and largest PUL inductance cases, respectively. The minimum via distance $s_{\min}$ was fixed to 0.35 mm and the plane size was 2 mm by 2 mm. As shown in Fig. 10, the via length varied from 0.02 to 0.10 mm. The edge effect causes additional parasitic PUL inductance when the via length is smaller than 0.04 mm. For a mobile platform PCB, the typical dielectric thickness between layers is 0.045–0.060 mm. In other words, the error introduced by the edge effect is negligible in this application. The modeling of the edge effect is beyond the scope of this article.

III. PDN Modeling Methodology

With the assistance of this pattern-based analytical method, a practical modeling methodology is proposed to calculate the PDN impedance of the entire PCB. The flow diagram is depicted in Fig. 11. On the left side of this diagram, the "Via Pattern Database" indicates that the via patterns from the previous projects can be stored and adapted for future designs. It is not only useful to determine the impedance of a known PCB structure, but also helpful to improve the layout, especially in the predesign stage. The dashed arrow lines represent the interactions with this database. On the right side of this diagram, the main workflow is divided into four steps. The first three steps, including "(1) PCB division," "(2) pattern identification,"

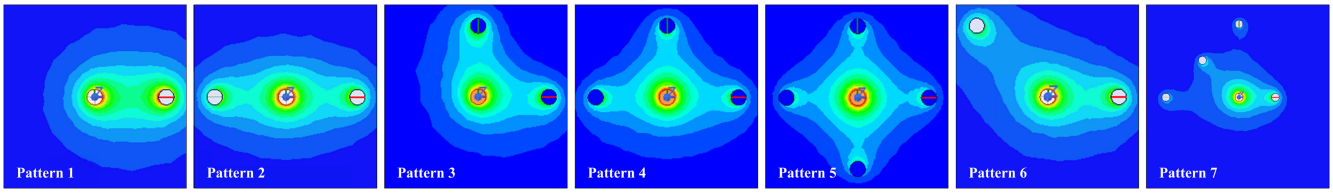


Fig. 8. Simulated magnetic flux for each via pattern, obtained using the ANSYS 2-D Extractor.

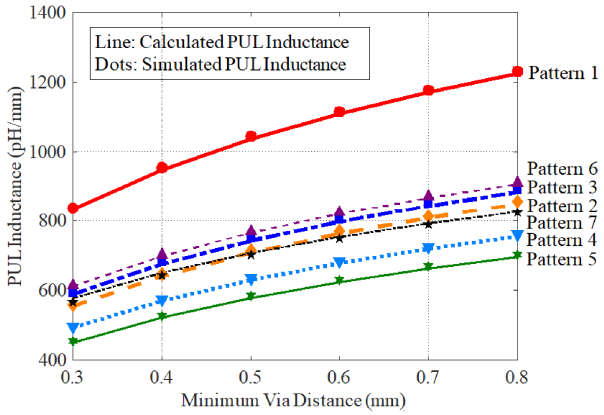


Fig. 9. Comparison between the simulated and calculated PUL via inductance for different via patterns and distances. The simulated results were obtained using the ANSYS 2-D Extractor. The calculated results were obtained based on the proposed analytical equation.

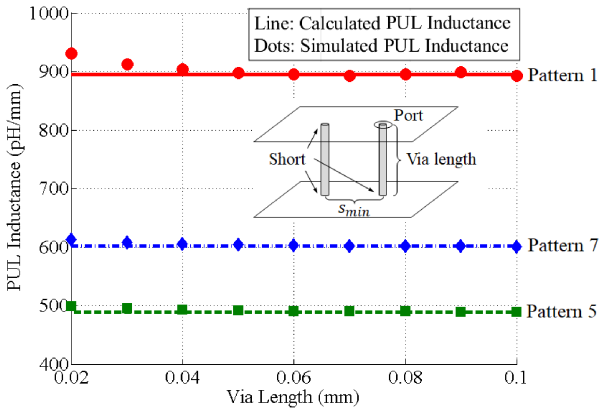


Fig. 10. Simulation results for the via inductance with different via lengths using the CST Studio. A port was added to the power via; the ground via(s) were shorted to provide a return path for the injected current. The minimum via distance $s_{\min}$ was fixed to 0.35 mm.

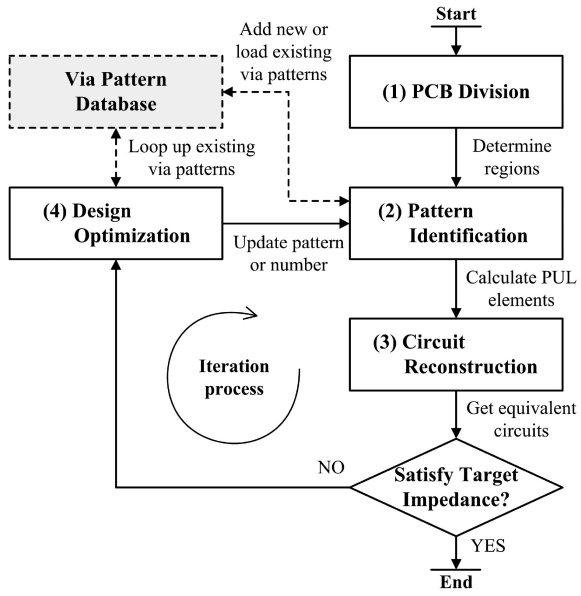


Fig. 11. Flow diagram of the modeling methodology.

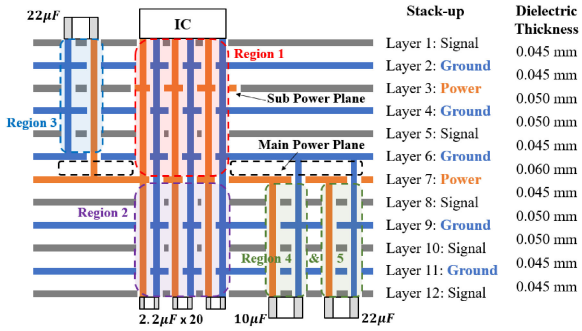


Fig. 12. Physical geometry and region division of the mobile phone PCB under investigation.

and "(3) circuit reconstruction," construct an equivalent circuit with one-to-one correspondences to the PCB physical geometry. Then, the PDN impedance can be obtained from the circuit simulations. If the target impedance is not satisfied for the initial design, an iteration process is conducted to further improve the impedance in the "(4) design optimization" step.

Following the modeling methodology, a real mobile phone PCB, illustrated in Fig. 12, is investigated as an example. Among the total 12 layers, the seventh layer is the main power plane connecting all the decoupling capacitors and IC, and the third layer is the subpower plane to unify the voltage under the IC. The ground planes are located on the second, fourth, sixth, ninth, and eleventh layers. The copper thickness is 0.023 mm for the top and bottom layers and 0.018 mm for all the internal layers. There are 0402 package (22 μF, 10 μF) and 0201 package (2.2 μF) decoupling capacitors placed on both the top and bottom layers. All of the 0201 package capacitors are placed directly under the IC, while the other 0402 package capacitors are placed besides the IC due to the space limitation.

A. PCB Division

Seen at the input port of the load IC, the current in the PDN is always flowing along the power vias from the decoupling

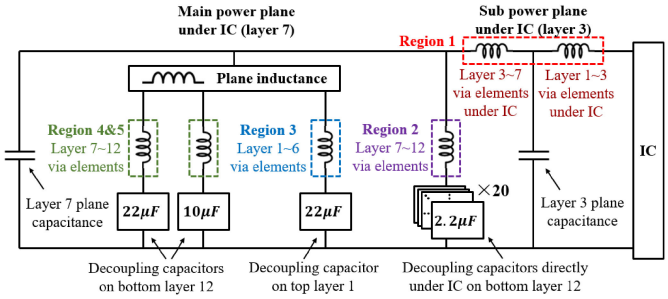


Fig. 13. Equivalent circuit corresponding to the PCB under investigation.

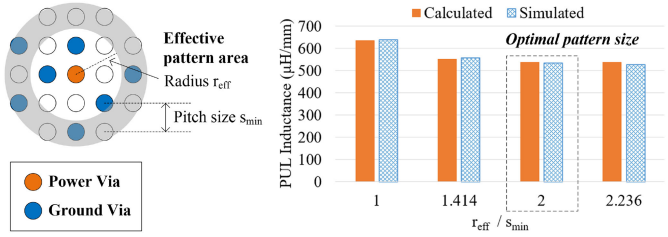


Fig. 14. Selection of the optimal pattern size.

capacitors and returning along the nearby ground vias. By tracing the current flow path, the multilayered PCB structure can be divided vertically into different regions between the main power plane and the ground plane. For the target PCB in Fig. 12, there are five regions associated with the physical geometry. "Region 1" and "Region 2" correspond to the vias directly under the IC from the top and bottom layers to the main power plane, respectively. "Region 2" also connects to the multiple 2.2-μF decoupling capacitors on the bottom layer. "Region 3," "Region 4," and "Region 5" correspond to the vias between the 0402 package decoupling capacitors and the main power plane. Since these capacitors are located besides the IC, we should include the plane inductance to reflect the current distribution on the main power plane. The mutual inductance among different regions is negligible because the distance between regions is relatively larger than the distance from the power via to the nearby ground vias [24]. Within each region, the parasitic elements of the vias can be merged into the equivalent inductance and resistance. The equivalent circuit of the entire PCB structure is depicted in Fig. 13.

B. Pattern Identification

The pattern formulations for the IC and decoupling capacitor vias are introduced in Section II. Accordingly, the patterns in "Region 1" are identified based on the IC pinout, and the patterns in other regions are identified based on the packages of the decoupling capacitors. Furthermore, an optimal pattern size needs to be selected for practical purposes. It is because a larger pattern includes more nearby ground vias, which leads to a more accurate result but also increases the complexity in pattern formulation. For the IC region shown in Fig. 14, the pitch size $s_{\min}$ is fixed to 0.35 mm and the radius of the effective pattern area r_{eff} is investigated using 1, $\sqrt{2}$, 2, and $\sqrt{5}$ times

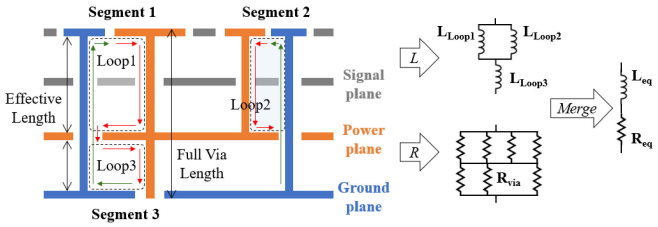


Fig. 15. Calculation of the equivalent inductance and resistance in one region.

$s_{\min}$. When $r_{\text{eff}} = s_{\min}$, only two ground vias are included in this pattern, but it yields a falsely high PUL via inductance of 635 μH/mm. By increasing r_{eff}, the PUL via inductance converges to 537 μH/mm. The optimal pattern size is achieved when $r_{\text{eff}} = 2s_{\min}$ as it provides an accurate result with the simplest structure. This experimental-based conclusion can be verified using other via patterns. Therefore, it is suggested to include the ground vias whose relative distance is within two pitch sizes into the pattern.

C. Circuit Reconstruction

This step aims to determine all the components of the equivalent circuit in Fig. 13. The PUL via inductance and resistance of the identified patterns can be calculated based on the analytical equations (9) and (13). Then, the inductance of a via segment is obtained by multiplying the PUL inductance by the effective length of this segment, and the resistance is obtained by multiplying the PUL resistance by the full segment length. Compared with the full length, the effective length excludes the layer thickness of the power and ground planes. It is because the inductance is related to the loop formed by the adjacent vias. The signal planes can also be ignored since they do not affect the impedance of the power nets. As illustrated in Fig. 15, the inductance and resistance of multiple segments in the same region can be merged depending on their series or parallel relationship. As a result, one equivalent inductance and one resistance are generated to represent the parasitic elements for each region.

The plane capacitance is insignificant for the mobile phone PCB because of the limited layout space, so the simple parallel-plate capacitor equation is sufficient to estimate the plane capacitance

$$C_{\text{plane}} = \frac{\varepsilon A}{d} \tag{14}$$

where ε is the dielectric permittivity, A is the plane area, and d is the dielectric thickness between the plane pair. The total inductance between the main power plane pair ("Plane inductance" in Fig. 13) is obtained based on the cavity model [15]–[18]. By merging the vias of the same region, the cavity model can be simplified by setting one port located at the center of each region instead of identifying the absolute positions for all the vias. At last, "Region 2," "Region 3," "Region 4," and "Region 5" connect to the decoupling capacitors on the top and bottom layers. For high accuracy, the SPICE model of the decoupling capacitor is employed in the circuit simulation since it includes both the

parasitics, such as the equivalent series inductance/resistance and the derating effects. Similar to the via inductance and resistance, the decoupling capacitors in the same region are in parallel and can be merged together.

D. Design Optimization

With the constructed equivalent circuit, the PDN impedance can be assessed by the circuit simulations. If the target impedance is not satisfied, an iteration process is conducted to further optimize the PDN design. The divided regions are helpful to identify the most critical component contributing to the total impedance. A common optimization method is to apply more decoupling capacitors, which can be easily implemented as increasing the number of the decoupling capacitor via pattern in our modeling methodology. Adding more ground vias is another feasible solution to reduce the parasitic via inductance, which is equivalent to changing the via pattern in design. The proposed pattern-based analytical equation is capable of predicting the PUL via inductance accurately, in order to provide quantitative guidance for the system designer. For instance, Fig. 9 shows the PUL inductance with different via distances of the seven patterns in Fig. 7. According to the calculated results, the designer is able to achieve lower impedance level with better utilization of the layout space for the new design. Therefore, our modeling methodology is especially useful in the predesign stage when the PCB layout is not fully completed.

IV. Validation

The PDN impedance of the mobile phone PCB in Fig. 12 was measured to validate our modeling methodology. The shunt-thru method was used to achieve the accurate $m\Omega$ impedance measurement [25], as depicted in Fig. 16. By landing the two microprobes (PacketMicro GR201504) between the IC's power and ground pads, the transmission coefficient S_{21} was measured by the vector network analyzer (Keysight E5061B). Then, the impedance of the entire PCB structure can be derived from the measured S-parameter: $Z_{\text{PDN}} = 25 \cdot S_{21}/(1 - S_{21})$. To avoid the mutual coupling between the microprobes, the landing locations were separated at the opposite sides of the IC pinout. Full two-port calibration and port extension were applied to move the reference planes to the microprobe tips. Ferrite cores were attached to the test cable to eliminate the measurement error caused by the cable ground loop [26]. To include the derating effects of the decoupling capacitors, 0.75-V dc bias voltage was enabled in the vector network analyzer. The frequency range in this measurement was from 300 kHz to 300 MHz.

The layout of this mobile phone PCB was also imported into a board-level electromagnetic field solver, Cadence Sigrity PowerSI. In addition to the total PDN impedance, the parasitic inductance and resistance of each region were simulated by manually setting the ports at different locations and layers. As a result, the accuracy of our modeling methodology can be validated by both whole structure and region-by-region comparisons.

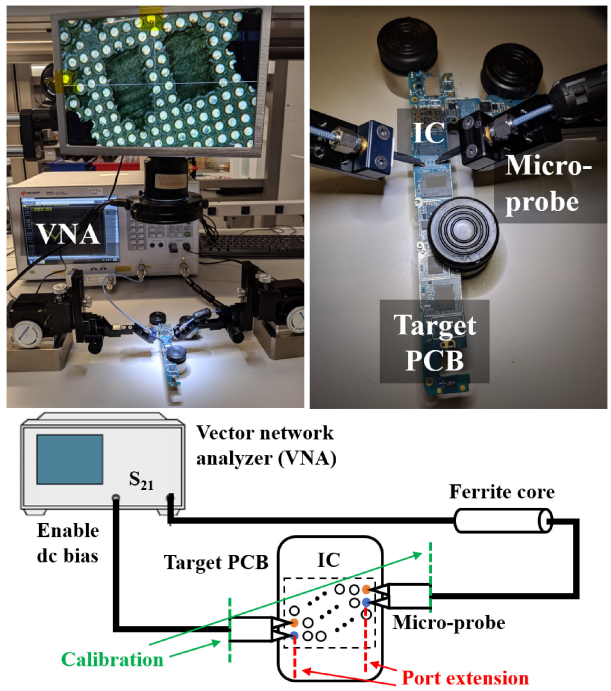


Fig. 16. Photograph and diagram of the shunt-thru measurement setup.

A. Whole Structure Comparison

The impedance for the whole structure is contributed by all the components embedded in the PCB. However, different components have dominant effects at different frequencies. For example, capacitance usually dominates at a lower frequency, and the via inductance is typically critical at a higher frequency. Therefore, it is desired to achieve good correlations with the simulations and measurements for the entire frequency range.

The calculated result based on our modeling methodology was using one lumped port grouping all the IC vias on the top layer. However, it is unrealistic to implement this lumped port in the measurement setup. As discussed above, the measured result was converted from the two-port S-parameter, which resulted in lower IC via inductance and caused lower impedance at higher frequencies. Therefore, the calculated and measured results could not be compared directly. To solve this issue, two simulated results obtained using the Cadence Sigrity PowerSI were added with the lumped port and two-port configurations, respectively. Then, the four types of results could be divided into two groups: the lumped port group including the calculated and simulated results, and the two-port group including the simulated and measured results.

Two criteria are evaluated to validate our modeling method: the resonant frequencies and the magnitude of the PDN impedance. As shown in Fig. 17, the impedance curves in the same configuration group agree well with each other. The three resonant frequencies, located at 1.5, 2.0, and 5.5 MHz, are all accurately captured with less than 100 kHz difference. The maximum variations of the impedance magnitude are within 0.26 and 0.33 mΩ for the lumped and two-port configurations, respectively. Between the two groups, we can indirectly compare

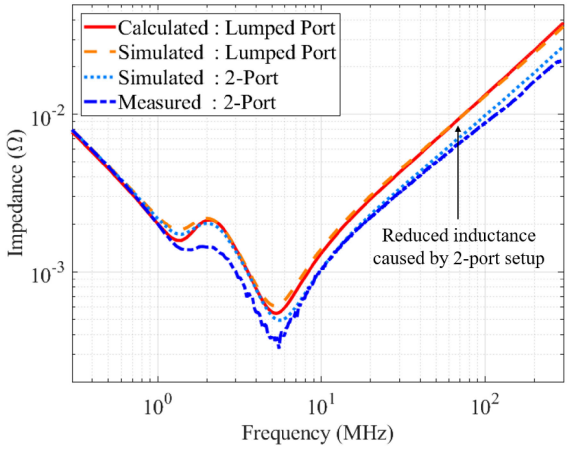


Fig. 17. Comparison of the PDN impedance for the whole PCB structure. The calculated results were obtained based on the proposed analytical equations, the simulated results were obtained using the Cadence Sigrity PowerSI, and the measured results were obtained from the shunt-thru measurement on the mobile phone PCB.

TABLE I
REGION-BY-REGION COMPARISON OF THE PARASITIC ELEMENTS

Location	Parasitic	Calculation	Simulation
Region 1	Inductance	2.10 pH	2.39 pH
Layer 1∼3	Resistance	0.05 mΩ	0.06 mΩ
Region 1	Inductance	4.81 pH	5.48 pH
Layer 3∼7	Resistance	0.14 mΩ	0.14 mΩ
Region 2	Inductance	13.51 pH	12.93 pH
Layer 7∼12	Resistance	0.20 mΩ	0.19 mΩ
Region 3	Inductance	289 pH	285 pH
Layer 1∼6	Resistance	2.95 mΩ	4.10 mΩ
Region 4	Inductance	312 pH	312 pH
Layer 7∼12	Resistance	3.62 mΩ	4.00 mΩ
Region 5	Inductance	242 pH	240 pH
Layer 7∼12	Resistance	3.62 mΩ	4.00 mΩ

the calculated and measured results with respect to the difference of the two simulated impedance. The good correlations across the entire frequency range validate the accuracy of our modeling methodology for the whole PCB structure.

B. Region-by-Region Comparison

Since the proposed modeling methodology is built on the basis of the divided regions, it is important to validate the equivalent inductance and resistance for each region. The calculated and simulated parasitic elements for different regions are compared in Table I. "Region 1" is split into two parts because of the subpower plane on layer 3. Other regions have only one set of equivalent inductance and resistance. The via resistance are obtained at the 6-MHz resonant frequency.

The error between the calculated and simulated parasitic inductance is within 12.2% for the IC vias and within 1.4% for the decoupling capacitor vias. The good agreement shows that this methodology can not only estimate the via inductance accurately, but also identify the critical components contributing to the total PDN impedance. The calculated parasitic resistance generally correlates well with the simulated results (with a discrepancy of 9.5%), except for "Region 3" (with a discrepancy of 28.0%). It is because there are multiple paralleled vias laid closely in the same pad of the decoupling capacitor in this region. Thus, the increased proximity effect causes higher ac resistance. However, the impedance curve is not significantly affected since the via resistance has a secondary impact mainly at dc and the resonant frequencies. Therefore, the current accuracy level for the resistance calculation is acceptable. The proximity effect modeling is not the focus of this article and will be discussed in future studies.

V. CONCLUSION

In this article, the limitations of the existing PDN modeling methods are discussed with the focus on mobile platform applications. To overcome these issues, a novel pattern-based analytical method is proposed for the impedance calculation. By utilizing the relative relationships between the adjacent vias, the localized via patterns are formulated based on the physical geometry. Then, the parastic via inductance and resistance are analytically derived for arbitrary via patterns. It can be shown that our method has better flexibility to handle the complicated PCB structure in mobile platforms. In addition, a practical modeling methodology is developed to model and guide the PDN design. With the capability of accurate and layout-free impedance estimation, this methodology is especially useful for the predesign stage to accelerate the development process. Finally, the proposed analytical equations and the modeling methodology have been extensively validated by the measurements and simulations on a real mobile phone PCB. Good agreements can be observed from both whole structure and region-by-region comparisons.

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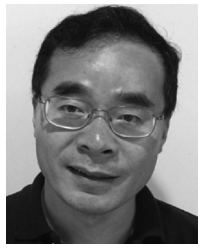

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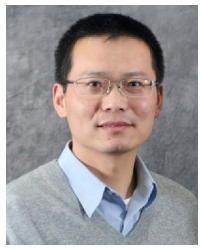

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