Accurate Inductance Models of Mounted Two-Terminal Decoupling Capacitors

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***Abstract*—The inductance associated with a decoupling capacitor is typically represented with a constant equivalent series inductance (ESL). In reality, this inductance depends on how the capacitor is mounted and on coupling to closely located structures, including the traces and vias connecting the capacitor to the power and return planes. Here, a method is proposed to quickly and accurately compute the inductance associated with decoupling capacitors and their connections to the power planes. We call this equivalent inductance $L_{above,decap}$. It is calculated by partitioning the geometry into sub-models for the connections to the power and return planes and for the mounted capacitor and pads. The accuracy of the partitioning approach is demonstrated in simulation and experiments using two common decoupling capacitor layouts. Simulations are performed using the finite element method (FEM) and the partial element equivalent circuit (PEEC) method. The partitioning approach estimates the overall inductance associated with the decoupling capacitor and its connections to the power bus within 16% if the distance between the capacitor and reference plane (dielectric thickness) is not more than 6 mils. A simplified PEEC model was further developed which allows a user to estimate the inductance associated with the capacitor using closed-form expressions. This simplified model estimates the capacitor's inductance within 14% of the results found using FEM. The models presented in this work should help both the power distribution network tool designer as well as the design engineer to obtain more accurate inductance estimates than is possible using the manufacturer's ESL value.**

***Index Terms*—Computational electromagnetics, inductance, multi-layer ceramic capacitor, power distribution network, partitioning, partial equivalent element circuit (PEEC) method, passive component modeling, signal and power integrity (SiPi).**

I. Introduction

DECOUPLING capacitors (decaps) are a major contributor to the power distribution network (PDN) impedance [1], [2]. Decoupling capacitors are used to reduce voltage ripples caused by simultaneous switching noise. Careful selection of the decoupling capacitor's value, package size, quantity and placement – as well as their connection inductance to the power and return planes – are critical for power integrity [3]. Noise in the power supply may also cause electromagnetic interference issues [4], [5]. The impedance of these capacitors is usually represented as an equivalent circuit consisting of an equivalent series capacitance (ESC), equivalent series inductance (ESL), and equivalent series resistance (ESR) [6], [7], as a distributed circuit [8], [9], or as an S-parameter block [10], [11]. However, these models often do not include the parasitic interactions between the capacitor and surrounding structures, including its mounting pads, the reference plane, and the traces and the vias connecting the capacitor to the power bus [12]. ESR and ESC values given by the manufacturer are typically correct within the specified tolerance [6], [13], but the actual inductance of the mounted capacitor can be much different than would be calculated using the ESL alone [14]. The equivalent inductance depends on the distance to the reference plane and the capacitor's inner electrode architecture [14], [15]. Hence, accurately modeling the inductance associated with decoupling capacitors can be critical to the design of the power delivery network (PDN). Unfortunately, it is often not practical to estimate the inductance of the capacitor and its connections to the PDN using computational electromagnetics (CEM) tools [16]–[18], considering the many connection configurations that are possible for the large number of decoupling capacitors that are often used in a design. However, estimations of these inductances can be made with the partial equivalent element circuit (PEEC) method using a simple representation of the decoupling capacitor [19], [20]. PEEC allows representation of electromagnetic parasitics with electrical circuit elements whose values can be calculated using closed-form expressions.

The PDN impedance is a combination of two impedances which are found to be independent from each other. Those two impedances are: the impedance of the capacitor(s) with the layout above the top return plan (pad, trace, via), and the impedance between a noise source on the IC and its connection to the power in return planes [21]. In this work, a method is proposed to estimate the inductance associated with decoupling capacitors by partitioning the total inductance into two sub-models: one for the capacitor and mounting pads, and one for the traces and

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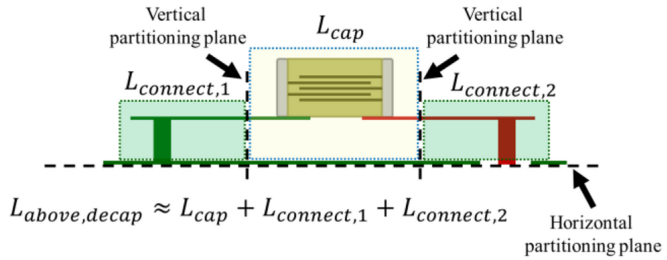


Fig. 1. Total inductance associated with a decoupling capacitor, $L_{above,decap}$, can be partitioned into a portion associated with the capacitor and mounting pads, L_{cap}, and a portion associated with the connecting traces and vias, $L_{connect}$.

vias connecting the capacitor to the power and return plane. The inductance associated with these sub-models can be found independent of one another or the rest of the PDN. Partitioning allows the inductance associated with the mounted capacitor to be established before designing the overall PDN circuit details, and allows to calculate the inductance associated with a wide variety of connections to the power and return planes separately.

The partitioning approach will be discussed in detail in this article. Two PEEC models will be presented, one of which is complex and requires numerical solution and one of which is simplified and can be solved using closed-form expressions. The internal geometrical structure of a number of commercial capacitors are analyzed in Section III, to account for variation in internal structures of the capacitors while estimating inductance. Results are presented in section IV, where estimates of the inductance of the mounted capacitor, pads, and the reference plane are measurements. Discussions and conclusions are summarized in Section V.

II. Partitioning Approach

Partitioning is used to simplify and speedup the modeling of decoupling capacitors for practical PDNs. A PDN may include hundreds of decoupling capacitors where exact modeling of all parts requires large compute times [17]. Conventional approaches do not lead to efficient solutions of the problem. The proposed method is based on horizontal and vertical partitioning planes as shown in Fig. 1. The metal plane under the capacitor in Fig. 1 is usually a ground plane. This horizontal metal plane is a good place for splitting the model of the capacitor from the rest of the PDN [3], [20], [22]. More specifically, the capacitor is typically partitioned from the rest of the PDN at the location where the power via transitions through the antipad in the ground plane. The ground plane isolates the mounted capacitor from the rest of the PDN layers, since there is minimal opportunity to couple energy through the ground plane or the via antipad. We will use this horizontal plane partition in all our models.

Here we will also use a second vertical partition for the contact connections as shown in Fig. 1 to separate the calculation of the inductance associated with the capacitor from the inductance associated with the connections to the power and return planes. The inductance associated with the connections between the capacitor and the power and ground planes will be represented by an inductance we call $L_{connect}$. The inductance associated

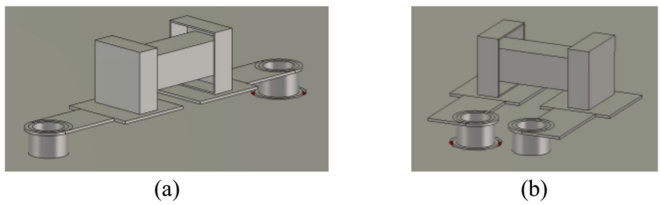


Fig. 2. Models of 100 nF 0603 capacitor mounted. (a) Straight. (b) L-shaped layout.

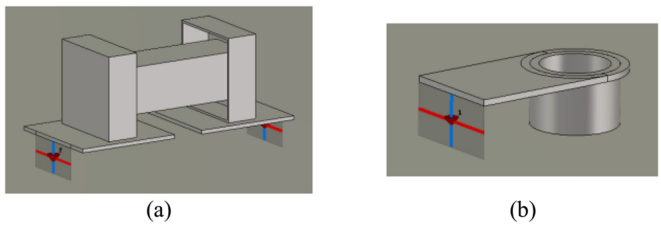


Fig. 3. Straight layout shown in Fig. 2(a) was partitioned into models. (a) L_{cap}, representing the pads, capacitor, and reference plane. (b) $L_{connect1}$, representing the connecting trace and via, and the reference plane.

with the capacitor, including the strong inductive coupling to the metal plane beneath it and its local environment, will be represented with L_{cap}.

Partitioning leads to two separate parts for the connections, $L_{connect} = L_{connect,1} + L_{connect,2}$, and for the capacitor, L_{cap}, which are weakly coupled to each other. The partition between $L_{connect}$ and L_{cap} is located sufficiently far away from the capacitor such that only weak couplings are interrupted by the partitioning cuts. We later present a more complicated model that better accounts for this coupling. For this simple partitioning, the inductance of the overall capacitor structure, $L_{above,decap}$, can be computed separately as

$$L_{above,decap} = L_{connect} + L_{cap} + err \tag{1}$$

where err is the error due to the simple partitioning approach. A key advantage of this partitioning approach is that the L_{cap} inductance can be the same for a large number of capacitors in a PDN if the same decoupling capacitor type is used. In this case, the modeling of all capacitors is much simpler for a large PDN with many capacitors than if the capacitor must be modeled over and over. More details will be given below.

A. Vertical Plane Partitioning of the Connection Between L_{cap} and $L_{connect}$

Capacitors may be connected to the PDN through a variety of connection layouts. A few of the more common layouts and their inductance are shown in Fig. 2 [23]. Layouts studied in this article are referred to as the "straight" and "L-shaped" layouts.

As shown in Fig. 1, the partitioning approach separates the inductance $L_{connect}$ from the inductance L_{cap}. This partitioning allows the user to quickly estimate the overall inductance, $L_{above,decap}$, for a number of layout configurations. To illustrate this flexibility, we consider two simple cases where the connections are to the sides as well as to the front as shown in Fig. 2. Figs. 3 and 4 show these layouts partitioned into structures

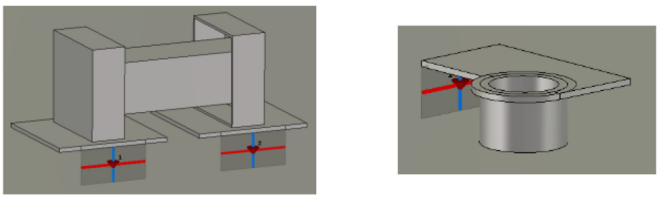


Fig. 4. L-shaped layout shown in Fig. 2(b) was partitioned into models. (a) L_{cap}, representing the pads, capacitor, and reference plane. (b) $L_{connect1}$, representing the connecting trace and via, and the reference plane.

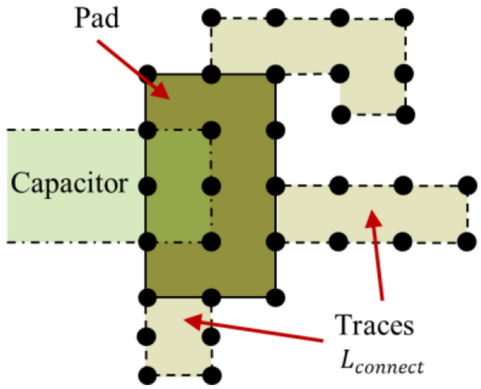


Fig. 5. Top view of pad with a variety of connections to traces.

for $L_{connect}$ and L_{cap}. The vertical lumped ports (highlighted with red and blue lines) in these figures were used to enable calculation of $L_{connect}$ and L_{cap} within the Dassault Systèmes CST Studio Suite solver [24] (CST). Input impedances at the lumped port locations were obtained using CST's finite element method (FEM) solver. Inductances were calculated from input impedance values. For PEEC, we used two different models. In the simple model, we ignored the partial mutual inductances which couple $L_{connect}$ and L_{cap}. This, of course, leads to relatively small errors and simpler, independent computations. The coupling between the sub-models for the capacitor and the traces is small unless the dielectric layer upon which the contacts are placed is far away from the ground plane. The accuracy of this approach will be shown in Section IV.

B. Improved Model for Connections Including Coupling

The partitioning approach presented in the last subsection leaves out the inductive couplings between L_{cap} and $L_{connect}$. In this section, we give an alternative approach where we show how the missing partial mutual inductances can be included to eliminate the coupling error in (1).

As shown in Fig. 3 and Fig. 4, the partition between L_{cap} and $L_{connect}$ is made at predetermined locations close to the capacitor. Fig. 5 shows a top view of these connections, where three different connections to the L_{cap} partition are shown. In this case, we assume that only a single L_{cap} model is needed for a given capacitor package size where the L_{cap} pads of the capacitor have enough PEEC nodes to connect all possible trace configurations. In the example in Fig. 5, we chose to show only 15 nodes for the L_{cap} pad part where six of the outside nodes

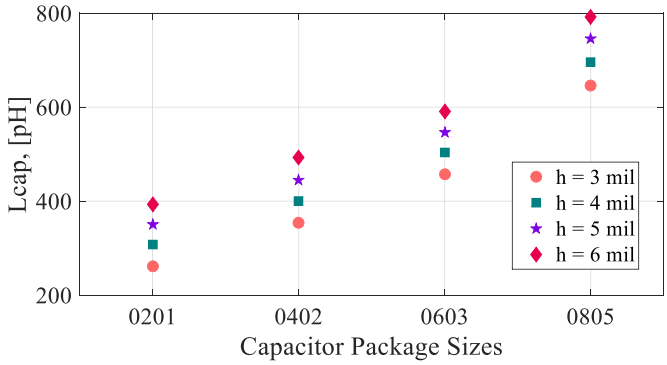


Fig. 6. Inductance associated with the capacitor as function of the distance between capacitor body and the reference plane. Values are given for typical package sizes.

are used for possible connections. Of course, all the connections and the capacitor base are located over the horizontal ground plane. In this case, the inductance $L_{above,decap}$ is calculated numerically for each configuration without partitioning L_{cap} and $L_{connect}$. This will clearly lead to a more complicated model, but the model for the multiple connections can be used multiple times to avoid the construction of multiple models for L_{cap}. To eliminate the coupling error, partial mutual inductances between the L_{cap} model and the connect PEEC models in Fig. 5 must be included. The rapid decay of the coupling inductance is well known [25], which minimizes the number of partial mutual inductances needed.

III. Modeling of the Capacitor Part, L_{CAP}

The value for ESL given by the manufacturer [26] does not account for the distance between the capacitor and the return plane. Fig. 6 shows the value of L_{cap} for conventional capacitor types for different distances to the return plane. As shown in this figure, capacitor mounting can significantly change L_{cap}. The following section shows the development of a highly simplified model for L_{cap} and a more complex model, which includes the internal plates of the capacitor among other features.

A. Simple PEEC Model for L_{cap}

We first consider a PEEC model for the simplest case, as shown in Fig. 7(a), which is an orthogonal Manhattan type model with only a few partial inductances. Each structure in Fig. 7(a) is represented as a single rectangular sheet with zero thickness or with a rectangular bar. The FEM waveguide port surfaces are also included in this model. Fig. 7(a) and (b) show a PEEC equivalent circuit for the capacitor and its image in the ground plane. Because of the influence of the capacitor and its image, the solution for the equivalent circuit will result in two times L_{cap} unless the symmetry is included in the PEEC model.

Equations for the inductances shown in Fig. 7 are given in [19], in which structures are represented using conductive sheets. Using equations from [19] and the models in Fig. 7, one can estimate values for L_{cap} from closed-form expressions. This capability has the advantage that one can estimate inductance

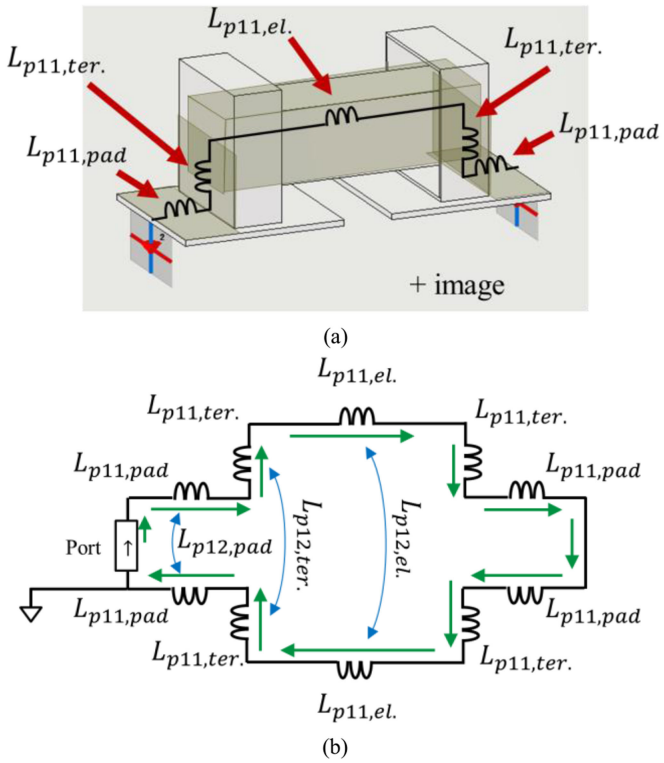


Fig. 7. Simplified PEEC-based model of L_{cap}. (a) Structures and elements associated with the model. (b) Equivalent circuit model.

without sophisticated modeling tools, for example, using MATLAB, and that the simple form of the model can give intuitive insight into the primary mechanisms that lead to a particular value for L_{cap}. A more accurate model results with refined meshing and if all the partial mutual inductances between all parts of the model are included. Example results for this simple model are shown in Section IV.

B. Detailed PEEC Model for L_{cap}

Fig. 7(a) and (b) represent a very simple equivalent circuit for the capacitor inductance. Even more sophisticated capacitor PEEC models include only a moderate number of nodes. Here, we suggest a somewhat more complex model where the cell structure is shown in Fig. 8. In fact, it is similar to the one used in [20] for a multi-terminal capacitor model. In Section IV.C, we show that the current flow in the capacitor body can be approximated by a PEEC block meshed uniformly as is indicated in Fig. 8. It is clear that this results in a major speed-up also for the FEM model. In general, the evaluation of the partial inductances takes a small fraction of a second. Even a 3D PEEC model for the capacitor does not result in many partial elements and can be computed in less than a second such that PDN models with a few hundred capacitors can be evaluated in minutes using the partitioning approach, even if the connect parts are different for most of the capacitors.

Fig. 8 shows the cells for the meshing of the L_{cap} part which shows an image to take the important ground-plane into account. The horizontal contacts at the end of the L_{cap} model pads are

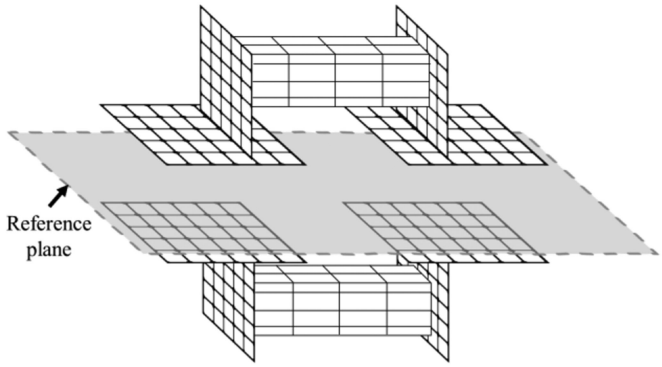


Fig. 8. Cells of the mesh to compute the mounted capacitor over a reference plane, where the reference plane was replaced with an image of the capacitor.

meshed such that $L_{connect}$ models can be applied as shown in Fig. 5. The geometrical dimensions are easily found for the external parts of the capacitor. Depending on the desired accuracy the vertical parts of the PEEC model can be modeled more accurately. However, all models in this article in Section IV used the relatively simple geometries.

The electrical PEEC modeling for the structure corresponding to Fig. 8 can be analyzed with a simple modified nodal analysis (MNA) circuit model [27]. A few observations are due to the special aspects of this model. The image cells are exact images of the PEEC model part. Thus, many partial self and mutual inductances are calculated only once. Mutual inductances between source and image cells are added to the MNA model as well. Similar to the Plane-Pair PEEC (PPP) modeling approach [19], [25], the symmetry can be used to reduce the number of variables. We observe that the voltages for the model and the image are equal and opposite resulting in half the voltages. The same is true for currents in the corresponding elements. The ground or zero volts must be at the plane in the middle shown in Fig. 8 similar to the PPP method [19].

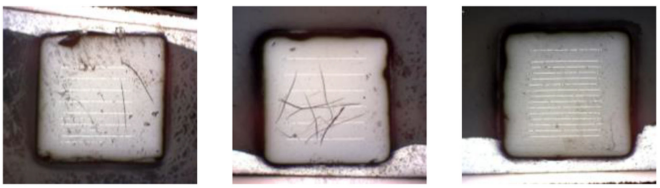
We can observe from Fig. 7(b) that while the image current is opposite in the x, y plane cells, it is in the same direction in the vertical z-directed cells for both the model and its image. While the current is the same as in the conventional model, the image model results in twice the voltage such that the inductance is

$$L_{cap} = \frac{V_p}{2I_p} \tag{2}$$

where V_p is a port voltage, I_p is a port current. Of course, the $L_{connect}$ results in very similar simple PEEC models as the L_{cap} model. For this reason, we do not consider the $L_{connect}$ modeling separately [19].

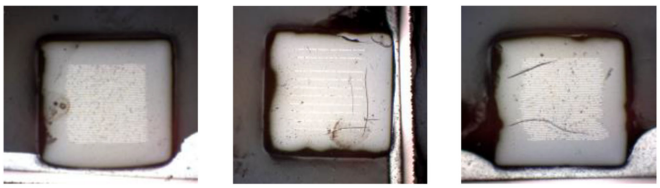
C. Geometry of the Capacitor Plate Part

The capacitor model shown in Fig. 8 was further extended using knowledge of the capacitor's internal architecture [28]. The internal geometry of several standard capacitors was studied. The decoupling capacitor package sizes are coded as 0201, 0402, 0603, and 0805, which represent the length and width of the component in hundredths of inches. Capacitors with values of 22 μF, 100 nF, and 1 nF and of type 0201, 0402, 0603,



(a) (b) (c)

Fig. 9. Cross-section of three 0603 capacitors with 1 nF nominal capacitance produced. (a) Manufacturer A. (b) Manufacturer B. (c) Manufacturer C.



(a) (b) (c)

Fig. 10. Cross-sections of three 0603 capacitors with 100 nF nominal capacitance produced. (a) Manufacturer A. (b) Manufacturer B. (c) Manufacturer C.

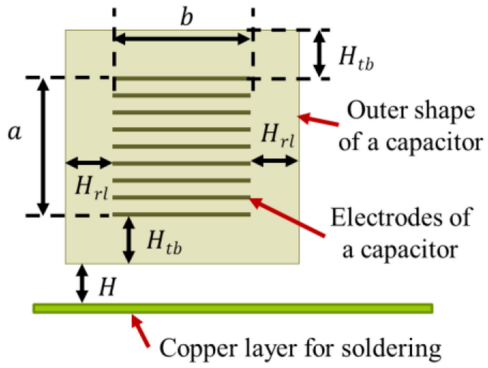


Fig. 11. Dimensions of each capacitor's internal architecture were measured under a microscope.

TABLE I
22 μF 0805 CAPACITOR INTERNAL GEOMETRY

	a [mil]	b [mil]	H_{tb} [mil]	H_{rl} [mil]	H [mil]
Minimum	38	27	1.6	3.5	1
Average	41	35	3	3.7	2
Maximum	44	44	4.5	4	4

TABLE II
1 NF 0603 CAPACITOR INTERNAL GEOMETRY

	a [mil]	b [mil]	H_{tb} [mil]	H_{rl} [mil]	H [mil]
Minimum	16	13	4.8	4	1
Average	18	18	6	6	2
Maximum	20	20	7.7	12	4

and 0805 sizes were considered because they are commonly used in PDN designs. To measure the internal dimensions of these capacitors, the capacitors were cut and viewed under a microscope. Cross-sections of two 0603 capacitors with values of 1 and 100 nF are shown in Fig. 9 and Fig. 10, respectively. The dimensions measured, besides the capacitor length, are shown in Fig. 11 and their values are shown in Tables I–V. The tables show the average, minimum and maximum dimensions from

TABLE III
100 NF 0603 CAPACITOR INTERNAL GEOMETRY

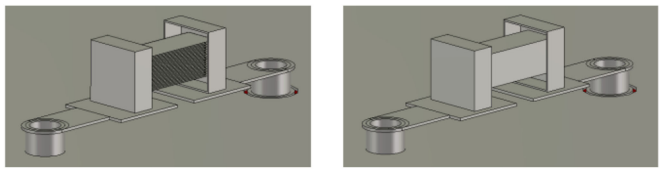
	a [mil]	b [mil]	H_{tb} [mil]	H_{rl} [mil]	H [mil]
Minimum	17.6	17.6	2.3	4.1	1
Average	19	19	5	5	2
Maximum	25	25	6.3	7	4

TABLE IV
100 NF 0402 CAPACITOR INTERNAL GEOMETRY

	a [mil]	b [mil]	H_{tb} [mil]	H_{rl} [mil]	H [mil]
Minimum	13.8	7.7	2.4	3.5	1
Average	13	11	3.5	4.5	2
Maximum	9.7	11.1	4.4	6.2	4

TABLE V
1 NF 0201 CAPACITOR INTERNAL GEOMETRY

	a [mil]	b [mil]	H_{tb} [mil]	H_{rl} [mil]	H [mil]
Average	12.6	10	3	3.5	2



(a) (b)

Fig. 12. (a) Simulation models of a detailed capacitor with 54 electrode plates. (b) Approximated capacitor where the plates are replaced with a solid PEEC conductive block.

capacitors of the same size and capacitance from five different manufacturers. Further, the results show that there are significant differences in the geometrical data for the same capacitors by different manufacturers. Unfortunately, this issue complicates the exact calculation of inductance.

IV. RESULTS

Estimates of $L_{connect,decap}$ were validated using FEM simulations in CST and using measurements. CST was chosen due to its flexible and easy to use graphical user interface. A simplified model of the capacitor, which replaces the internal electrode stack with a solid conductor, is first evaluated to demonstrate that the gains in compute time achieved with this simpler model do not sacrifice accuracy. Simulated values of inductance for the simplified capacitor model are then compared with measurements. Finally, results found using FEM and using the simplified and complex PEEC models are compared below.

A. Model of Mounted Capacitor

While modeling the entire electrode stack might lead to improved accuracy, modeling the many conductors in the electrode stack significantly increases the computational effort [20], [29], [30]. To demonstrate the impact of using a PEEC block model, simulations of FEM models for an 0603 100 nF capacitor and its straight connections were conducted where all 54 electrode plates were included in the model and where the electrode plates were replaced with a solid conductor. Fig. 12(a) shows the model

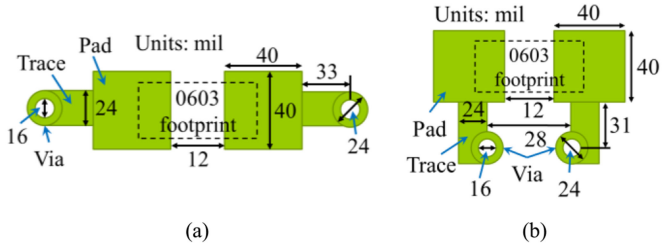


Fig. 13. Dimensions of the (a) straight; (b) *L*-shaped layouts [31].

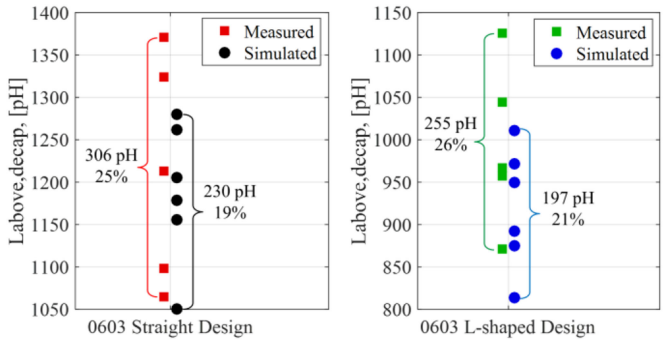


Fig. 14. Variation of measured and simulated values of $L_{above,decap}$ while changing the 0603 capacitor's geometry and placement. (a) Straight. (b) *L*-shaped layout designs.

which includes the electrode plates and Fig. 12(b) shows the model where the electrodes are approximated as a solid conductive block. Both models were solved using FEM and were built using the average geometric information in Table III. Geometric information for the pads is given in Fig. 13. The vias, pads, traces, and capacitor body were discretized using tetrahedral meshing with a maximum 3 mil mesh step width. Experiments were performed to demonstrate acceptable convergence for this discretization density. The loop inductance, $L_{above,decap}$, for the detailed capacitor model in Fig. 12(a) was 1092 pH, and was 1179 pH for the approximated body model in Fig. 12(b). The 87 pH (7%) difference between the models is small considering the large difference in compute time.

B. Measurements

In this section, we compare values for the inductance of a 0603 capacitor found through simulation of the FEM model and found through measurements. Results are found for both the straight and L-shaped contact layouts shown in Fig. 13. For the measurements, the decoupling capacitors were mounted on a fixture consisting of a standard 4-layer PCB, with two SMA ports connected to the plane below the two ground planes [32]. To obtain $L_{above,decap}$, a measurement of the transfer impedance between the two ports was used to measure the inductance, L_1, into the PDN including the capacitor, pads, vias, and the ground plane. The inductance of the PCB layers and vias, L_2, was also measured, where the decoupling capacitor inductance is eliminated from the measurement by shorting the via to the return plane [32]. The inductance $L_{above,decap}$ was found by subtracting the two measured inductances, i.e.,

$$L_{above,decap} = L_1 - L_2 \tag{3}$$

The inductance for the mounted capacitor varies between manufacturers and between tests depending on the internal structure of the capacitor [23] and on the soldering details, which can cause variations in the distance between the capacitor and return plane or position of the capacitor on the pads. Since the precise geometries associated with the measured capacitors were not known, measurements of inductance were made using five 0603 100 nF capacitors of the same capacitance but from different manufacturers. An attempt was made to minimize the amount of solder on the pad and thus the variation in the height of the capacitor above the return plane with solder thickness. Measurements were made for both straight and for L-shaped connections as shown in Fig. 2. FEM models were built using the geometric information in Table III while modeling the electrode plates as a solid conductive block as shown in Fig. 2.

TABLE VI
AVERAGE VALUES OF $L_{ABOVE,DECAP}$

	Straight Layout [pH]	L-shaped Layout [pH]
Simulated (Fig. 2)	1188	919
Measured	1214	993
Difference	2%	8%

The measured results are compared in Fig. 14 to results found using FEM, and are summarized in Table VI. The measured values of inductance vary by about 26% for the straight and L-shaped connection layouts. As expected, the inductance for the straight layout was higher than for the L-shaped layout. Variations in the values of inductance closely matched the measurement. As shown in Table VI, the difference between the average inductance found with the FEM solver and the measurement was within 8%, providing confidence in the methods used to determine $L_{above,decap}$.

The slightly higher inductance values in the measurements compared to the FEM results can be attributed to solder tilting or a small rotation of the capacitor in the measurement setup above the return plane. These changes in placement of the decoupling capacitors have not been included in the FEM modeling.

C. Results for Simple Partitioning of $L_{above,decap}$ FEM Model

As introduced in Fig. 1, the vertical partitioning approach separates the inductance $L_{above,decap}$ into a part associated with the traces and vias, $L_{connect}$, and a portion associated with the capacitor and its pads, L_{cap}. In this section, we evaluate the error resulting from using this partitioning. Fig. 2(a) and Fig. 2(b) show the models for the straight and L-shaped layout without partitioning, and Fig. 3 and Fig. 4 show the models with partitioning. The partitioning cuts were made at the connection between the trace and pads for this study. The inductance values for L_{cap}, $L_{connect}$ were computed using the presented partitioning approach and then used to estimate $L_{above,decap}$. The estimates for $L_{above,decap}$ are compared to values found by

TABLE VII
INDUCTANCE ESTIMATED WITH PARTITIONING APPROACH USING FEM

Straight Design					
Height, h, [mil]	Partitioning Approach			Direct Sim.	error
	$L_{connect}$ [pH]	L_{cap} [pH]	$L_{above,decap} \approx L_{connect} + L_{cap}$ [pH]	$L_{above,decap}$ [pH]	
3	158	457	615	622	2%
5	246	547	793	769	3%
6	286	590	876	836	5%
8	362	671	1033	960	8%
10	438	748	1186	1073	11%
12	510	823	1333	1179	13%
L-shaped Design					
Height, h, [mil]	Partitioning Approach			Direct Sim.	error
	$L_{connect}$ [pH]	L_{cap} [pH]	$L_{above,decap} \approx L_{connect} + L_{cap}$ [pH]	$L_{above,decap}$ [pH]	
3	160	416	576	547	5%
5	246	481	727	645	13%
6	286	513	767	687	16%
8	364	572	936	759	23%
10	436	629	1065	820	29%
12	508	684	1192	875	36%

simulating the entire structure in Table VII. While the capacitor and pad geometries did not change for the straight and L-shaped layouts, the values for L_{cap} differ between the designs because of the port locations. Results shown in Table VII were obtained using FEM simulations to validate the partitioning approach.

As shown in Table VII, the accuracy of the simple partitioning approach is a function of the thickness of the dielectric spacing under the capacitor. This error is due to the missing mutual inductive coupling between L_{cap} and $L_{connect}$. It is not surprising that the error increases with the distance of the connections from the return plane. Dielectric thickness in high-speed, multilayer PCBs, however, does not exceed 6 mil, which suggests the error should not exceed 16% in these applications. The general connection model with mutual inductances in Section II.B can be used to eliminate this error, which is accomplished by adding the partial mutual inductances between the existing $L_{connect}$ and L_{cap} PEEC models and by solving the combined PEEC model with these mutual inductances.

D. PEEC Inductance Model for $L_{above,decap}$

In this section, we compare estimates of the inductance between PEEC and FEM. First, we consider the L_{cap} inductance for an 0603 capacitor using both approaches. Values in this table were calculated using the average 0603 dimensions shown in Table III, using the pads dimensions shown in Fig. 13 and using a capacitor height, *h,* of 5 mils. Results were found both for a detailed PEEC model, using a complex 3D model of the structure, with hundreds of mesh cells as shown in Fig. 8, and for a simplified PEEC model, using a few tens of mesh cells as shown in Fig. 7. The simplified PEEC model can simply be solved using analytical equations as discussed in Section III.A. The results for both the simplified and the detailed L_{cap} models are shown in Table VIII. No results are shown for the simplified PEEC model for the L-shaped layout, since this model was only solved for the straight layout. The detailed and simplified PEEC models differed from the FEM model by 11% to 14%. These values are typically within the acceptable range of errors. The modestly larger values estimated by the detailed PEEC model may have resulted because the pads and terminals are approximated with zero thickness conductors. Importantly, the PEEC model required less than a minute to calculate the inductance of the capacitor, which illustrates the significant benefit of the PEEC models in comparison to the FEM model.

TABLE VIII
L_{CAP} FOUND USING PEEC AND FEM (100 NF 0603 CAPACITOR)

Design	FEM	Detailed PEEC	Simplified PEEC
L_{cap} for straight layout (Fig. 3(a)) [PH]	547	607	473
L_{cap} for L-shaped layout (Fig. 4(a)) [PH]	481	550	N/A

TABLE IX
SELF AND MUTUAL INDUCTANCES FOR CIRCUIT ELEMENTS SHOWN IN FIG. 7

$L_{p11,pad}$ [pH]	57.7	$L_{p12,pad}$ [pH]	29.7
$L_{p11,ter.}$ [pH]	81.7	$L_{p11,el.}$ [pH]	569.9
$L_{p12,ter.}$ [pH]	23.3	$L_{p12,el.}$ [pH]	279.9

The partial self- and mutual inductances calculated by the simple PEEC model for an 0603 capacitor are shown in Table IX [19]. Mutual inductances in the table are given with respect to a structure's image in the return plane, as shown in Fig. 7(b) [19]. Other mutual inductances were ignored. Using these values, the total equivalent inductance, L_{cap}, for the capacitor model in Fig. 7 can be found as:

$$L_{cap} = \frac{L_{p11} - L_{p12}}{2} \tag{4}$$

where

$$L_{p11} = 2\left(2L_{p11,pad} + 2L_{p11,ter.} + L_{p11,el.}\right) \tag{5}$$

$$L_{p12} = 2\left(2L_{p12,pad} + 2L_{p12,ter.} + L_{p12,el.}\right) \tag{6}$$

Analyzing the circuit elements in Table IX demonstrates that the conductor associated with the capacitor's electrodes is responsible for nearly 60% of the value of L_{cap}. The mutual coupling ($L_{p12,el.}$) between the capacitor and its image in the reference plane contributes substantially to the overall value of L_{cap} as well. In this case, the partial mutual inductance to the image is almost half the partial self-inductance of each component. The large contribution of this mutual inductance helps demonstrate the importance of considering the reference plane distance in the L_{cap} calculations.

V. DISCUSSION AND CONCLUSIONS

The main aim of this article is the efficient, accurate computation of decoupling capacitor inductances. They can contribute a fraction of the overall PDN system inductance which is important for high performance systems. Unfortunately, the single

ESL inductance value for the decoupling capacitor provided by the manufacturers is not an accurate value because it fails to account for the inductive coupling to the reference plane and other local physical parameters.

Determining the inductance associated with each decoupling capacitor layout in a VLSI package design is expensive using commercial CEM tools. Using the presented approaches to compute the values for a large number of decaps is time consuming. Further, some layout tools physically short the pads under the part as an approximation. This interferes with the strong coupling under the capacitor observed in this work, which we call the inductive coupling sandwich.

The partitioning techniques presented in this article result in the separation of the decap into several parts which are faster to evaluate. The partitioning is implemented with a horizontal part which separates the decap from the PDN circuit computation. Two vertical partitions are presented which allow the separate evaluation of the connection paths from the capacitor body parts. This is important, since the connection parts can assume different shapes. This allows multiple uses for the PEEC model parts. In the simpler approach, couplings are ignored if the pad-to-ground spacing is sufficiently small. This is the case for higher performance designs.

The simpler PEEC models developed here allow users to compute the equivalent inductance associated with the capacitor and pads without the use of extensive modeling tool. We give an example where a closed-form expression associated with this model estimated the inductance of a 0603 capacitor within 14% of the overall inductance.

An important simplification of the modeling is accomplished by replacing the detailed multiple plate internal model with a PEEC conductor block resulting in close inductance values. It is shown in this work that additional information on the physical measurements of the capacitors are required for accurate decap inductance models. Unfortunately, differences in physical details for different manufacturers were observed even for specific models.

Our results using the partitioning approach are useful to speed-up the computation of inductances for a large number of decaps in larger designs. Also, more accuracy of the decap elements can be helpful for the recently introduced machine learning model designs, which can be evaluated with the models presented.

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